UniSite

User Manual

DATA I/O
Corporation

981-0014-008

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Data I/O Corporation
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Redmond, Washington 98073-9746 USA
(206) 881-6444

Acknowledgments:

Safety Summary

General safety information for operating personnel is contained in this summary. In addition, specific WARNINGS and CAUTIONS appear throughout this manual where they apply and are not included in this summary.

Anti Static Wrist Strap

To avoid electric shock, the anti-static wrist strap must contain a 1MΩ (min) to 10MΩ (max) isolating resistor.

Definitions

WARNING statements identify conditions or practices that could result in personal injury or loss of life. CAUTION statements identify conditions or practices that could result in damage to equipment or other property.

Fuse Replacement

For continued protection against the possibility of fire, replace the fuse only with a fuse of the specified voltage, current and type ratings.

Grounding the Product

The product is grounded through the grounding conductor of the power cord. To avoid electric shock, plug the power cord into a properly wired and grounded receptacle only. Grounding this equipment is essential for its safe operation.

Power Cord

Use only the power cord specified for your equipment.

Power Source

Check the voltage selector indicator (located on the rear panel) to verify that the product is configured for the appropriate line voltage.

Servicing

To reduce the risk of electric shock, do not perform any servicing other than that described in this manual.

Symbols


This symbol appears on the equipment and it indicates that the user should consult the manual for further detail.


This symbol stands for VAC.


This symbol stands for fuse ratings.


This symbol denotes a ground connection.

Table of Contents

Product Definition

UniSite is a universal programmer that supports all device programming technologies such as EPROM, bipolar, MOS, CMOS, ECL and package types such as DIP, PLCC, LCC, PGA, and SOIC. UniSite provides support for programming, verifying, and testing all actively marketed programmable memory, logic, and microcontroller devices.

Product Overview

UniSite consists of:

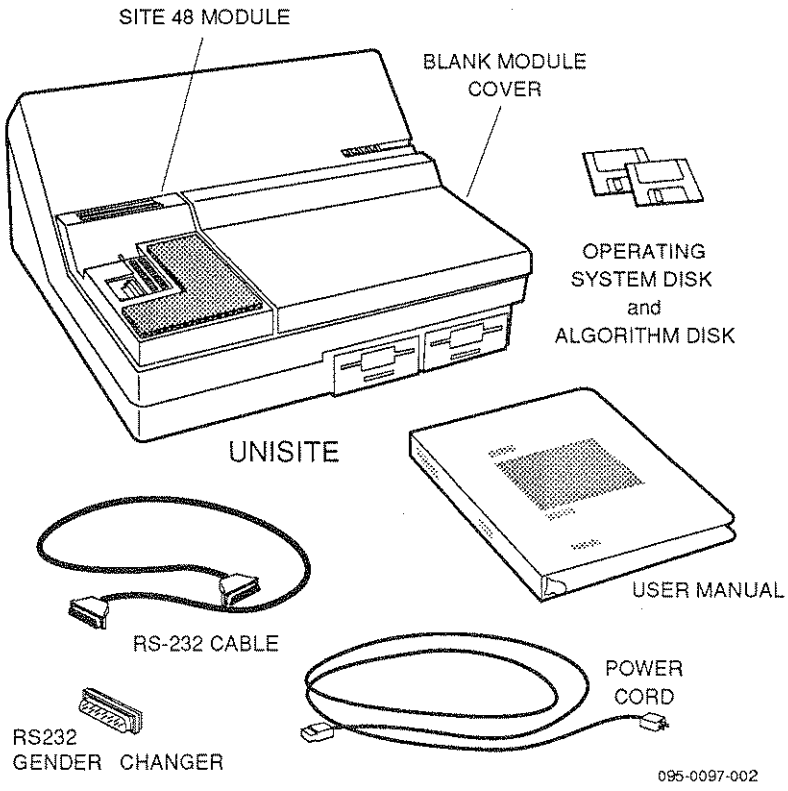

Figure 1
Contents of the UniSite Universal Programmer

A newly formatted UniSite disk can hold a total of 112 data files or 730,112 bytes of data, whichever is reached first. Both the system and algorithm disks each have space for user data files. Additional User RAM is optional.

Another option is the PinSite module, which provides device support for Plastic Leaded Chip Carrier (PLCC), Leadless Chip Carrier (LCC), Pin Grid Array (PGA) and Small Outline IC (SOIC) device packages. Also available is the SetSite module, which allows set/gang programming of up to eight DIP EPROMs or EEPROMs simultaneously.

Specifications

Functional

User RAM	1 Mbyte standard (4 Meg total User RAM optional)
Disk Format	Dual-sided, dual-density 3.5 inch disk with 135 tracks per inch (T.P.I).
Controller	68000, 16-bit microprocessor controlled
Terminal Support	Interfaces with ANSI X3.64 standard terminal (VT-100 Type), IBM PC running a terminal emulator program, and many popular ASCII terminals
SmartPort	Automatic port configuration feature
Communication Standard	RS-232C
Data transfer rate	110 to 115.2K baud

Power Requirements

Operating Voltages	120Vac or 240 Vac ±10%
Frequency Range	48 - 63 Hz
Power Consumption	500VA maximum
Fuse Ratings	250V/6A/F (Fast Blow)

Physical and Environmental

Dimensions	18.06h x 43.48w x 36.20d cm (7.11h x 17.12 w x 14.25d in.)
Weight	10.9 kg (24lb) Shipping Weight: 16.3 kg (36 lb)
Operating Temperature	+10° to +40°C (+50° to +105°F)
Storage Temperature	+4° to +50°C (+40° to + 122°F)
Relative Humidity	8% To 80% RH Non-Condensing
Operating Altitude	To 5,000 meters

Safety

UniSite is designed to comply with the following safety standards.

Underwriters Laboratories	UL 1244
Canadian Standard Association	CSA C22.2 NO. 151
International Electrotechnical Commission	IEC 348

Electromagnetic Emissions

UniSite is certified to meet: VDE 0871 Limit B (FTZ 1046)

Note: ***Periodic Maintenance/calibration*** *– UniSite is a state-of-the-art self-calibrating precision instrument. To assure that your UniSite remains fully calibrated, Data I/O recommends that the customer cycle power at least every three months. Alternatively, a customer may run one complete cycle of Self Test at least every three months.*

Certificate of RFI/EMI Compliance With VDE 0871 Level B

Data I/O certifies that the UniSite complies with the Radio Frequency Interference (RFI) and Electromagnetic Interference (EMI) requirements of VDE 0871 level B, as required in West German postal regulation number vfg 1046/1984, page 1943. Data I/O further certifies that the German Postal Service (DBP) has been notified of Data I/O's intention to market this equipment in West Germany. Data I/O acknowledges that the DBP reserves the right to retest this equipment to verify its compliance with the regulation.

Options and Accessories

Following is a list of available UniSite options. The order name column on the left lists the name of the option you should use when calling Data I/O.

Option (Order Name)	Description
USRAM128TO1	128KB-1MB Upgrade (Service Center Installed)
USRAM512TO1	512KB-1MB Upgrade (Service Center Installed)
USRAM128TO4	128K-4MB RAM Upgrade (Service Center Installed)
USRAM1TO4	512KB/1MB RAM Upgrade to 4MB RAM (Service Center Installed)
USHANDLERSITE	Handler Interface
USSETSITE	Gang/Set Programming Module
USPINSITE	PinSite for PLCC, SOIC, and PGA packages
USPINDRIVER	Additional pindriver boards
USUSERMAN	Operator's Manual
USMAINTMAN	Service Manual
USCABLESET	6' RS-232C cable with Gender Changer
USSUPPORT	Software update service (12 months)

Contacting Customer Support

If you require technical assistance with your UniSite, there are two ways to contact Customer Support: one for users inside the United States, and one for users outside the United States.

In the United States, the Data I/O Customer Resource Center is staffed with Support Engineers between 6:00 AM and 5:00 PM Pacific Time. Outside the United States, you should call your local Data I/O representative. For the phone number of your local Data I/O representative, refer to the Warranty Service section of this chapter.

Regardless of whether you call Data I/O or your local Data I/O representative, you can ensure quick and accurate phone assistance by following the steps below:

1. Have your programmer (and terminal) in front of you.
2. Have the UniSite Operator Manual available.
3. Be ready to provide the following information:
   - Type of modules installed (SetSite, PinSite etc.) and number of pin drivers installed
   - Manufacturer and part number of the device you are using
   - Error codes and messages exactly as they appeared

- Disk Software revision numbers; to find these numbers, refer to the UniSite power-up screen.
- UniSite serial number; to find this number, refer to the UniSite back panel.

The phone numbers for the Data I/O Customer Resource Center and the Data I/O representatives are listed in the Warranty Service section of this chapter.

Customer Support BBS

In addition to talking to the Data I/O Customer Resource Center, you can also call the Data I/O Customer Support Electronic Bulletin Board System (BBS).

From the Customer Support BBS you can obtain a wide range of information on Data I/O products, including current product information, new revision information, known bugs (and work-arounds), helpful application notes, and other miscellaneous information. In addition, the BBS has a collection of DOS utilities you can download.

The Customer Support BBS also has a message facility which allows you to leave messages to Customer Support Personnel. For example, you could request support for a specific device, or suggest how we can improve our products. Or you could leave us a message telling us what you think of Data I/O product(s).

To learn more about the Data I/O Customer Support BBS, call it at (206) 882-3211. The protocol is 1200/2400/9600 (Courier HST) baud, 8 data bits, 1 stop bit, and no parity. On-line help files are available throughout the BBS to help you learn more about the BBS.

Warranty Service

Data I/O maintains customer support centers throughout the world, each staffed with factory-trained technicians to provide prompt, quality service. This includes not only repairs, but calibration of all Data I/O products.

Data I/O Corporation warrants its products against defects in materials and workmanship for a period of ninety (90) days for software and one (1) year for hardware unless specified otherwise, which begins when the equipment is shipped. Refer to the warranty card inside the back cover of this manual for information on the length and conditions of the warranty. For warranty service, contact your nearest Data I/O Customer Support Center. If you return the unit for service, please return the disks with the unit. If you do not have a name or phone number for your nearest office, the following is a list of Data I/O offices:

United States
Data I/O Corporation
10525 Willows Road N.E.
P.O. Box 97046
Redmond, WA 98073-9746
Telephone: (206) 881-6444
Fax: (206) 882-1043
Telex: 152167 (Inside U.S.)
4740166 (Outside U.S.)

U.S. Customer Resource Center
(800) 247-5700

Customer Support BBS
(206) 882-3211

Data I/O San Jose
1701 Fox Drive
San Jose, CA 95131
Telephone (408) 437-9600
Fax: (408) 437-1218

Data I/O New Hampshire
20 Cotton Road
Nashua, NH 03063
Telephone (603) 889-8511
(800) 858-5803 (NJ & NY only)
Fax: (603) 880-0697

Data I/O Japan
Sumitomoseimei
Higashishinbashi Bldg. 8F
2-1-7, Higashi-Shinbashi
Minato-Ku, Tokyo 105, Japan
Telephone: (03) 432-6991
Fax: (03) 432-6094 (Sales)
(03) 432-6093 (Other)
Telex: 2522685 DATAIO J

Data I/O Canada
6725 Airport Road, Suite 302
Mississauga, Ontario
L4V 1V2 Canada
Telephone: (416) 678-0761
Fax: (416) 678-7306

Data I/O-Instrumatic Electronic Systems Vertriebs GmbH
Lochhammer Schlag 5a
D-8032 Gräelfing
West Germany
Telephone (0)89 858580
Fax: (0)89 8585810

Data I/O Europe
World Trade Center
Strawinskylaan 633
1077 XX Amsterdam
Telephone: +31 (0)20-6622866
Fax: +31 (0)20-6624427
Telex: 16616 DATIO NL

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10. No Waiver. The failure of either party to enforce any rights granted hereunder to take action against the other party in the event of any breach hereunder shall not be deemed a waiver by that party as to subsequent enforcement of rights or subsequent actions in the event of future breaches.

How To Use This Manual

This manual is organized to first provide information for quick and easy part identification and set up in the Getting Started section. The section following, Sample Sessions, is devoted to showing example programming situations. The remainder of the manual provides important reference information, including commands, messages, CRC operation and translation formats.

Listed below are descriptions of the sections in this manual.

- **Getting Started** — This section offers general information about how to begin using UniSite. Included in this section are descriptions of all the front and rear panel features, a description of how to power up and procedures on changing the line fuse.
- **Sample Sessions** — This section contains five sample programming sessions. Each session shows a typical programming example.
- **Commands** — Information in this section explains all UniSite's commands. The information in this section can be accessed quickly by using the command tree in the front of the section as a guide.
- **Messages** — The messages documented in this section are UniSite's system messages only. Descriptions of all other UniSite error messages are available through the UniSite User Interface.
- **Computer Remote Control** — The information necessary to operate UniSite in Computer Remote Control is located in this section.
- **Translation Formats** — This section provides descriptions of all data translation formats supported by UniSite.
- **Index** — This is an alphabetical guide to all major topics covered in this manual.

Typographic Conventions

Throughout this manual different typographic conventions represent different cases of input and output.

Filenames

Filenames will be displayed in an italic typeface. For example, *source.hex* and *autoexec.bat* are filenames.

Note: DOS is not case-sensitive; commands can be entered in either upper- or lower-case.

User Input

Keyboard Keys

Keyboard keys, such as the alpha numeric keys, are shown in boxes. For example, [Q] .

The Enter key (or on some keyboards, the Return key) is shown as this symbol [↵] .

Key Combinations

Key combinations, such as Control-Z, are shown as two key boxes separated by a dash. For example, [Ctrl] – [Z] .

A key combination like [ESC] [Ctrl] – [T] means to press and release [ESC] , then press [Ctrl] and [T] at the same time.

Keyboard Input

Longer strings of keyboard input will be shown like keyboard keys, but without the surrounding box. For example,

you should type in what you see in this typeface.

Variable inputs are italicized within the input line and should be replaced with the requested information. For example,

copyexactly *filename.hex*

means type in **copyexactly** just as you see it and replace ***filename.hex*** with the name of your file.

Displayed Messages

Text that appears on the screen will be displayed in a typewriter-like typeface. For example,

```
You will see this text displayed on the screen.
```

UniSite™

Universal Programmer

User Notes – Version 4.2

DATA I/O

984-0014-031

June 1993 984-0014-031

Data I/O Corporation
10525 Willows Road N.E., P.O. Box 97046
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(206) 881-6444

Acknowledgments:

What's New in Version 4.2

The User Notes include the most current information about device support and new features and enhancements to your UniSite. Read the following Special Notes before proceeding to the rest of the User Notes.

Special Notes

PPI-5101 and PPI-5102 Users

This note applies only if you are using PinSite with the PPI-5101 adapter or the PPI-5102 adapter.

We are in the process of optimizing the way the UniSite system software controls the PPI adapters. The net effect of the optimization will be to improve programming yields and speeds. In order to maintain as much backwards compatibility as possible, we have decided to implement the change in two steps.

The first step has been implemented in this release. The second and final step will be implemented in version 4.3, which is scheduled to be released in August 1993.

We anticipate that fewer than one half of 1% of our customers will be impacted by the changes made as a result of this first step. Specifically, you will have make sure neither Site40 nor Site48 is installed in UniSite when you perform a device operation using the PPI-5101 or the PPI-5102 with PinSite.

Similarly, you will have make sure neither PPI-5101 nor PPI-5102 is installed in PinSite when you perform a device operation using Site40 or Site48.

This workaround will only affect this version of system software. Version 4.3 will mark the second step of the two-step process described above and will eliminate the need for this workaround.

BBS Support Extended

The Keep Current algorithms are now available at no cost to all UniSite users who have the current version of UniSite software. Simply call the Keep Current BBS to register. See the *Keep Current User Manual* for more information.

Contents of these User Notes

The following sections comprise the remainder of the User Notes:

- **Updated Device Support** — The programming algorithms for over 165 devices have been updated since the last release.
- **New Device Support** — Over 205 new devices have been added since the last release.
- **New Features and Enhancements** — A brief description of the changes and additions for this release.
- **Installation Instructions** — Information about installing this new version of software.
- **Updated Manual Pages** — Replacement pages that bring your copy of the *UniSite User Manual* up-to-date. See the section titled "Updating Your Manual" for more information.
- **Technical Reference Guides** — New one-page troubleshooting guides designed to help you identify and resolve common problems.
- **Application Notes** — Two new Application Notes, Memory Chart and Programming 8-bit Devices for 16-bit and 32-bit Target Applications.
- **Device List** — A complete list of all devices supported by UniSite. Device List pages are identified by the prefix DL-. Place the Device List behind the Device List divider tab in your User Manual.

Updated Device Support

The programming algorithms for the devices listed below have been updated since the previous release. The algorithms were updated for one or more of the following reasons:

- A change in the specification issued by the semiconductor company
- An improvement in the programming algorithm to increase programming yields and/or to increase programming speed

Device Part Number	Pin Count	Package Type	Module	
AMI Semiconductor				
18CV8	20	DIP	Site 48/40	*
18CV8	20	PLCC	ChipSite	*
18CV8	20	PLCC	PinSite	*
Actel				
A1010-PG84	85	PGA	PinSite	*
A1010-PL68	68	PLCC	PinSite	*
A1010-PL68	68	PLCC	USM-340-001	*
A1010A-PG84	85	PGA	PinSite	*
A1010A-PL44	44	PLCC	PinSite	*
A1010A-PL44	44	PLCC	USM-340-002	*
A1010A-PL68	68	PLCC	PinSite	*
A1010A-PL68	68	PLCC	USM-340-001	*
A1010A-PQ100	100	QFP	PinSite	*
A1020-PL68	68	PLCC	PinSite	*
A1020-PL68	68	PLCC	USM-340-001	*
A1020A-CQ84	84	QFPCAR	PinSite	*
A1020A-JQ44	44	JLCC	PinSite	*
A1020A-JQ68	68	JLCC	PinSite	*
A1020A-JQ84	84	JLCC	PinSite	*
A1020A-PG84	85	PGA	PinSite	*
A1020A-PL44	44	PLCC	PinSite	*
A1020A-PL44	44	PLCC	USM-340-002	*
A1020A-PL68	68	PLCC	PinSite	*
A1020A-PL68	68	PLCC	USM-340-001	*
A1020A-PL84	84	PLCC	PinSite	*
A1020A-PL84	84	PLCC	USM-340-002	*
A1225-PG100	100	PGA	PinSite	*
A1225-PL84	84	PLCC	PinSite	*
A1225-PQ100	100	QFP	PinSite	*
A1240-PG132	132	PGA	PinSite	*
A1240-PL84	84	PLCC	PinSite	*
A1240-PQ144	144	QFP	PinSite	*
A1280-PG176	176	PGA	PinSite	*
A1280-PQ160	160	QFP	PinSite	*
Advanced Micro Devices/MMI				
CE22V10H-10/5	24	DIP	PinSite	*
CE22V10H-10/5	24	DIP	Site 48/40	
CE22V10H-10/5	28	PLCC	ChipSite	

* *Indicates a device that had its programming algorithms changed because the semiconductor company changed the specification for the device.*

Device Part Number	Pin Count	Package Type	Module	
CE22V10H-10/5	28	PLCC	PinSite	*
CE22V10H-15/4	24	DIP	Site 48/40	
CE22V10H-15/4	24	SO	ChipSite	
CE22V10H-15/4	24	SO	PinSite	
CE22V10H-15/4	28	PLCC	ChipSite	
CE22V10H-15/4	28	PLCC	PinSite	
CE22V10H-25/4	24	DIP	Site 48/40	
CE22V10H-25/4	24	SO	ChipSite	
CE22V10H-25/4	24	SO	PinSite	
CE22V10H-25/4	28	PLCC	ChipSite	
CE22V10H-25/4	28	PLCC	PinSite	
CE22V10H-7/5	24	DIP	Site 48/40	
CE22V10H-7/5	28	PLCC	ChipSite	
CE22V10H-7/5	28	PLCC	PinSite	
CE22V10Q-10/5	24	DIP	Site 48/40	
CE22V10Q-25/4	24	DIP	Site 48/40	
CE22V10Q-25/4	28	PLCC	ChipSite	
CE22V10Q-25/4	28	PLCC	PinSite	
CE29MA16/4	24	DIP	Site 48/40	
CE29MA16/4	28	PLCC	ChipSite	
CE29MA16/4	28	PLCC	PinSite	
Altera Corporation				
5192	84	JLCC	PinSite	
5192	84	PGA	PinSite	
5192	84	PLCC	PinSite	
Cypress Semiconductor, Inc.				
100E301/16P8	24	DIP	Site 48/40	*
100E301/16P8	28	PLCC	ChipSite	*
100E301/16P8	28	PLCC	PinSite	*
100E302/16P4	24	DIP	Site 48/40	*
100E302/16P4	28	PLCC	ChipSite	*
100E302/16P4	28	PLCC	PinSite	*
10E301	28	LCC	ChipSite	*
10E301	28	LCC	PinSite	*
10E301	28	PLCC	ChipSite	*
10E301	28	PLCC	PinSite	*
10E301/16P8	24	DIP	Site 48/40	*
10E302/16P4	24	DIP	Site 48/40	*
16L8-4	28	PLCC	PinSite	*
16L8-5	20	DIP	Site 48/40	*
16L8-5	20	PLCC	ChipSite	*
16L8-5	20	PLCC	PinSite	*
16L8-7	20	DIP	Site 48/40	*
16L8-7	20	PLCC	ChipSite	*
16L8-7	20	PLCC	PinSite	*
16R4-4	28	PLCC	PinSite	*
16R4-5	20	DIP	Site 48/40	*
16R4-5	20	PLCC	ChipSite	*
16R4-5	20	PLCC	PinSite	*
16R4-7	20	DIP	Site 48/40	*
16R4-7	20	PLCC	ChipSite	*
16R4-7	20	PLCC	PinSite	*
16R6-4	28	PLCC	PinSite	*
16R6-5	20	DIP	Site 48/40	*
16R6-5	20	PLCC	ChipSite	*

Device Part Number	Pin Count	Package Type	Module	
16R6-5	20	PLCC	PinSite	*
16R6-7	20	DIP	Site 48/40	*
16R6-7	20	PLCC	ChipSite	*
16R6-7	20	PLCC	PinSite	*
16R8-4	28	PLCC	PinSite	*
16R8-5	20	DIP	Site 48/40	*
16R8-5	20	PLCC	ChipSite	*
16R8-5	20	PLCC	PinSite	*
16R8-7	20	DIP	Site 48/40	*
16R8-7	20	PLCC	ChipSite	*
16R8-7	20	PLCC	PinSite	*
7C341	84	JLCC	PinSite	
Hyundai Electronics Industries Co., Ltd.				
18CV8	20	DIP	Site 48/40	*
Intel Corporation				
28F200BX-B	44	SOP	PinSite	*
28F200BX-B	44	SOP	SetSite	*
28F200BX-T	44	SOP	PinSite	*
28F200BX-T	44	SOP	SetSite	*
28F400BX-B	44	SOP	PinSite	*
28F400BX-B	44	SOP	SetSite	*
28F400BX-T	44	SOP	PinSite	*
28F400BX-T	44	SOP	SetSite	*
International CMOS Technology, Inc.				
18CV8	20	DIP	Site 48/40	*
18CV8	20	PLCC	ChipSite	*
18CV8	20	PLCC	PinSite	*
Lattice Semiconductor				
22V10	24	DIP	Site 48/40	
22V10	28	LCC	ChipSite	
22V10	28	LCC	PinSite	
22V10	28	PLCC	ChipSite	
22V10	28	PLCC	PinSite	
22V10B	24	DIP	PinSite	*
22V10B	24	DIP	Site 48/40	
22V10B	28	LCC	ChipSite	
22V10B	28	LCC	PinSite	
22V10B	28	PLCC	ChipSite	
22V10B	28	PLCC	PinSite	
22V10B-QP	24	DIP	Site 48/40	
ispLSI1016	44	PLCC	PinSite	*
ispLSI1016	44	PLCC	Site 48/40	*
ispLSI1024	68	PLCC	PinSite	*
ispLSI1024	68	PLCC	Site 48/40	*
ispLSI1032	84	PLCC	PinSite	*
ispLSI1032	84	PLCC	Site 48/40	*
ispLSI1048	120	QFP	Site 48/40	*
Mitsubishi Electronics of America				
37702E4	80	LCC	Site 48/40	*
37702E4	80	QFP	Site 48/40	*

Device Part Number	Pin Count	Package Type	Module	
Motorola Inc.				
68705S3-A20T	28	DIP	Site 48/40	
Philips Semiconductor				
10020EV8	24	DIP	Site 48/40	*
10020EV8	28	PLCC	ChipSite	*
10020EV8	28	PLCC	PinSite	*
10H20EV8	24	DIP	Site 48/40	*
10H20EV8	28	PLCC	ChipSite	*
10H20EV8	28	PLCC	PinSite	*
82HS187	24	DIP	Site 48/40	*
82HS187	28	PLCC	ChipSite	*
82HS187	28	PLCC	PinSite	*
82HS189	24	DIP	Site 48/40	*
82HS189	28	PLCC	ChipSite	*
82HS189	28	PLCC	PinSite	*
82HS191	24	DIP	Site 48/40	*
82HS191	28	PLCC	ChipSite	*
82HS191	28	PLCC	PinSite	*
82HS195	20	DIP	Site 48/40	*
82HS195	20	PLCC	ChipSite	*
82HS195	20	PLCC	PinSite	*
82HS321	24	DIP	Site 48/40	*
82HS321	28	PLCC	ChipSite	*
82HS321	28	PLCC	PinSite	*
PLUS105	28	DIP	Site 48/40	*
PLUS105	28	PLCC	ChipSite	*
PLUS105	28	PLCC	PinSite	*
PLUS405	28	DIP	Site 48/40	*
PLUS405	28	PLCC	ChipSite	*
PLUS405	28	PLCC	PinSite	*
SGS-Thomson Microelectronics				
27C1000	32	DIP	SetSite	*
27C1000	32	DIP	Site 48/40	*
27C1001	32	DIP	SetSite	*
27C1001	32	DIP	Site 48/40	*
27C1001	32	PLCC	ChipSite	*
27C1001	32	PLCC	PinSite	*
27C1024	40	DIP	SetSite	*
27C1024	40	DIP	Site 48/40	*
27C1024	44	PLCC	ChipSite	*
27C1024	44	PLCC	PinSite	*
27C2001	32	DIP	SetSite	*
27C2001	32	DIP	Site 48/40	*
27C256B	28	DIP	SetSite	*
27C256B	28	DIP	Site 48/40	*
27C256B	32	PLCC	ChipSite	*
27C256B	32	PLCC	PinSite	*
27C4001	32	DIP	SetSite	*
27C4001	32	DIP	Site 48/40	*
27C4002	40	DIP	SetSite	*
27C4002	40	DIP	Site 48/40	*
27C4002	44	PLCC	ChipSite	*
27C4002	44	PLCC	PinSite	*
27C512	28	DIP	SetSite	*
27C512	28	DIP	Site 48/40	*

Device Part Number	Pin Count	Package Type	Module	
27C512	32	PLCC	ChipSite	*
27C512	32	PLCC	PinSite	*
27C64A	28	DIP	Site 48/40	*
87C257	28	DIP	SetSite	*
87C257	28	DIP	Site 48/40	*
87C257	32	PLCC	ChipSite	*
87C257	32	PLCC	PinSite	*
Texas Instruments				
1830	68	JLCC	ChipSite	
1830	68	JLCC	PinSite	
1830	68	PLCC	ChipSite	
1830	68	PLCC	PinSite	
27C256	28	DIP	SetSite	*
27C256	28	DIP	Site 48/40	*
27PC256	28	DIP	SetSite	*
27PC256	28	DIP	Site 48/40	*
27PC256	32	PLCC	ChipSite	*
27PC256	32	PLCC	PinSite	*
TPC1010AFN-044	44	PLCC	PinSite	*
TPC1010AFN-044	44	PLCC	USM-340-002	*
TPC1010AFN-068	68	PLCC	PinSite	*
TPC1010AFN-068	68	PLCC	USM-340-001	*
TPC1010AMGB84	85	PGA	PinSite	*
TPC1010AVE-100	100	QFP	PinSite	*
TPC1020AFN-044	44	PLCC	PinSite	*
TPC1020AFN-044	44	PLCC	USM-340-002	*
TPC1020AFN-068	68	PLCC	PinSite	*
TPC1020AFN-068	68	PLCC	USM-340-001	*
TPC1020AFN-084	84	PLCC	PinSite	*
TPC1020AFN-084	84	PLCC	USM-340-002	*
TPC1020AMGB84	85	PGA	PinSite	*
TPC1240GB-133	133	PGA	PinSite	*
TPC1240VE-144	144	QFP	PinSite	*
TPC1280GB-176	176	PGA	PinSite	*
Waferscale Integration, Inc.				
PAC1000	88	PGA	PinSite	*
PSD301	44	JLCC	ChipSite	*
PSD301	44	JLCC	PinSite	*
PSD311	44	JLCC	ChipSite	*
PSD311	44	JLCC	PinSite	*
PSD311C1	44	PLCC	PinSite	*
Xilinx				
1765	8	DIP	Site 48/40	*
1765	20	PLCC	ChipSite	*
1765	20	PLCC	PinSite	*

New Device Support

The following devices have been added to UniSite since the previous release:

Device Part Number	Pin Count	Package Type	Module
Actel			
A1010-PL44	44	PLCC	USM-340-002
A1010A-PL44	44	PLCC	PinSite
A1010A-PL44	44	PLCC	USM-340-002
A1010B-PG84	85	PGA	PinSite
A1010B-PL44	44	PLCC	PinSite
A1010B-PL44	44	PLCC	USM-340-002
A1010B-PL68	68	PLCC	PinSite
A1010B-PL68	68	PLCC	USM-340-001
A1010B-PQ100	100	QFP	PinSite
A1020A-PL44	44	PLCC	PinSite
A1020A-PL44	44	PLCC	USM-340-002
A1020B-CQ84	84	QFPCAR	PinSite
A1020B-PG84	85	PGA	PinSite
A1020B-PL44	44	PLCC	PinSite
A1020B-PL44	44	PLCC	USM-340-002
A1020B-PL68	68	PLCC	PinSite
A1020B-PL68	68	PLCC	USM-340-001
A1020B-PL84	84	PLCC	PinSite
A1020B-PL84	84	PLCC	USM-340-002
A1020B-PQ100	100	QFP	PinSite
A1225A-PG100	100	PGA	PinSite
A1225A-PL84	84	PLCC	PinSite
A1225A-PQ100	100	QFP	PinSite
A1240A-PG132	132	PGA	PinSite
A1240A-PL84	84	PLCC	PinSite
A1240A-PQ144	144	QFP	PinSite
A1280A-PG176	176	PGA	PinSite
A1280A-PQ160	160	QFP	PinSite
Advanced Micro Devices/MMI			
16L8-5	20	PLCC	ChipSite
16L8-5	20	PLCC	PinSite
16R8-4	28	PLCC	PinSite
20L8-5	28	PLCC	ChipSite
20L8-5	28	PLCC	PinSite
20R6-5	28	PLCC	ChipSite
20R6-5	28	PLCC	PinSite
20R8-5	24	DIP	PinSite
20R8-5	24	DIP	Site 48/40
22V10-10/-15	28	PLCC	ChipSite
22V10-10/-15	28	PLCC	PinSite
22V10-7	24	DIP	Site 48/40
22V10-7	28	PLCC	ChipSite
22V10-7	28	PLCC	PinSite
27H010	32	LCC	ChipSite
27H010	32	LCC	PinSite
27H010	32	PLCC	ChipSite
27H010	32	PLCC	PinSite
27H256	32	PLCC	ChipSite
27H256	32	PLCC	PinSite
CE16V8H-7/5	20	PLCC	ChipSite

Device Part Number	Pin Count	Package Type	Module
CE16V8H-7/5	20	PLCC	PinSite
CE16V8HD-15	28	PLCC	ChipSite
CE16V8HD-15	28	PLCC	PinSite
CE16V8Z-25/4	20	SO	ChipSite
CE16V8Z-25/4	20	SO	PinSite
CE22V10H-10/5	24	DIP	PinSite
CE22V10H-10/5	24	DIP	Site 48/40
CE22V10H-10/5	28	PLCC	ChipSite
CE22V10H-10/5	28	PLCC	PinSite
CE610	24	DIP	PinSite
CE610	24	DIP	Site 48/40
CE610H	24	DIP	PinSite
CE610H	24	DIP	Site 48/40
Altera Corporation			
5130	84	JLCC	PinSite
5130	84	PLCC	PinSite
5130	100	PGA	PinSite
5130	100	QFP	PinSite
5130	100	QFPCAR	PinSite
7032	44	JLCC	PinSite
7032	44	PLCC	PinSite
7032	44	QFP	PinSite
7096	68	JLCC	PinSite
7096	68	PLCC	PinSite
7096	84	JLCC	PinSite
7096	84	PLCC	PinSite
EP610JC-25	28	JLCC	ChipSite
EP610JC-25	28	JLCC	PinSite
EP610JC-35	28	JLCC	ChipSite
EP610JC-35	28	JLCC	PinSite
EP610LC-15T	28	PLCC	PinSite
EP610LC-20T	28	PLCC	PinSite
EP610LC-25T	28	PLCC	PinSite
EP610PC-15T	24	DIP	Site 48/40
EP610PC-20T	24	DIP	Site 48/40
EP610PC-25T	24	DIP	PinSite
EP610PC-25T	24	DIP	Site 48/40
EPS464	44	JLCC	PinSite
EPS464	44	PLCC	PinSite
Asahi Kasei			
6420	8	SO	PinSite
6440	8	SO	PinSite
93C55	8	DIP	Site 48/40
93C55	8	SO	PinSite
93C65	8	SO	PinSite
Atmel Corporation			
22V10B	28	LCC	ChipSite
22V10B	28	LCC	PinSite
22V10B	28	PLCC	ChipSite
22V10B	28	PLCC	PinSite
27C040	32	LCC	PinSite
27C040	32	PLCC	ChipSite
27C040	32	PLCC	PinSite
27C1024	44	PLCC	ChipSite

Device Part Number	Pin Count	Package Type	Module
27C1024	44	PLCC	PinSite
27HC1024	44	JLCC	ChipSite
27HC1024	44	JLCC	PinSite
27LV010	32	LCC	ChipSite
27LV010	32	LCC	PinSite
27LV010	32	PLCC	ChipSite
27LV010	32	PLCC	PinSite
27LV256R	32	LCC	ChipSite
27LV256R	32	LCC	PinSite
27LV256R	32	PLCC	ChipSite
27LV256R	32	PLCC	PinSite
27LV512R	32	LCC	ChipSite
27LV512R	32	LCC	PinSite
27LV512R	32	PLCC	ChipSite
27LV512R	32	PLCC	PinSite
29LV512	32	DIP	Site 48/40
29LV512	32	PLCC	ChipSite
29LV512	32	PLCC	PinSite
Catalyst Semiconductor			
24C08	8	DIP	Site 48/40
28C64B	32	PLCC	ChipSite
28C64B	32	PLCC	PinSite
Cypress Semiconductor, Inc.			
22V10G	24	DIP	Site 48/40
22V10G	28	PLCC	ChipSite
22V10G	28	PLCC	PinSite
22VP10G	24	DIP	Site 48/40
22VP10G	28	PLCC	ChipSite
22VP10G	28	PLCC	PinSite
610	28	PLCC	ChipSite
610	28	PLCC	PinSite
7B333B	28	DIP	Site 48
7B333B	28	LCC	PinSite
7B333B	28	PLCC	ChipSite
7B333B	28	PLCC	PinSite
7C266	32	PLCC	ChipSite
7C266	32	PLCC	PinSite
7C270	44	LCC	ChipSite
7C270	44	LCC	PinSite
7C270	44	PLCC	ChipSite
7C270	44	PLCC	PinSite
7C276	44	LCC	ChipSite
7C276	44	LCC	PinSite
7C276	44	PLCC	ChipSite
7C276	44	PLCC	PinSite
7C335	28	PLCC	PinSite
7C341	84	PGA	PinSite
7C341	84	PLCC	PinSite
CY7C381-0JC	44	PLCC	PinSite
CY7C382-0JC	68	PLCC	PinSite
CY7C383-0JC	68	PLCC	PinSite
CY7C384-0JC	84	PLCC	PinSite
PALC22V10B	28	LCC	ChipSite
PALC22V10B	28	LCC	PinSite

Device Part Number	Pin Count	Package Type	Module
Hitachi, Ltd.			
27C4000	40	DIP	Site 48/40
58C256	28	SO	PinSite
58C66	28	SO	PinSite
6473388	84	LCC	PinSite
6475368	84	LCC	PinSite
6475368	84	PLCC	PinSite
Intel Corporation			
28F200BX-B	44	SOP	PinSite
28F200BX-B	44	SOP	SetSite
28F200BX-T	44	SOP	PinSite
28F200BX-T	44	SOP	SetSite
28F400BX-B	44	SOP	PinSite
28F400BX-B	44	SOP	SetSite
28F400BX-T	44	SOP	PinSite
28F400BX-T	44	SOP	SetSite
IFX780-10	132	BQFP	PinSite
KU87C51SL	100	BQFP	PinSite
International CMOS Technology, Inc.			
20CG10A	24	DIP	Site 48/40
Lattice Semiconductor			
16LV8	20	DIP	Site 48/40
16V8C	20	DIP	Site 48/40
16V8C	20	PLCC	ChipSite
16V8C	20	PLCC	PinSite
16V8Z	20	DIP	Site 48/40
16V8Z	20	PLCC	ChipSite
16V8Z	20	PLCC	PinSite
20LV8	24	DIP	Site 48/40
20V8C	24	DIP	Site 48/40
20V8C	28	PLCC	ChipSite
20V8C	28	PLCC	PinSite
20V8Z	24	DIP	Site 48/40
20V8Z	28	PLCC	ChipSite
20V8Z	28	PLCC	PinSite
22V10B	24	DIP	PinSite
22V10B	24	DIP	Site 48/40
22V10B-QP	28	PLCC	ChipSite
22V10B-QP	28	PLCC	PinSite
22V10B-QPUES	28	PLCC	ChipSite
22V10B-QPUES	28	PLCC	PinSite
22V10C	24	DIP	Site 48/40
22V10C	28	PLCC	ChipSite
22V10C	28	PLCC	PinSite
22V10CUES	24	DIP	Site 48/40
22V10CUES	28	PLCC	ChipSite
22V10CUES	28	PLCC	PinSite
6001	28	PLCC	ChipSite
6001	28	PLCC	PinSite
6001B	28	PLCC	ChipSite
6001B	28	PLCC	PinSite

Device Part Number	Pin Count	Package Type	Module
Macronix Inc.			
27C4000	32	DIP	Site 48/40
Microchip Technology Inc.			
16C57	28	SO	PinSite
Mitsubishi Electronics of America			
28F101	32	SO	PinSite
37702E6	80	LCC	Site 48/40
37702E6	80	QFP	Site 48/40
M6M72561J	68	PLCC	PinSite
Mitsubishi Plastics			
0512EP1TC20	32	CARD	Site 48
National Semiconductor Corp.			
22CV10-10	24	DIP	Site 48/40
22CV10-10	28	PLCC	ChipSite
22CV10-10	28	PLCC	PinSite
22CV10-7	24	DIP	Site 48/40
22CV10-7	28	PLCC	ChipSite
22CV10-7	28	PLCC	PinSite
27C020	32	DIP	SetSite
27C020	32	DIP	Site 48/40
27LV010	32	TSOP	PinSite
27LV512	32	TSOP	PinSite
27P210	44	PLCC	ChipSite
27P210	44	PLCC	PinSite
Oki Electric Industry Co., Ltd.			
27C802	42	DIP	Site 48
27C802	44	SO	PinSite
27C822	42	DIP	Site 48
27C822	44	SO	PinSite
27C832	42	DIP	Site 48
27C832	44	SO	PinSite
Philips Semiconductor			
27C010	32	DIP	SetSite
27C010	32	DIP	Site 48/40
27C512	28	SO	PinSite
87C51FB	44	JLCC	ChipSite
87C51FB	44	JLCC	PinSite
87C51FB	44	PLCC	ChipSite
87C51FB	44	PLCC	PinSite
87C52	44	QFP	PinSite
87C654	44	QFP	PinSite
QuickLogic Corporation			
QL12X16-0PL68C	68	PLCC	PinSite
QL12X16-0PL84C	84	PLCC	PinSite
QL8X12-0PL44C	44	PLCC	PinSite

Device Part Number	Pin Count	Package Type	Module
Ricoh Corporation			
16RP4B	20	SO	ChipSite
16RP4B	20	SO	PinSite
SGS-Thomson Microelectronics			
27C2001	32	PLCC	ChipSite
27C2001	32	PLCC	PinSite
28F101	32	DIP	Site 48/40
28F101	32	PLCC	ChipSite
28F101	32	PLCC	PinSite
28F102	40	DIP	Site 48/40
28F512	32	DIP	Site 48/40
28F512	32	PLCC	ChipSite
28F512	32	PLCC	PinSite
Seiko Epson			
BWB065 YO	68	CARD	PinSite
BWB129SDX	68	CARD	PinSite
HWB513-XO	68	CARD	Site 48/40
Sharp Corporation			
CE-776S	45	CARD	Site 48/40
Silicon Storage Technology, Inc.			
28EE010	32	DIP	Site 48/40
Texas Instruments			
20L8-5	24	DIP	PinSite
20L8-5	24	DIP	Site 48/40
20R8-5	24	DIP	PinSite
20R8-5	24	DIP	Site 48/40
22V10-10	28	PLCC	ChipSite
22V10-10	28	PLCC	PinSite
28F010	32	PLCC	ChipSite
28F010	32	PLCC	PinSite
28F210	40	DIP	Site 48/40
28F512	32	DIP	Site 48/40
28F512	32	PLCC	ChipSite
28F512	32	PLCC	PinSite
320E17	44	JLCC	PinSite
320P14	68	PLCC	ChipSite
320P14	68	PLCC	PinSite
320P15	40	DIP	Site 48/40
320P15	44	PLCC	PinSite
320P17	40	DIP	Site 48/40
TPC1010AFN-044	44	PLCC	PinSite
TPC1010AFN-044	44	PLCC	USM-340-002
TPC1010BFN-044	44	PLCC	PinSite
TPC1010BFN-044	44	PLCC	USM-340-002
TPC1010BFN-068	68	PLCC	PinSite
TPC1010BFN-068	68	PLCC	USM-340-001
TPC1010BVE-100	100	QFP	PinSite

Device Part Number	Pin Count	Package Type	Module
TPC1020AFN-044	44	PLCC	PinSite
TPC1020AFN-044	44	PLCC	USM-340-002
TPC1020AMHT84	84	QFPCAR	PinSite
TPC1225AVE-100	100	QFP	PinSite
TPC1280VB-160	160	QFP	PinSite
Toshiba America			
541001A	32	DIP	Site 48/40
541001A	32	SO	PinSite
544000	32	SO	PinSite
58F010	32	DIP	Site 48/40
9800P	20	SO	PinSite
9806P	20	DIP	Site 48/40
Waferscale Integration, Inc.			
57C191C	28	LCC	PinSite
57C191C	28	PLCC	ChipSite
57C191C	28	PLCC	PinSite
Xicor, Inc.			
28C010	32	PLCC	ChipSite
28C010	32	PLCC	PinSite
28HC16	24	DIP	Site 48/40
28HC16	24	SO	PinSite
28HC256	28	DIP	Site 48/40
28HC256	32	PLCC	ChipSite
28HC256	32	PLCC	PinSite
28HC64	28	DIP	Site 48/40
28HC64	28	SO	PinSite
28HC64	32	LCC	PinSite
28HC64	32	PLCC	ChipSite
28HC64	32	PLCC	PinSite
Xilinx			
XC17128	8	DIP	Site 48/40
XC17128	20	PLCC	ChipSite
XC17128	20	PLCC	PinSite
XC1718D	8	DIP	Site 48/40
XC1718D	8	SO	PinSite
XC1718D	20	PLCC	ChipSite
XC1718D	20	PLCC	PinSite
XC1736D	8	DIP	Site 48/40
XC1736D	8	SO	PinSite
XC1736D	20	PLCC	ChipSite
XC1736D	20	PLCC	PinSite
XC1765D	8	DIP	Site 48/40
XC1765D	8	SO	PinSite
XC1765D	20	PLCC	ChipSite
XC1765D	20	PLCC	PinSite

New Features and Enhancements

In addition to the updated and new device support, Version 4.2 also adds these new features and changes:

- Changed the way the **n40]** CRC command works. For more information, see the description of the **n40]** command on pages 6-22 to 6-24 of the *UniSite User Manual.*
- Added the High Speed Logic Drivers parameter to the list of parameters that can be saved/restored with the Save Configuration and Restore Configuration commands. For more information, see the description starting on page 5-28 of the *UniSite User Manual.*
- Added the **n4A]** CRC command, which can be used by QuickComm to load files from disk. For more information, see the description of the **n4A]** command on page 6-25 of the *UniSite User Manual.*

Updating Your Manual

The most current manual pages for Version 4.2 contain the June 1993 printing date at the bottom of the page. Please update your manual with the new pages.

Following are brief descriptions of the changes affecting each replacement page:

- 6-21 to 6-26 — Expanded and updated the description of the **n40]** CRC command beginning on page 6-22.

  Added the **n4A]** CRC command to page 6-25.
- Technical Reference Guides — Insert the new Technical Reference Guides behind the Messages chapter in your *UniSite User Manual.* The Guides are designed to help you troubleshoot and resolve common problems.
- Application Notes — Insert the two Application Notes, Memory Chart and Programming 8-bit Devices for 16-bit and 32-bit Target Applications, behind the Application Notes divider tab in your *UniSite User Manual.*

Installing Your New Software

Refer to pages 5-43 through 5-47 of the *UniSite User Manual* for instructions on installing your new version of system software.

1 Getting Started

Introduction

This section provides a description of UniSite's controls and indicators and all installation procedures for your UniSite. Use this part of the manual as a general guide to UniSite's operation. For further information on using UniSite in actual programming situations, see Sample Sessions and see the Commands section for detailed information on all of UniSite's commands.

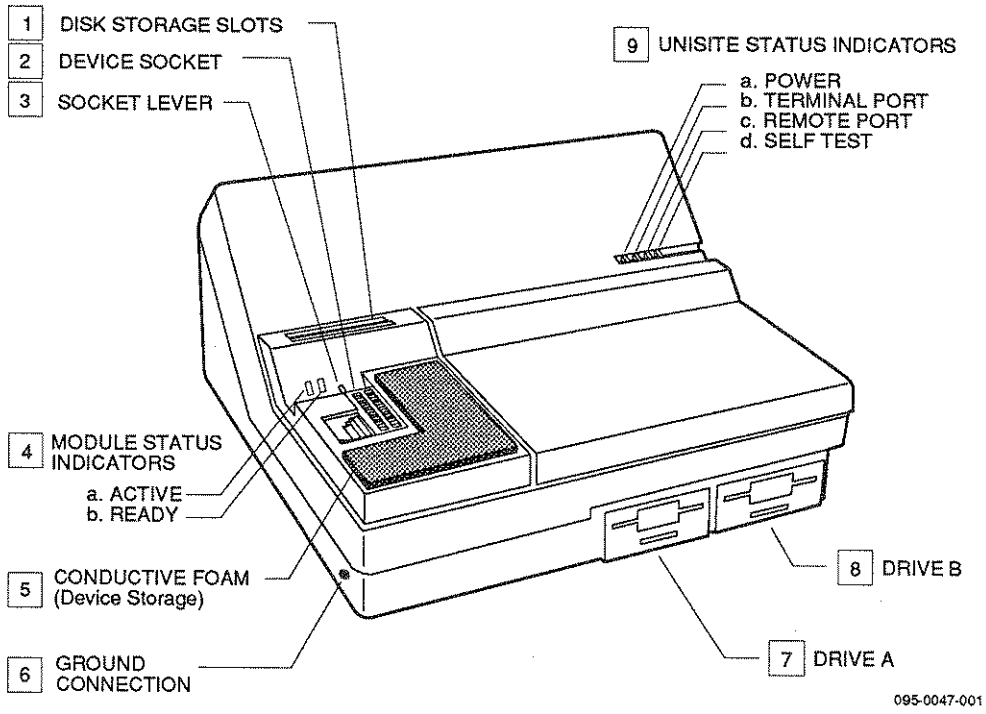
This section is divided into the following subsections:

- **Front and Rear Panel Features** — Illustrates and describes the details of UniSite's exterior.
- **Installation Procedures** — Describes connecting UniSite to a terminal or host computer, installing the modules, connecting AC power, installing the software, powering up UniSite, and configuring the serial ports.
- **Guide to Operations** — Describes the MAIN MENU format, methods for controlling the cursor, selecting commands, and using key functions. Also included are procedures for changing both the operation voltage and the line fuse.

Front and Rear Panel Features

UniSite's front and rear panel features are shown in Figure 1-1 and are described in this subsection. Each callout has a number next to it. To find out more information about a certain numbered item, read the accompanying numbered descriptions on the following pages.

Figure 1-1
Front Panel Features



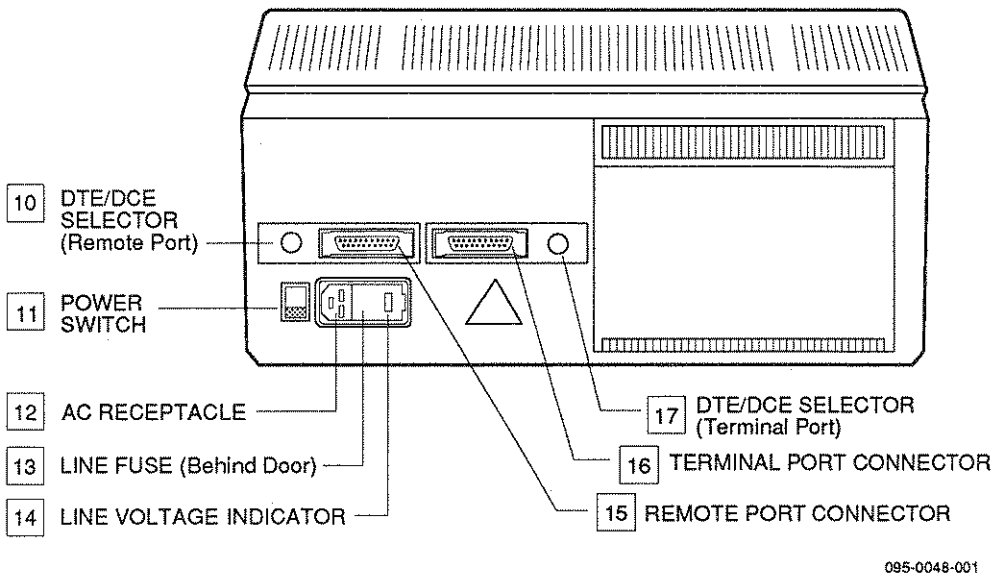
1. **Disk Storage Slots** — These slots provide a convenient place to store two data disks.
2. **Device Socket** — Holds the device to be programmed or the master device to be read.
3. **Socket Lever** — Locks the device into the device socket. To insert a device, place the lever in the upright position, insert the device and push the lever down to lock the device in the socket.
4. **Module Status Indicators** — Provides information about the module's operational status.
   a. **ACTIVE Indicator** — Lights when a device-related operation is in progress. When the ACTIVE indicator is illuminated, do not remove the module or insert/remove a device.
   b. **READY Indicator** — Lights when the device socket is ready to accept a device.
5. **Conductive Foam** — Provides a convenient spot to place devices while using UniSite. The conductive foam is safe for static-sensitive devices.
6. **Ground Connection** — Used to connect an anti-static wrist-strap.

WARNING: *An anti-static wrist strap connected here MUST contain a 1MΩ(min) to 10MΩ(max) isolating resistor, to meet safety standards.*

7. **Drive A** — This is the main disk drive. The System disk must be inserted into this drive before UniSite is powered up (see step 3 in Installation Procedures, later in this section). If you have a single-drive UniSite, you will need to insert the Algorithm disk here when you are selecting a device.
8. **Drive B** — This is the second disk drive. Drive B may be used to read the Algorithm disk, or as a convenient, faster way to duplicate disks.
9. **UniSite Status Indicators** — These indicators provide information about UniSite's operational status:
   a. **Power indicator**—This indicator lights when the power switch (see description 11) is in the "ON" position and the AC line cable is connected.
   b. **Terminal Port indicator**—This indicator lights when the terminal port on the rear panel is properly connected to the terminal. (See the "configure terminal port" procedure, later in this section.) If not illuminated, either the port is not properly connected or the DTE/DCE switch is set wrong.
   c. **Remote Port indicator**—This indicator lights when the Remote port on the rear panel is properly connected to the remote computer. (See the "configure terminal port" procedure, later in this section.) If this indicator does NOT illuminate, either the port is not connected or the DTE/DCE switch is set incorrectly.
   d. **Self-test indicator**—This indicator lights when UniSite is performing its self test. When the self test is complete, the indicator will go out.

UniSite's rear panel features are shown in the following illustration.

Figure 1-2
Rear Panel Features



10. **Remote Port DTE/DCE Selector** — Configures the remote port either as DTE (Data Terminal Equipment) or DCE (Data Communication Equipment). (See the "configure terminal port" procedure, later in this section.)

11. **Power Switch** — Powers up UniSite when the AC power cable is connected. (See the Power Up installation procedure later in this section.)

12. **AC Receptacle** — Connects the AC power cable.

13. **Line Fuse** — Houses the line fuse, providing AC overcurrent protection. To check or change the fuse, see the Fuse Replacement subsection.

14. **Line Voltage Indicator** — Shows UniSite's operating voltage. The voltage may be changed by following the instructions later in this section.

15. **Remote Port Connector** — Used to connect UniSite to either a host or remote computer. If you are using version 2.8 or later software, this port may be connected to a terminal to control UniSite, instead of using the Terminal port for this function. This is a 25-pin "D" type RS-232C serial port.

16. **Terminal Port Connector** — Used to connect UniSite to an ASCII terminal. This is a 25-pin "D" type RS-232C serial port.

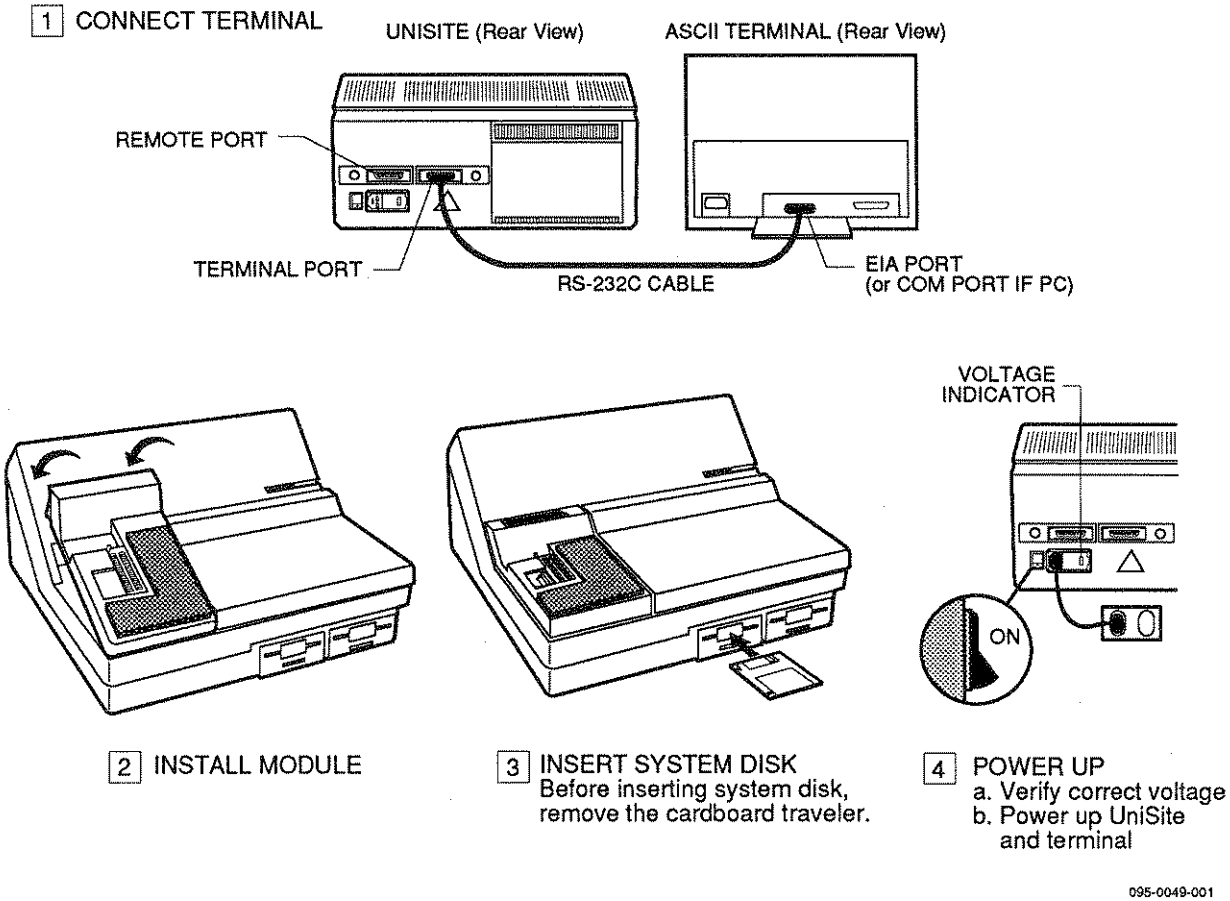
17. **Terminal Port DTE/DCE Selector** — Configures the terminal port as DTE (Data Terminal Equipment) or as DCE (Data Communication Equipment). (See the installation procedure in the "Configure Terminal Port" subsection later in this section.)

Installation Procedures

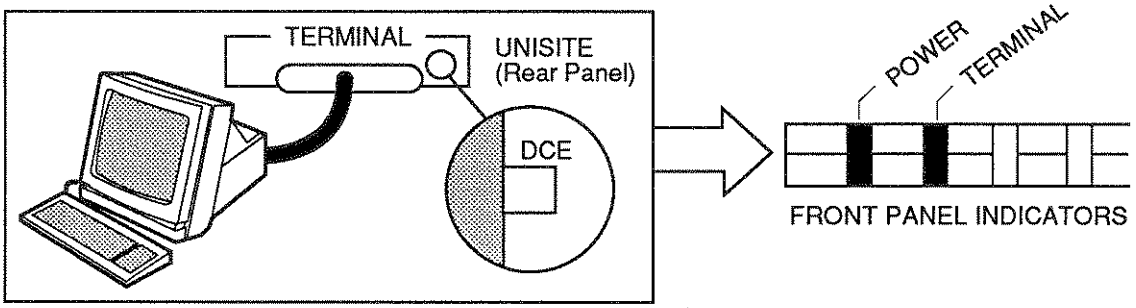
This subsection explains how to power up and operate UniSite.

The illustrations below and on the next page are to be used as a quick reference guide to all of the steps necessary to get UniSite operating. Numbers next to each drawing correspond to detailed descriptions on the pages that follow.

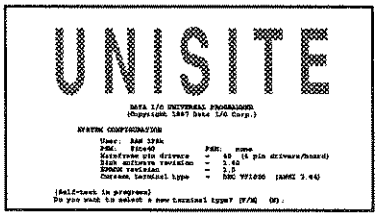
Figure 1-3
Installation Procedures



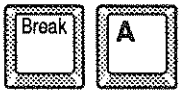
5 CONFIGURE TERMINAL PORT



6 POWER ON SCREEN



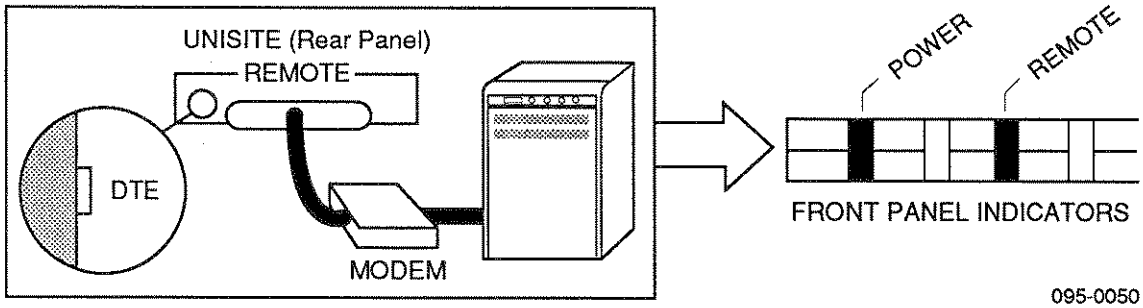
If the screen is blank or shows random characters, press



This initiates the Auto Baud feature.

When Auto Baud selects the correct baud rate, the Terminal Selection Screen will appear.

7 CONFIGURE REMOTE PORT



095-0050

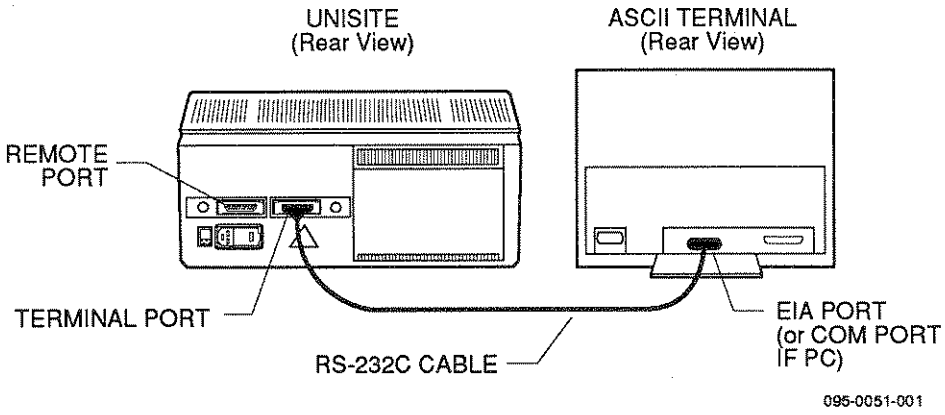
Note: If using a PC instead of a terminal, connect the cable to a COM port (COM1 OR COM2) on the PC. If running HiTerm on the PC, refer to Sample Session Five for instructions on how to use HiTerm.

1. Connect Terminal

UniSite is connected to an ASCII terminal via the RS-232C cable that is provided with UniSite. An IBM compatible personal computer running a VT-100 terminal emulation program (such as Data I/O's HiTerm) can be used instead of a terminal. UniSite is designed to be used with a terminal that has a 25-pin "D" type connector. If your terminal's 25-pin "D" type connector does not match correctly with the connector on the UniSite RS-232C cable, you will need to use the gender changer that is included with UniSite.

1. Connect the EIA or Modem connector on the back of the terminal to UniSite's terminal connector using the RS-232C cable, as shown in the following illustration.

Figure 1-4
Terminal Connection



Compatible Terminals List

The following is a list of terminals that have been tested with UniSite and which are completely supported.

- IBM PC (TERM-100 or VTERM terminal emulation software)
- WYSE WY-30, WY-50 (WY-30 emulation mode), WY-75 (VT100 emulation mode)
- WYSE WY-60 (TVI 910 emulation mode)
- DEC VT100, 101, 220, 320 (VT100 emulation mode)
- Qume QVT 101, 102 (QVT 101 emulation mode), QTV 103 (VT100 emulation mode)
- VDS DP-920 (WY-30 emulation mode)
- Televideo 910, 905 (910 emulation mode), P1000 (VT100 emulation mode)
- Televideo 9220 (VT100 emulation mode)

2. Install Module

A number of socket modules are available with UniSite. The modules available at the time of the printing of this manual are listed below. For a current list of all available modules, contact your sales representative.

- **Site 48** — Fits in the smaller module (PSM) receptacle and allows you to program, test and verify any device available in a DIP (dual, in-line package), with up to 48 pins.
- **PinSite** — This programming module allows you to program all surface mount package type devices including SOIC, LCC, PLCC; Pin Grid Array (PGA) devices and any device with up to 84 pins, expandable to 188 pins.
- **SetSite** — Also fits in the larger module (FSM) receptacle (the right-hand side) and allows you to program eight MOS memory devices at once. SetSite's sockets are designed to hold DIP devices of 40 pins or less.
- **HandlerSite** — This is a handler interface system that allows the UniSite to interface to several different handlers. HandlerSite is a PC-based system that allows a user to operate the UniSite and handler system from a PC, using powerful HANDLERlink software.
- **ChipSite** — Fits in the larger module (FSM) receptacle (the right-hand side) and allows you to support devices available in a PLCC (Plastic Leaded Chip Carrier), LCC (Leadless Chip Carrier) package with up to 68 pins, or an SOIC (Small Outline Integrated Circuit) with up to 28 pins. (This module is no longer available. PLCC/LCC, SOIC support is now provided by the PinSite module.)

UniSite is designed to accept two modules, a small one on the left and a large one on the right. Each module allows you to support devices of a specific package style, or support special types of programming operations such as set/gang programming. The installation of large and small modules are similar, so only the installation of the small module is shown in the illustrations (although the installation of both is explained in the text).

When you receive your UniSite, a dummy FSM (large module) may be installed. You must remove the top cover, remove the dummy FSM, which is held on by two screws, and replace the top cover before installing other FSMs.

Top Cover Removal

WARNING: *To avoid electrical shock, disconnect the power cord before removing the top cover. Do not reconnect the power cord until the top cover has been reinstalled.*

1. Place the UniSite onto an anti-static workstation. You should also place the disassembly tools onto this workstation.
2. Turn off UniSite's power switch.
3. Remove any front panel PSM modules (small) that may be installed.
4. Remove the power cord from UniSite's back panel.
5. Using the screwdriver, remove the top cover screws (see figure).
6. Remove the top cover by first sliding it toward the front (about 1/4"), then lifting the cover straight up.
7. Turn the top cover over and remove the two screws that attach the dummy FSM to the cover.
8. Replace the top cover on the UniSite.

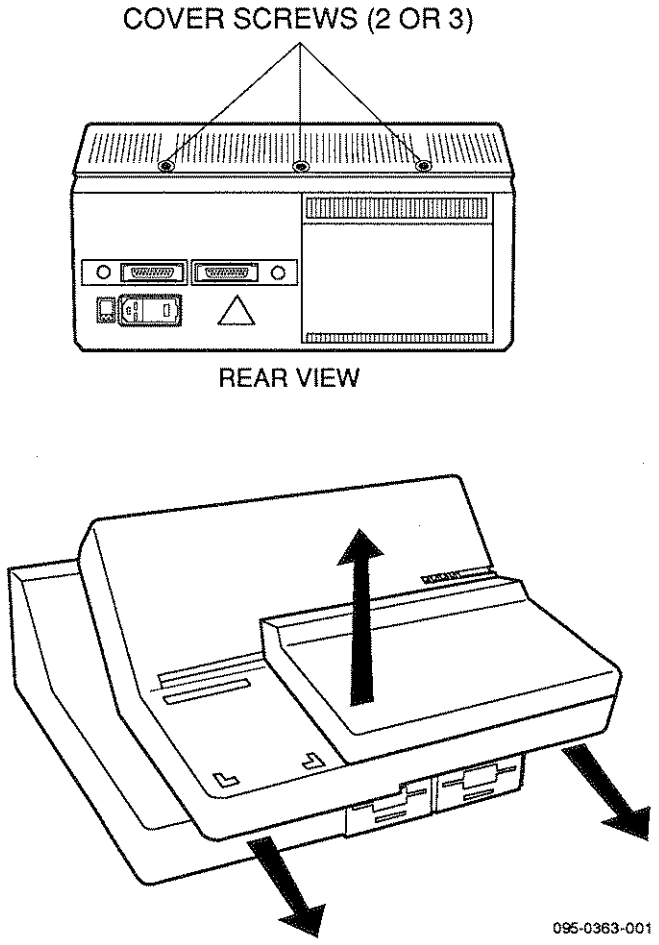
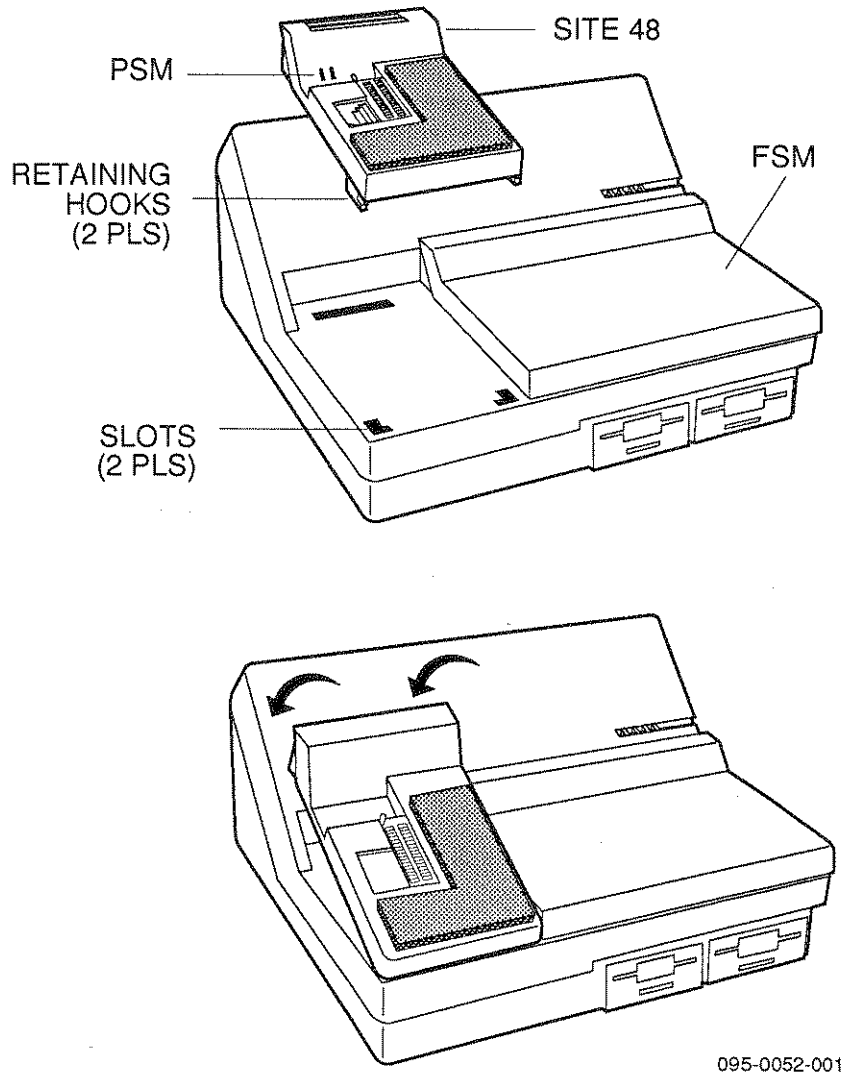


Figure 1-5
Top Cover Removal

Module Installation

1. If you are installing the small module, insert the two retaining hooks on the bottom of the module into the two left slots on the top of the UniSite base unit (see illustration). If you are installing one of the large modules, insert the two retainer hooks on the bottom of the module into the two right slots on the top of the UniSite base unit.
2. Slowly lower the back of the module until the module connector touches its mating connector on top of UniSite.
3. To ensure complete contact, firmly press down on the rear of the module.
4. To remove the module, lift the rear of the module until the retaining hooks on the front of the module are disengaged from the slots on the top of UniSite.

Figure 1-6
Module Installation



3. Insert System Disk

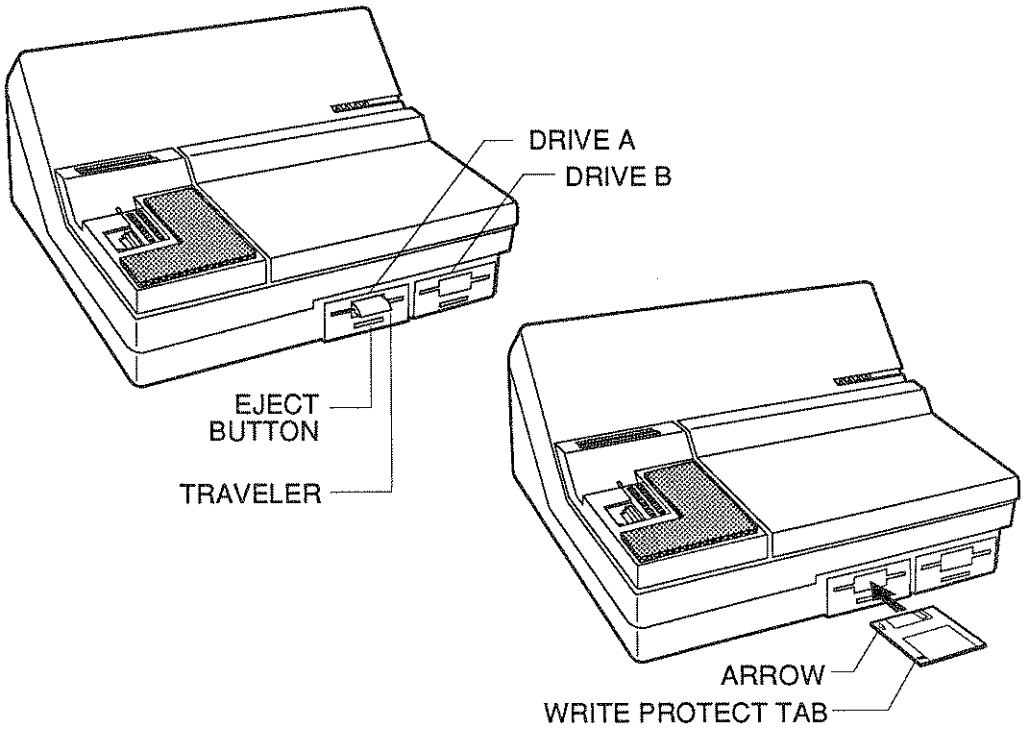
IMPORTANT: Before inserting the disk, read the licensing agreement that is printed on the software package. If you do not agree with the terms of the licensing agreement, do not open the package. You may return UniSite and its unopened software package for a full refund. Opening the package indicates that you have accepted the terms of the agreement. Data I/O will not make refunds for opened software packages.

1. After you read, understand, and accept the terms of the agreement, open the package and remove the disks. Discard the package. Fill out, sign, and send in the Warranty Registration/License Agreement card located in this manual. After registering with Data I/O, you will receive information about all future UniSite updates.

Note: Please complete the (pre-paid postage) card; we must receive this card before Data I/O can send you any software updates.

2. Remove the cardboard traveler from drive A and drive B (see the following illustration).

Figure 1-7
System Disk Insertion



3. Insert the System disk into drive A (the drive on the left). When inserting a UniSite disk, make sure that the arrow molded into the disk's plastic case is on the top and is pointing toward UniSite, as shown in the following illustration. Push the disk straight into the drive until the disk drops down and the eject button pops out.

Note: Do not attempt to use the System disk with more than one UniSite. Each disk is configured to work only with one particular UniSite. You can, however, make backup copies of the System disk.

UniSite's Algorithm disk contains copies of all the currently supported device algorithms. This disk must be installed each time you select a device. If you have a single-drive UniSite, a screen prompt will appear at the point in the select device procedure where you need to insert the Algorithm disk. If you have a two-drive UniSite, insert the System disk in drive A and the Algorithm disk in drive B.

Software Version Compatibility

The UniSite system and algorithm diskettes contain separate version numbers for their contents. UniSite will check the version numbers of the two diskettes and inform the user if the two diskettes are not compatible with each other. Although the diskettes must be compatible, their version numbers don't have to match exactly. The version numbers are considered compatible if they meet the following rules:

1. Digits to the left of the decimal point must match exactly.
2. The first digit to the right of the decimal point must match exactly. (Any additional digits, if present, don't have to match.)

For example:

System Version	Algorithm Version	Compatible?
2.50	2.50	Yes
2.51	2.50	Yes
2.50	2.51	Yes
2.50	2.40	No

This version control system allows the algorithm diskette to be updated without requiring a new system diskette.

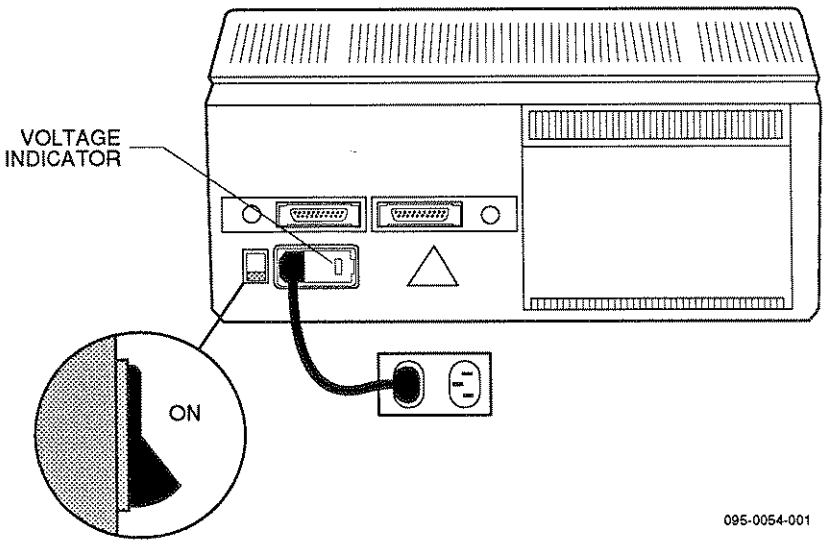
4. Power Up

1. Verify that the operating voltage is correct by checking the operating voltage indicator on the rear panel (see the following illustration). If the operating voltage is not correct, see the subsection Changing the Operating Voltage for instructions.

*CAUTION: **Damage to the equipment may occur if the instrument is operated with the wrong voltage.***

2. Connect one end of the AC line cord to the AC receptacle on UniSite's rear panel and the other end to a properly grounded AC outlet.

Figure 1-8
UniSite's Rear Panel



3. Power up the ASCII terminal.

WARNING: *To avoid electrical shock hazard, connect UniSite only to a properly grounded AC outlet.*

4. Power up UniSite.

UniSite has completed power up when the self-test LED and disk drive LED are off. The self-test indicator will go off in about two minutes. Do not remove the disk(s) or change the modules while the indicators are lit.

The four front panel LEDs illuminate in different patterns. In general, if one or more front panel indicators is blinking after the self test, there may be a faulty circuit board in UniSite. Contact your nearest Data I/O Service Center and arrange to send the unit in for servicing. The following table shows the LED combinations you should be concerned with.

Indicator				
Power	Terminal	Remote	Self-Test	Description
Off	n/a	n/a	n/a	Power supply off, or no 5V supply.
On	Blinking	Off	On	Bad CPU, EPROM, U50 or power-fail defect.
On	Off	Blinking	On	Bad system RAM (locations 80000-FFFFF).
On	Blinking	Blinking	On	Bad serial port DUART (68681).
On	Off	Off	On	Performing self-test

5. If the Power On screen is displayed on the terminal after power is applied, proceed to the Guide to Operations subsection. If the Power On screen is not displayed, your terminal may not be communicating properly with UniSite: go to the next step, Configure Terminal Port.

5. Configure Terminal Port

Before communication between UniSite and the terminal can be established, three requirements must be met:

- UniSite's terminal port must be configured using the DCE/DTE button so that it is compatible with your terminal.
- UniSite's serial I/O parameters must match the terminal's setup.
- UniSite must recognize the type of terminal that you are using. (Selecting the correct terminal type is described in the next step, Power On screen.)

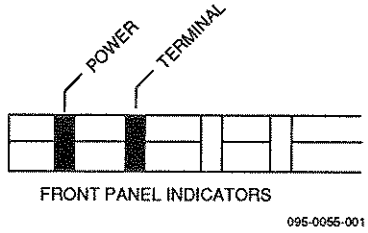
UniSite's SmartPort and autobaud features help you establish communications with the terminal quickly and easily by performing the following functions:

- Detecting a disconnected cable.
- Automatically detecting and matching the terminal's baud rate.
- Detecting the presence of Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) at the other end of the interconnection cable. An indicator lights when the instruments are configured correctly.

Note: Refer to the Computer Remote Control (CRC) section for the conditions that determine the automatic selection of terminal or CRC modes upon power up.

1. After you have powered up UniSite and the Self-Test indicator has gone out, observe the Terminal Indicator on the front panel.

Figure 1-9
Front Panel Indicators



a. If the Terminal indicator is lit, UniSite's terminal port is configured correctly.

b. If the Terminal indicator is not lit, press the button next to the terminal port on the rear panel of UniSite once. The button next to the port is a two-position switch; pressed in, the UniSite acts as Data Terminal Equipment (DTE); the "out" position configures the port as Data Communications Equipment (DCE).

2. If the Power On screen is displayed, proceed to step 6 to select the correct terminal type.

   a. If the Power On screen does not appear on the terminal at this time, one or more of the serial port communication parameters may not be set correctly on the terminal.

      Ensure that the terminal parameters match the UniSite factory default settings shown on the next page. UniSite has the capability to automatically adjust the baud rate of the terminal port to match the terminal's baud rate through the use of the auto baud feature.

      To use the auto baud feature, make sure that all of the communication parameters shown in the table match the terminal settings with the exception of the baud rate value. Next, press the [Break] key and then type [A]. UniSite will now adjust the baud rate to match that of the terminal, and the Power On screen should appear.

   b. At this point you are being prompted to select the terminal type. Type [Y] to select a new terminal type or press [↵] to go to the MAIN MENU.

UniSite's factory default serial I/O parameter settings for the terminal port are listed below:

Parameter	Factory Default Setting
Baud Rate	9600
Parity	none
Number of Data Bits	8
Number of Stop Bits	1
Communication Mode	full duplex
Handshake	CTS/DTR

Note: CTS/DTR (Hardware Handshake) is enabled as default, however, if those signals (CTS/DTR) on the terminal aren't connected, UniSite will sense this and still communicate properly using XON/XOFF (Software Handshake). XON/XOFF is always utilized by UniSite regardless of whether CTS/DTR handshake is enabled.

Note: Refer to the CRC section, Entering CRC Mode, for UniSite's Terminal and Remote port power up conditions and how to specify them.

6. Power On Screen

Observe the current terminal type displayed on the Power On screen.

1. If the current terminal type shown is the correct terminal type, press [↵] to go to the MAIN MENU.

Note: If random characters or nothing appears on the screen after pressing RETURN, the terminal port configuration is incorrect. Restart the system by cycling power. Then return to the second step in the "Configure Terminal Port" procedure.

2. If the current terminal type shown does not match the type of terminal connected to UniSite, type [Y][↵] to go to the terminal selection screen. The terminal selection screen displays the terminal types currently supported by UniSite.
3. Select the terminal type that matches your terminal by typing in the number corresponding to your terminal. Press [↵] if you do not see your terminal listed on the screen and do not know what terminal type(s) it can be operated as, refer to the Compatible Terminals list shown previously in this manual.
4. When you have selected the correct terminal type, you will be prompted to save the terminal type as power-on default by entering a Y or N. If you do not want the terminal type you selected to be saved as the default, press [↵] and the MAIN MENU will appear, indicating that UniSite is ready for operation. If you want to save the new terminal type as default, type [Y][↵] .

7. Configure Remote Port

Before communication between UniSite and a host computer can be established, the following requirements must be met:

- UniSite's remote port must be configured so that it is compatible with your host. Use UniSite's Serial Port Configuration screen to set the parameters.

Note: If the Remote port will be connected to a terminal, make sure the Serial Port parameters for the Remote port match those of the terminal you are using.

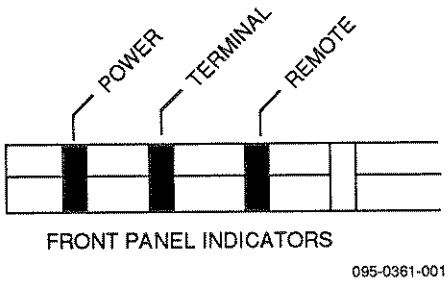
UniSite's SmartPort feature helps you establish communications with the host quickly and easily by performing the following functions:

- Detecting a disconnected cable.
- Detecting the presence of Data Communications Equipment (DCE) or Data Terminal Equipment (DTE) at the other end of the interconnection cable. An indicator lights when the instruments are configured correctly.

Note: Refer to the Computer Remote Control (CRC) section for the conditions that determine the automatic selection of terminal or remote modes upon power up.

1. After you have powered up UniSite and the Self Test indicator has gone out, observe the Remote Indicator on the front panel.
   a. If the Remote indicator is lit, UniSite's remote port is configured correctly.
   b. If the Remote indicator is not lit, press the button next to the remote port on the rear panel of UniSite once. The button next to the port is a two-position switch; pressed in, the UniSite acts as Data Terminal Equipment (DTE); the "out" position configures the port as Data Communications Equipment (DCE). The Indicator should now be lit.

Figure 1-10
Front Panel Indicators



UniSite's factory default serial I/O parameter settings for the remote port are listed below:

Parameter	Factory Default Setting
Baud Rate	9600
Parity	none
Number of Data Bits	8
Number of Stop Bits	1
Communication Mode	full duplex
Handshake	CTS/DTR Enabled

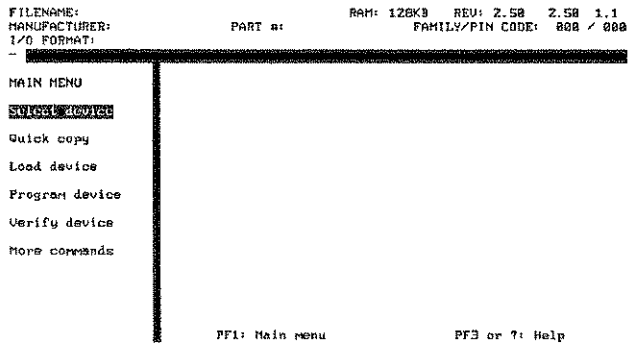
If your host computer requires different settings for these parameters, make the appropriate changes in the More commands/Configure system/Edit/Serial I/O screen on UniSite.

Guide to Operations

This subsection provides a general guide to reading the menu screens and selecting and executing commands. Included in this subsection is information that describes the screen format, how to control the cursor, how to select a command, and how to use key functions.

Screen Format

After power is applied and the self test is complete, press ↵ and the MAIN MENU will appear. From this screen, you can access any of the functions that UniSite is capable of performing.



Cursor Control

Pressing the arrow keys moves the cursor in the direction indicated on the key. When the cursor has gone as far as it can go and the key is pressed again, the cursor will "wrap around," or return to the original position.

Selecting and Executing a Command

You can select a UniSite command two ways: a) any of the commands in a menu area can be selected by moving the cursor to the desired command and pressing ↵ or b) you may select a command by typing the first letter of the command: for example, select programming by typing P (it does not matter where the cursor is).

Online Help

Online Help screens providing information about a UniSite feature selection can be displayed by pressing PF3 , F3 , or ? . To use Help, move the cursor to the area of the screen you want information on and press one of the help keys. If the selected device has specific information associated with it, a message will appear on the status line of your screen. Press PF3 F3 , or ? to access the information.

The Help screen is divided into three sections. The section at the top of the screen describes the general commands that are available when using UniSite. The middle section describes the top level state of the current menu command, and the bottom section provides more detailed information about the command or parameter currently selected by the cursor.

Online help is also available for error messages when an error message is displayed in the system message area. To use this help function, press [PF3], [?], or [F3]. The screen will be cleared and the explanation for the error message will be displayed.

Note: Online help is not available for status messages (such as `Loading device menu data` *or* `OPERATION COMLETE`*), for fatal system error messages, or if the prompt* `^Z to abort` *is appended to the error message.*

To exit the Help function, press [PF1] to return you to the MAIN MENU or [PF2] to redisplay the previous screen from which the Help function was invoked.

Using Key Functions

Some of UniSite's functions may be performed by pressing a key or a combination of keys. When using the [Ctrl] key, hold it down and then momentarily press the second key. The key functions are listed below with their corresponding keystroke sequence.

Keystroke (s)	Description
[↑]	Move the cursor up.
[↓]	Move the cursor down.
[←]	Move the cursor to the left or up.
[→]	Move the cursor to the right or down.
[PF1] or [F1]	Return to the MAIN MENU.
[PF2] or [F2]	Go to the previous menu.
[PF3] or [F3] or [?]	Display on-line help for the current operation or for error message displayed on the system message line.
[PF4] or [F4]	Displays the Optional Parameters screen.
[↵]	Execute highlighted command.
[Ctrl] – [N]	Display next page.
[Ctrl] – [P]	Display previous page or first page (works on all paging operations).
[Ctrl] – [R]	Repaint screen.

Keystroke(s)	Description
Ctrl – Z or Ctrl – C	Abort current operation being performed.
Esc Ctrl – J	Stop or start job file recording.
Esc Ctrl – T	Enter or exit the transparent mode with host computer.
Esc Ctrl – W	Restart UniSite (warm boot).
Brk – A	Execute AutoBaud detect (works only from power up screen).
First letter of a command	Execute that visible command or enter the parameter entry area command for that command

Changing the Operating Voltage

Data I/O has configured your UniSite to operate on 115Vac unless specified otherwise. The operating voltage indicator is visible through the window in the back panel door that covers the voltage selector wheel, shown in the following figure. The AC line voltage that will be used to operate UniSite must match the number indicated in the window. If the voltage you need to use is NOT the same as the number in the window, use the following procedure to change the selected voltage.

CAUTION: ***The instrument may be damaged if operated with the wrong line voltage.***

1. Disconnect the power cord.
2. Gently pry open the door that covers the voltage selector wheel with a flat-tipped screwdriver.
3. Pull the voltage selector wheel out of its slot.

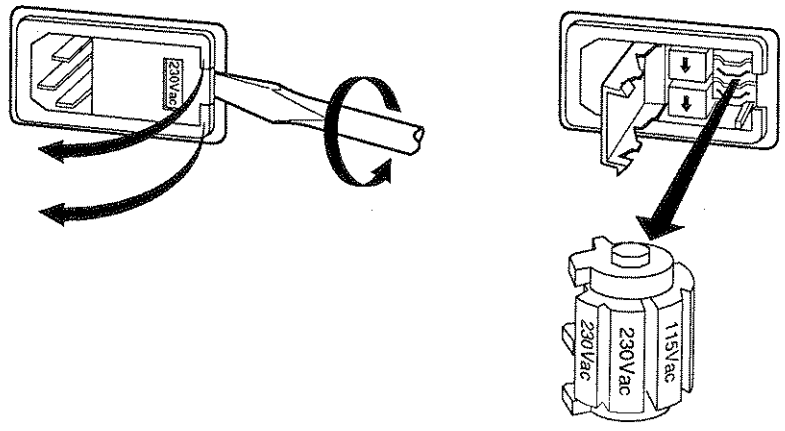


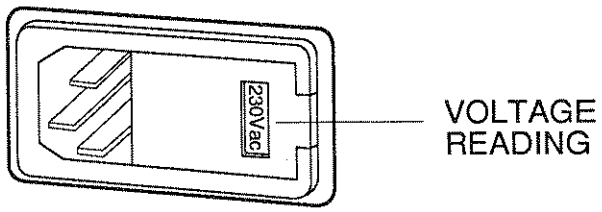
Figure 1-11
Voltage Selector Wheel Removal

4. Rotate the selector until the correct operating voltage points away from UniSite's rear panel, and then insert the selector back into its slot.

Note: The voltage wheel has two positions; 115Vac and 230Vac. These are nominal voltages -- each voltage has high and low limits. The limits for 115Vac is 90Vac to 132Vac and the limits for the 230Vac position are 180Vac to 264Vac.

5. Snap the door closed.
6. The correct voltage will now appear in the window.

Figure 1-12
Voltage Reading

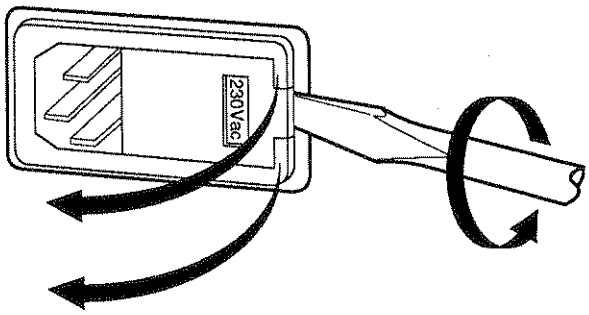


Fuse Replacement

The line fuse is located behind the same door that covers the voltage selector wheel. Perform the following procedure to replace the line fuse. In the event that the fuse is blown, replace it with one of the same size and rating.

1. Gently pry open the door that covers the fuse holder using a flat-tipped screwdriver.

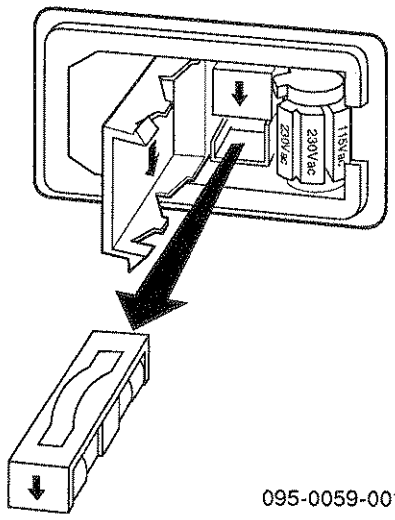
Figure 1-13
Opening the Fuse Holder



Note: The power entry module will accept two fuse cartridges. One cartridge holds domestic size fuses (1/4" x 1 1/4") and the other holds international size (5mm x 20mm) fuses. Only the bottom receptacle is connected to UniSite's circuitry.

2. Pull the bottom fuse holder out of its slot.

Figure 1-14
Removing the Fuse Holder

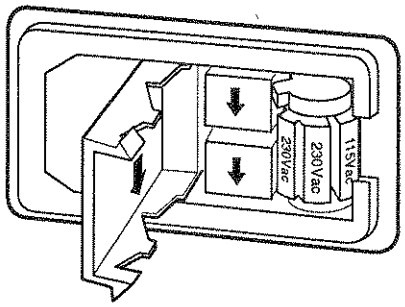


3. Check to determine whether the fuse is intact. If it is intact, proceed to Step 4. If it is blown, install a new fuse.

CAUTION: ***For continued protection against the possibility of fire, replace only with a fuse of the correct voltage, current and type ratings.***

4. Insert the fuse holder into its slot so that the arrow points in the same direction as the arrows on the door.
5. Snap the door closed.

Figure 1-15
Inserting the Fuse Holder



2 Sample Sessions

Introduction

After you have performed the Getting Started procedures and configured your system, you are ready to start programming.

This section consists of five sample programming sessions that you can use to produce programmed devices. You need to supply some blank parts and data files. Each sample session is slightly more complex than the previous one, because additional programming features are introduced with each new session.

The sessions included in this section are listed below:

- **Session One** — Programming a single memory device from a master device using terminal mode
- **Session Two** — Programming a logic device with data downloaded from a host computer
- **Session Three** — Programming a set of memory devices with data downloaded from a host computer
- **Session Four** — Programming a logic device from a host computer using remote control
- **Session Five** — Terminal emulation and file transfer using HiTerm

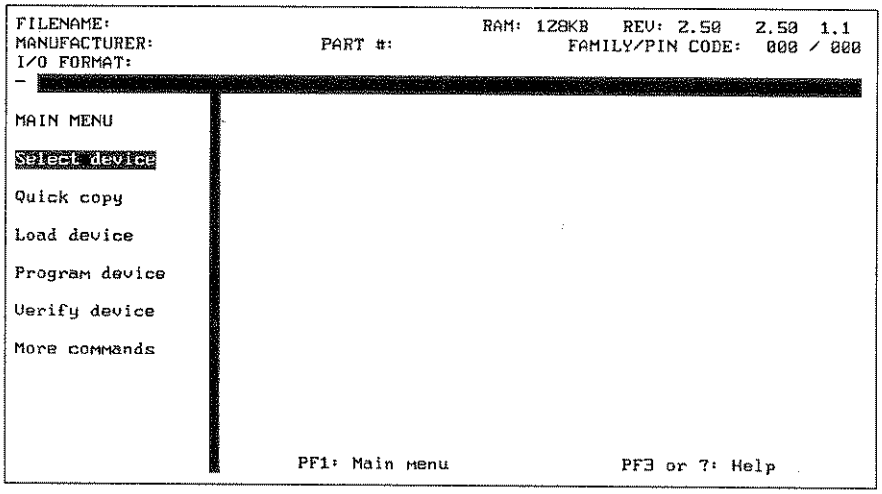
For sample sessions using Data I/O's SetSite module, refer to the SetSite manual. In the sample sessions on the following pages, a system with two disk drives is used. If you have a UniSite with a single disk drive, some variations in the procedure are required.

Session One: Program a Single Memory Device from a Master Device Using Terminal Mode

This session illustrates the programming of a single memory device from a master device (a device that is already programmed), using UniSite in terminal mode with a VT-100 type terminal. In this session you will load the program data into UniSite's RAM from a master device and then program that data into a blank device. The device used in this session is an Intel 27128 EPROM inserted into the PSM module, although you can use any EPROM supported by UniSite.

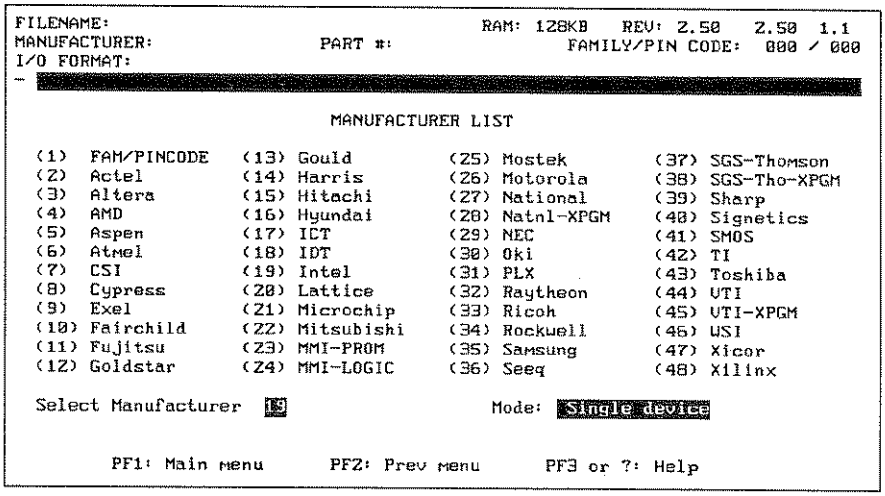
1. If UniSite is off, turn it on. The Power On screen will be displayed. Press [↵] if the current terminal type indicates the one you are using or press [Y] [↵] to select a new terminal type. The default terminal type is DEC VT100. The MAIN MENU will appear as shown in Figure 2-1 after the terminal type has been selected.

Figure 2-1
The Main Menu



2. Type [S] to choose Select device from the MAIN MENU. The MANUFACTURER LIST screen will appear as shown.

Figure 2-2
Manufacturer List Screen



Note: Since the number of supported devices changes periodically and since the Manufacturer List screens shown in this manual are examples only, you may see different manufacturers listed on your screen.

3. Move the cursor to the "Mode" field by pressing the arrow key and change the display to "Single device" by pressing the space bar once if not currently displayed. Next, move the cursor back to the "Select Manufacturer" field and select the manufacturer of the device you want to program by typing in the number that appears next to the name of the manufacturer and pressing [↵] . The screen will change as shown in the PART MENU FOR MANUFACTURER figure. For example, select Intel by typing in its line number and pressing [↵] .

Note: The PART MENU FOR MANUFACTURER screens shown in this manual are examples only. The devices shown may be different than the devices appearing on your screens since the number of supported devices changes periodically.

4. The information on the screen changes to show the device numbers of all the Intel parts that may be programmed by UniSite; if you selected a different manufacturer, the devices for that manufacturer will be displayed. Press [Ctrl] – [N] to see the next page of device numbers; [Ctrl] – [P] returns you to the previous page.

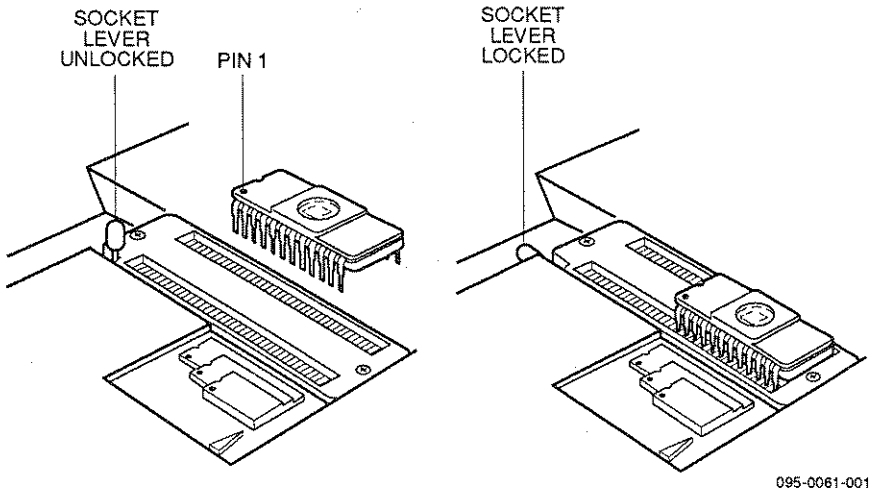
   Select a device by typing the number that appears next to the device you want to program and then pressing [↵] . For example, select the 27128 by typing in its line number and pressing [↵] . The device you selected will then be displayed in the status area at the top of your screen and the display will change to show the MAIN MENU.

Figure 2-3
Part Menu for Manufacturer Screen

```
FILENAME:                                   RAM: 128KB   REV: 2.50   2.50  1.1
MANUFACTURER:                PART #:                 FAMILY/PIN CODE:  000 / 000
I/O FORMAT:
-

      PART MENU FOR MANUFACTURER:   Intel                    Page  1 of 2

 (1)  2708          (13) 27011        (25) 27C256-PLCC    (37) 28F256P2PLCC
 (2)  2716          (14) 27128        (26) 27F256         (38) 5AC312
 (3)  2732          (15) 27128A       (27) 27512          (39) 5C031
 (4)  2732A         (16) 27128B       (28) 27512-PLCC     (40) 5C032
 (5)  2764          (17) 27C128       (29) 27513          (41) 5C060
 (6)  2764A         (18) 27C202       (30) 2815           (42) 5C060-PLCC
 (7)  27C64         (19) 27C203       (31) 2816           (43) 5C090
 (8)  27C64-PLCC    (20) 27210        (32) 2816A          (44) 5C090-PLCC
 (9)  27F64         (21) 27210-JLCC   (33) 2817A          (45) 5C121
 (10) 27010         (22) 27210-PLCC   (34) 2864A          (46) 5C180-PLCC
 (11) 27C010        (23) 27256        (35) 28F256-P1      (47) 68C257
 (12) 27C010-PLCC   (24) 27C256       (36) 28F256-P2      (48) 68C257M

 Select Part [4]

       ^N: Next page       ^P: Prev page       Return: Load Algorithm
       PF1: Main menu      PF2: Prev menu      PF3 or ?: Help
```

5. Insert the device to be copied into the device socket and lock it into place by pushing the socket lever down. Use the diagram next to the socket to verify that the device is positioned correctly (i.e., bottom-justified in the socket).

Figure 2-4
Locking and Unlocking a Device

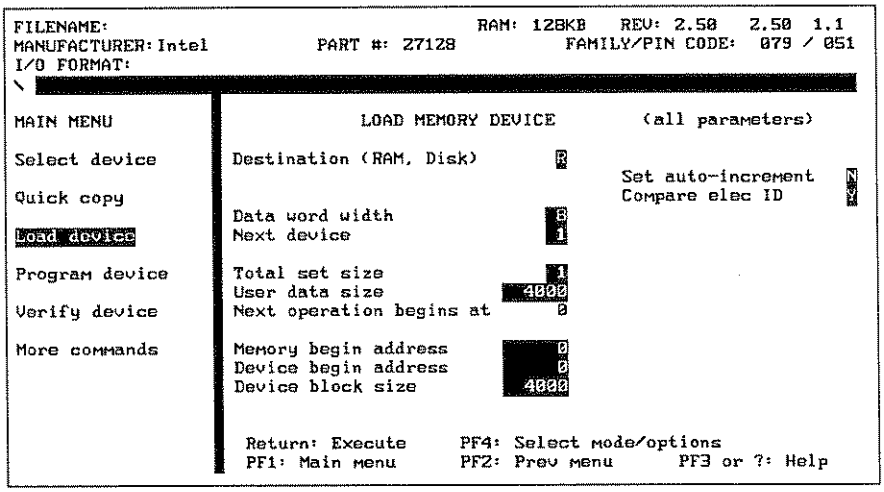


If you are programming a device in a PLCC (plastic leaded chip carrier), use the package orientation diagram next to each device socket to properly insert the device into the ChipSite module.

6. Select Load device from the MAIN MENU and then press [↵] to display the LOAD MEMORY DEVICE menu screen. If the correct screen is not shown, press [PF4] until the following screen is displayed.

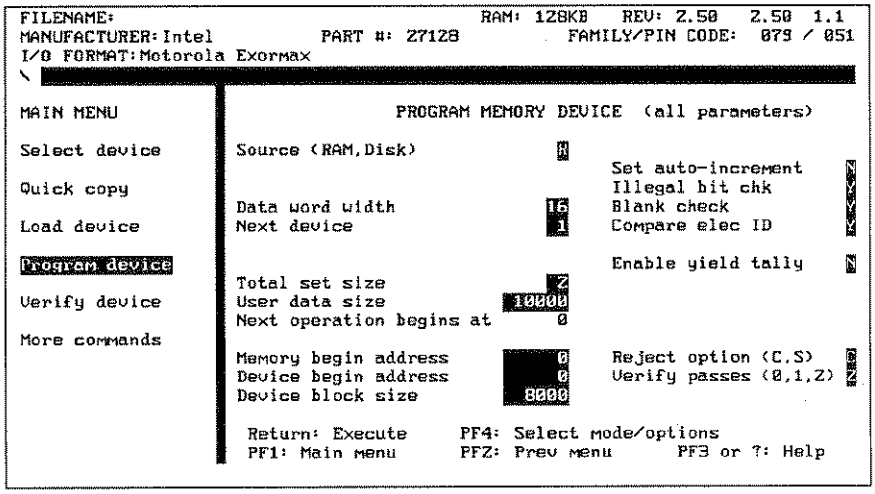
Note: Selecting Load device automatically specifies the data source as being a master device or devices.

Figure 2-5
The Load Memory Device Parameter Screen



7. Press [↵] to begin the Load device operation. In this session, you will be using default (values) for all of the Load device parameters, so you do not need to change any parameters at this point. (See the Commands section for details on selecting parameter values for this operation.)
8. When the operation is complete, a message will appear. Remove the master device from the socket by rotating the socket lever up to unlock the device. The data has now been loaded into RAM. Replace the master device with the blank device to be programmed and rotate the lever down to lock the blank device in place.
9. Press [PF1] or [PF2] and select Program device from the MAIN MENU. Then press [PF4] until the following screen appears.

Figure 2-6
The All Parameters Load Memory Screen



You do not need to enter any parameters at this point. (See the Commands section for details on selecting parameter values for this operation.)

10. Press [↵] . UniSite will begin programming your device. When the device is programmed, the following message appears.

```
OPERATION COMPLETE: Sumcheck =XXXXXXXX"
```

11. Remove the programmed device from the device socket.

12. If you want to program another device, insert that device and press [↵] .

Session Two: Program a Logic Device with Data Downloaded from a Host Computer

In this session you will instruct UniSite to download data from a host computer and to program that data into a logic device. In order to perform this session you will need a blank logic device and a data file that can be programmed into the device. You will also need to connect UniSite to the host computer containing that data file, if it is not already connected to a host. (See the Getting Started section for instructions on connecting UniSite to a host computer.)

The device used in this example is an MMI 16R8, although you can use any logic device that is supported by UniSite. A JEDEC file containing the fuse data will be downloaded from the host computer with a UNIX operating system in this sample session. If you are using a different file format or a different operating system, you will need to enter the correct parameters for your file and system instead of the parameters shown in the sample session.

1. If UniSite is off, turn it on. The Power On screen will be displayed. Press [↵] if the current terminal type indicates the one you are using or press [Y][↵] to select a new terminal type. The default terminal type is DEC VT100. The MAIN MENU will appear after the terminal type has been selected.

2. Type [S] to choose Select device from the MAIN MENU. The MANUFACTURER LIST screen will appear as shown in Figure 2-7.

Figure 2-7
Manufacturer List

```
FILENAME:                                    RAM: 128KB   REV: 2.50   2.50  1.1
MANUFACTURER:                  PART #:                FAMILY/PIN CODE:  000 / 000
I/O FORMAT:
-

                          MANUFACTURER LIST

 (1)  FAM/PINCODE   (13) Gould        (25) Mostek       (37) SGS-Thomson
 (2)  Actel         (14) Harris       (26) Motorola     (38) SGS-Tho-XPGM
 (3)  Altera        (15) Hitachi      (27) National     (39) Sharp
 (4)  AMD           (16) Hyundai      (28) Natnl-XPGM   (40) Signetics
 (5)  Aspen         (17) ICT          (29) NEC          (41) SMOS
 (6)  Atmel         (18) IDT          (30) Oki          (42) TI
 (7)  CSI           (19) Intel        (31) PLX          (43) Toshiba
 (8)  Cypress       (20) Lattice      (32) Raytheon     (44) UTI
 (9)  Exel          (21) Microchip    (33) Ricoh        (45) UTI-XPGM
 (10) Fairchild     (22) Mitsubishi   (34) Rockwell     (46) WSI
 (11) Fujitsu       (23) MMI-PROM     (35) Samsung      (47) Xicor
 (12) Goldstar      (24) MMI-LOGIC    (36) Seeq         (48) Xilinx

 Select Manufacturer 19                    Mode: Single device

        PF1: Main menu      PF2: Prev menu      PF3 or ?: Help
```

3. Select the manufacturer of the device you want to program by typing in the number that appears next to the name of the manufacturer and then pressing [↵] . When you have selected the manufacturer and pressed [↵] , the screen for selecting the part number will appear. For example, select MMI-LOGIC by typing in its item number and pressing [↵] . The first page of devices will appear. Go to the second page of devices by pressing [Ctrl] – [N] . The following screen will appear.

Figure 2-8
MMI-Logic Part Number Selection Screen

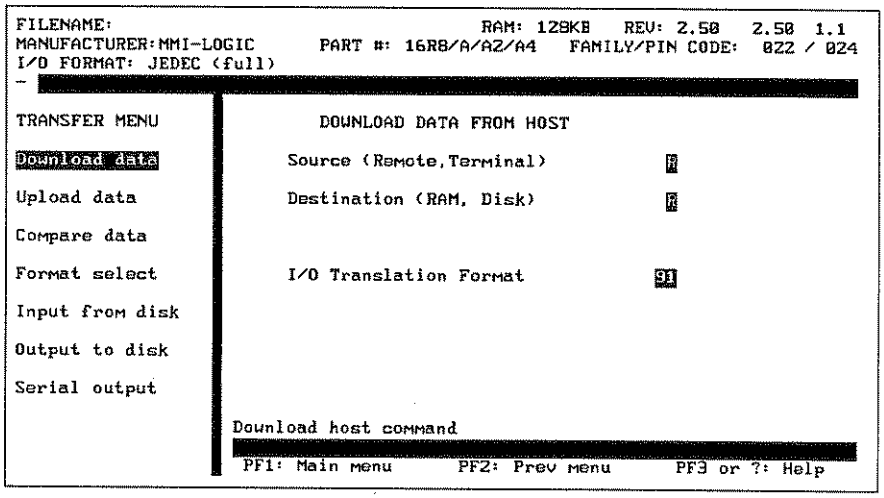
```
FILENAME:                                    RAM: 128KB   REV: 2.50   2.50  1.1
MANUFACTURER:MMI-LOGIC      PART #: 16R8/A/A2/A4   FAMILY/PIN CODE:  022 / 024
I/O FORMAT:
-

      PART MENU FOR MANUFACTURER:   MMI-LOGIC              Page  2 of 5

 (1)  16L6-NL       (13) 16P8A         (25) 16R6/A/A2/A4  (37) 16R8B/D
 (2)  16L6-SOIC     (14) 16P8A-SOIC    (26) 16R6BZ/B4     (38) 16R8/A/Z/4NL
 (3)  16L8/A/A2/A4  (15) 16R4/A/A2/A4  (27) 16R6B/D       (39) 16R8BZ/B4-NL
 (4)  16L8BZ/B4     (16) 16R4BZ/B4     (28) 16R6/A/Z/4NL  (40) 16R8B/D-NL
 (5)  16L8B/D       (17) 16R4B/D       (29) 16R6BZ/B4-NL  (41) 16R8/A/Z/4S0
 (6)  16L8/A/Z/4NL  (18) 16R4/A/Z/4NL  (30) 16R6B/D-NL    (42) 16R8BZ/B4-S0
 (7)  16L8BZ/B4-NL  (19) 16R4BZ/B4-NL  (31) 16R6/A/Z/4S0  (43) 16R8B/D-S0
 (8)  16L8B/D-NL    (20) 16R4B/D-NL    (32) 16R6BZ/B4-S0  (44) 16R8H-15
 (9)  16L8/A/Z/4S0  (21) 16R4/A/Z/4S0  (33) 16R6H-15      (45) 16RA8
 (10) 16L8BZ/B4-S0  (22) 16R4BZ/B4-S0  (34) 16R6B/D-S0    (46) 16RA8-PLCC
 (11) 16L8B/D-S0    (23) 16R4B/D-S0    (35) 16R8/A/A2/A4  (47) 16RA8-SOIC
 (12) 16L8H-15      (24) 16R4H-15      (36) 16R8BZ/B4     (48) 16RP4A

 Select Part 25

        ^N: Next page       ^P: Prev page       Return: Load Algorithm
        PF1: Main menu      PF2: Prev menu      PF3 or ?: Help
```

4. Select the device number by typing in the number that corresponds on-screen to the device you want to program; then press [↵] . You will be returned to the MAIN MENU. For example, select a 16R8 by typing in its line number and pressing [↵] .

Note: The device screens shown in this manual are examples only. The devices shown may be different than the devices appearing on your screen since the number of supported devices changes periodically.

5. Insert the device that you want to program into the device socket and lock it into place.
6. Go to the More commands/Transfer data menu by typing [M] and then [T].
7. Select Download data from the Transfer data menu. By using the arrow keys, move the cursor to each of the parameter areas and change them to the values listed below.

Figure 2-9
The Download Data From Host Screen



Parameter	Selection	Description
Source	R	Selects the port that the data will be transferred through. The remote port (R) is the default and is used in our example; this assumes that the host computer is hooked up through the remote port.
Destination	R	Selects the destination for the downloaded data. Selecting "R" instructs UniSite to store the data that is downloaded from the host computer in RAM.
I/O Format	91	The number "91" represents the I/O translation format used in this example, which is JEDEC standard for logic fuse map.
Host Command	*CAT CTRL.JED*	Directs the UNIX host to send data after it receives this command.

Note: In this sample session you will be downloading the data file to RAM, so you do not need to specify a disk filename for the data to be written to. The filename field only appears if "disk (D)" is chosen as the destination.

8. Using the arrow key, move the cursor down to the Download host command field on the DOWNLOAD DATA FROM HOST screen.

9. Select the transparent mode by pressing [Esc] and then [Ctrl] - [T] . This action will connect your terminal directly to the host system so you can set up the host for a download operation (login, change directories, etc.).

   When you have completed setting up your host computer for downloading, press [Esc] and then [Ctrl] - [T] to exit the transparent mode and return to the Download data menu.

10. Enter the appropriate command line for your host computer that will cause the download to begin, followed by the command delimiter. UniSite appends the end of the host command with a [↵] . For example, type "CAT CTRL.JED" for a UNIX system.

11. Press [↵] to execute the Download data command. The message "Transferring data" will be displayed in the message area. The host command you typed on the Download data screen will be sent to the host computer at the beginning of the download. The action symbol will begin to rotate when data transfer begins. When "Data transfer complete" appears in the message area the downloading is complete.

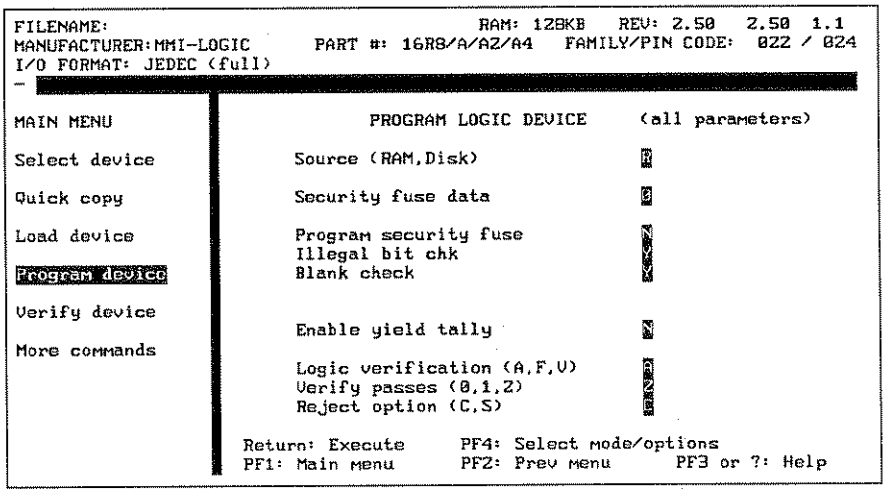
12. When downloading is complete, press [PF1] to go back to the main menu.

13. Select Program device from the MAIN MENU. Type [PF4] until the correct screen is displayed, as shown below. The factory defaults shown are the correct parameter settings for this sample session, so you do not need to enter any parameters at this point. (See the Commands section for details on selecting parameter values for this operation.)

14. Press [↵] to begin the Program device operation. When programming is complete, the message "OPERATION COMPLETE: Sumcheck=XXXX" will appear in the message area.

15. Remove the programmed device by rotating the socket lever up to unlock the device. If you wish to program another device, insert the device and press [↵] . If not, then press [PF1] to return to the MAIN MENU.

Figure 2-10
The Program Logic Device Screen

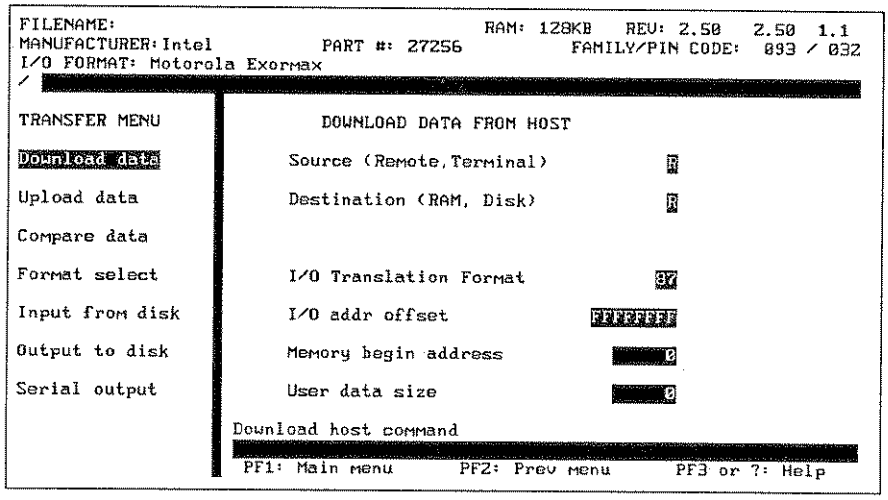


Session Three: Program a Set of Memory Devices with Data Downloaded from a Host Computer

This session illustrates how to program a set of Intel 27256 memory devices with a 16-bit data file downloaded from a UNIX system host computer. In order to perform this sample session you will need a set of blank devices and a data file that can be programmed into that set of devices. The data file must be in a format that is supported by UniSite and it must be on a host computer connected to UniSite. (See the Getting Started section of this manual for instructions on connecting UniSite to a host computer.)

1. If UniSite is off, turn it on. The Power On screen will be displayed. Press [↵] if the current terminal type indicates the one you are using or press [Y] [↵] to select a new terminal type. The default terminal type is DEC VT100. The MAIN MENU will appear as shown below after the terminal type has been selected.
2. Type [S] to choose Select device from the MAIN MENU. The MANUFACTURER LIST screen will appear.
3. Select the manufacturer of the device you want to program by typing the number that appears next to the name of the manufacturer whose device you want to program, then pressing [↵] . For example, Intel can be selected by typing in its item number and pressing [↵] .
4. Select the device you want programmed from the Part Menu screen by typing in the number next to the device and pressing [↵] . For example, select 27256 by typing in its item number and pressing [↵] . The MAIN MENU will then be displayed.
5. Go to the More commands/Transfer data menu by typing [M] and then [T] .
6. Type [D] to select the Download data menu. The following screen will appear.

Figure 2-11
The Data Download From Host Screen



7. Type in the I/O translation format number corresponding to the format of the file you are downloading. If you do not know the number of the correct I/O translation format for your file, press [PF2] and select Format Select from the Transfer menu. The Format Select screen will appear showing a list of I/O formats that UniSite supports.

   In this sample session you will use the factory defaults for all of the Download Data parameters, so you do not need to enter any parameters (other than the I/O translation format).

8. Enter the transparent mode by pressing [Esc] and then [Ctrl] – [T]. This will connect your terminal to the host system so you can set up your host computer for a transfer.

9. When you have completed setting up your host computer for downloading, exit the transparent mode and return to the Download Data menu by pressing [Esc] and then [Ctrl] – [T].

10. Move the cursor down to the host command field. Enter the appropriate command line for your host computer that will initiate the download and then press [↵]. For example, you could type **cat pgm.run**.

11. Press [↵] to execute the Download Data command. When

    ```
    Data transfer complete
    ```

    appears in the message area the downloading operation is complete.

12. When downloading is complete, press [PF1] to return to the MAIN MENU.

13. Press [P] to select the Program Device menu. When the PROGRAM MEMORY DEVICE screen appears, press [PF4] until the following screen appears.

Figure 2-12
The Program Memory Device Screen

```
FILENAME:                              RAM: 128KB   REV: Z.50   2.50  1.1
MANUFACTURER: Intel          PART #: Z7256          FAMILY/PIN CODE:  093 / 032
I/O FORMAT: Motorola Exormax
/

MAIN MENU                  PROGRAM MEMORY DEVICE  (all parameters)

Select device    Source (RAM,Disk)                 R
                                                   Set auto-increment    N
Quick copy                                         Illegal bit chk       N
                 Data word width                   Blank check           N
Load device      Next device                       Compare elec ID       N

Program device                                     Enable yield tally    N
                 Total set size                1
Verify device    User data size             8000
                 Next operation begins at      0
More commands
                 Memory begin address          0  Reject option (C,S)   C
                 Device begin address          0  Verify passes (0,1,2) 2
                 Device block size          8000

                  Return: Execute     PF4: Select mode/options
                  PF1: Main menu      PF2: Prev menu      PF3 or ?: Help
```

14. Move the cursor to the "Data word-width" field, and select 16-bit word-width by typing [1] [6] [↵].

15. UniSite will display the set size in the Total set size field: it should display a "1" (one 16-bit set). The device to be programmed is indicated in the Next device field. A "1" indicates that the first device of the set will be programmed next.

Note: Total set size defines how many virtual devices are in the set for device operations. For programming 16-bit wide data into two 8-bit wide devices, your virtual device still equals one. (One 16-bit virtual device.)

16. Move the cursor to the "Set auto-increment" field and type [Y]. Now, UniSite will automatically increment the "Next Device" when the first device has been programmed.

17. Insert the first device to be programmed into the device socket and press [↵].

18. When the programming operation is complete the following message will appear:

```
OPERATION COMPLETE: Sumcheck=XXXXXXXX
```

19. Remove the programmed device from the device socket. This becomes the first member of the set with even bytes. Then insert the next device to be programmed.

20. Press [↵] to program the next device. This device will contain the odd bytes.

21. Repeat steps 19 through 21 until all of the devices are programmed.

22. When the programming of the last device is complete, the total sumcheck is displayed for the entire set in the message area. The Next device number is also reset to 1 and UniSite is ready to program the first device of another set.

23. Press [PF1] to return to the MAIN MENU.

Note: You may also perform set programming operations using Data I/O's SetSite module, which can gang/set program eight DIP PROMs simultaneously. The SetSite manual contains sample programming procedures. Also note that the sumcheck is omitted in the Operation Complete message when performing program or verify operations on an empty socket.

Session Four: Program a Logic Device from a Host Computer Using Remote Control

This session illustrates how to use the UniSite in the remote mode to program an MMI 16L8 logic device.

1. If UniSite is off, turn it on. The Power On screen will be displayed. Press [↵] if the current terminal type indicates the one you are using or press [Y][↵] to select a new terminal type. The default terminal type is DEC VT100. The MAIN MENU will appear after the terminal type has been selected.

2. Press [M] to select More commands from the MAIN MENU.

3. Press [R] to select the Remote control mode.

4. UniSite is now in remote mode. Pressing [Ctrl] – [Z] from UniSite's terminal (or sending [Z][↵] from the remote computer) exits the remote mode and returns UniSite to Terminal mode.

Note: Remote mode can be designated as the power up default mode: Change the"Power Up CRC Mode" line on the Interface Parameters screen to Y (Yes). Then, save that parameter as a "Power Up Default" on the Save System Parameters screen.

UniSite will also power up in CRC mode if only the remote port is connected.

5. Initiate UniSite and Remote computer communication by either running PROMLink, which is available from Data I/O, or your own programmer driver program. Follow the following example in the driver program to perform the same sequence of steps as presented in Sample Session 2.

   If you are planning to develop your own driver, the steps in this session outline the commands you would send to UniSite to download data to UniSite and program a device. See the Computer Remote Control section in this manual for more details on UniSite's Computer Remote Control commands.

6. From the remote computer send **2217@** [↵] to signal the UniSite to select the correct family and pinout code for the device to be programmed. Refer to the Device List to look up the family and pinout code for different devices. UniSite will return with a > prompt.

Note: 2217 is the family and pinout code for an MMI 16L8.

7. Select the I/O translation format by sending **091A** [↵] from the remote computer. UniSite will return with a > prompt.

Note: The number "091 ", used as an example in step 7, indicates two parameters; "0" is the instrument control Code and "91" specifies the "Jedec" I/O format. A list of these codes is available in the Translation Formats section of this manual.

8. Send [I][↵] from the remote computer. Then send the data in the format selected to UniSite. At the end of data transfer, UniSite will return with a > prompt.

9. After installing a blank part, send [P][↵] . Programming of the device will start. If the programming operation was successful, UniSite will return with a > prompt.

Session Five: Terminal Emulation and File Transfer Using HiTerm

This session illustrates how to install, run and transfer files using HiTerm on an IBM PC or equivalent. For detailed information on HiTerm, refer to the PC Utilities, HiTerm User's Guide, 983-0234.

Installing HiTerm on a Hard Drive

1. Copy all the files from the HiTerm diskette to the hard disk in any subdirectory you desire.
2. Modify the AUTOEXEC.BAT file in the root directory of the hard disk so that the PATH points to the subdirectory where the HiTerm files reside (if it doesn't already point there). For more information regarding the PATH command, refer to your DOS manual.
3. Modify the PROGRAM.BAT file to reflect the location of the HiTerm files on your system. This batch file must be modified so HiTerm can find the configuration files when it is invoked. Edit the two lines which invoke HiTerm so they indicate the drive which contains the HiTerm files and also the path to the subdirectory where they reside. Refer to the following example.

Note: The bold print indicates the portion that may be modified.

PROGRAM.BAT (original file)

```
echo off
Rem: HITERM will use the configuration filename from command line if present.
If not (%1) == () HITERM %1

Rem: HITERM will use PRG9600.CFG if no configuration file is specified.
If (%1) == () HITERM PRG9600.CFG
```

PROGRAM.BAT (modified file)

```
echo off
Rem: HITERM will use the configuration filename from command line if present.
If not (%1) == () HITERM C:\UTIL\%1

Rem: HITERM will use PRG9600.CFG if no configuration file is specified.
If (%1) == () HITERM C:\UTIL\PRG9600.CFG
```

4. Installation is now complete. Reboot your computer.

Running HiTerm From a Hard Disk

After installing the HiTerm files, simply enter **PROGRAM** ↵ to start HiTerm.

When HiTerm is started, it will read the configuration file to set the operating mode to Programmer and set the various communication port parameters (baud rate, parity, etc.). In order to run HiTerm at a different baud rate, enter the appropriate configuration filename on the command line following the command 'PROGRAM'. For example:

- Entering **PROGRAM PRG19200.CFG** will invoke HiTerm using the PRG19200.CFG configuration file, which will cause HiTerm to run at 19200 baud.
- The configuration filenames and batch filenames can be changed to any legal filename, if desired, to reduce the number of keystrokes required to invoke HiTerm.
- If a configuration file is not specified after the word PROGRAM, the PROGRAM.BAT batch file will use the PRG9600.CFG file by default which will cause HiTerm to run at 9600 baud.

Transferring Files With HiTerm

A special host command named "Transfer" is used by the UniSite to communicate with HiTerm.

Only the first two characters (TR) in either upper- or lower-case are necessary, or you may type **TRANSFER**. The Transfer command should be followed by a filename and ended with a carriage return. There should be at least one space to separate the command and the filename. Extra spaces are ignored. To transfer a file between the PC and UniSite, enter the Transfer command followed by the filename on the host command line of UniSite's upload or download menus. The file will be automatically opened and closed on the PC at the appropriate times.

Upload

1. When you are in the More commands/Transfer data/Upload menu, ensure that the destination field is set to "T" for Terminal port. If you are using High Speed Mode, the destination field must be set to "R" for Remote port*.
2. In the Upload Data to Host field at the bottom of the screen, enter the following:

   transfer <filename> ↵ or alternately **tr <filename>** ↵
3. Enter another ↵ to initiate the data transfer.

Download

1. When you are in the More commands/Transfer data/Download menu, ensure that the Source field is set to the port which the PC is connected to. For High Speed mode, the Source field must be set to "R" for Remote port*

* *If you are performing a High Speed Download the User Menu Port switch must be set to (R) and the High Speed Download switch must be set to (Y) on the More commands/Configure system/Edit/Communication screen. Refer to the PC Utilities HiTerm User's Guide (983-0234) for more details. .*

2. In the Download Data from Host field at the bottom of the screen, enter the following:

   transfer <filename> ↵ or alternately **tr <filename>** ↵ .

3. Enter another ↵ to initiate the data transfer.

Recapturing the UniSite Screen

Anytime you want to repaint the UniSite screen, press Ctrl – R .

3 Commands

Introduction

This section describes all the commands that you can access from UniSite's menus. The "command tree" illustration on the following pages shows how all the menus are interrelated. All the commands in this section are organized according to their order on the command tree.

UniSite's most frequently used commands are on the Main Menu. These commands are on the first page of the command tree drawing, they are: Select device, Quick copy, Load device, Program device, Verify device, and More commands.

The commands used less often are on the More Commands menu, shown on the second and third pages of the command tree drawing. The following commands are on this menu: Configure system, Device checks, Edit data, File operations, Job file, Remote control, Self-test, Transfer data, and Yield tally. The screens associated with these commands are also shown on the command tree figure.

Special Parameter Fields

Some manufacturer's devices support special data functions such as the program signature and XNOR table. If a function does not apply to a certain device, that field won't be displayed.

Using User RAM

The following operations will utilize User RAM, overwriting any user data that may have been there.

1. Load device to disk file
2. Program device from disk file
3. Verify device from disk file
4. More commands/Device checks/Illegal bit check to disk file
5. More commands/Device checks/Underblow to disk file
6. Duplicate disk
7. Transfer/Upload from disk file
8. Transfer/Output to disk from disk file
9. Transfer/Serial output from disk file
10. Transfer/Input from disk to disk file
11. Transfer/Download data to disk file
12. Transfer/Compare data to disk file
13. Self-Test User RAM test

Factory Default Settings

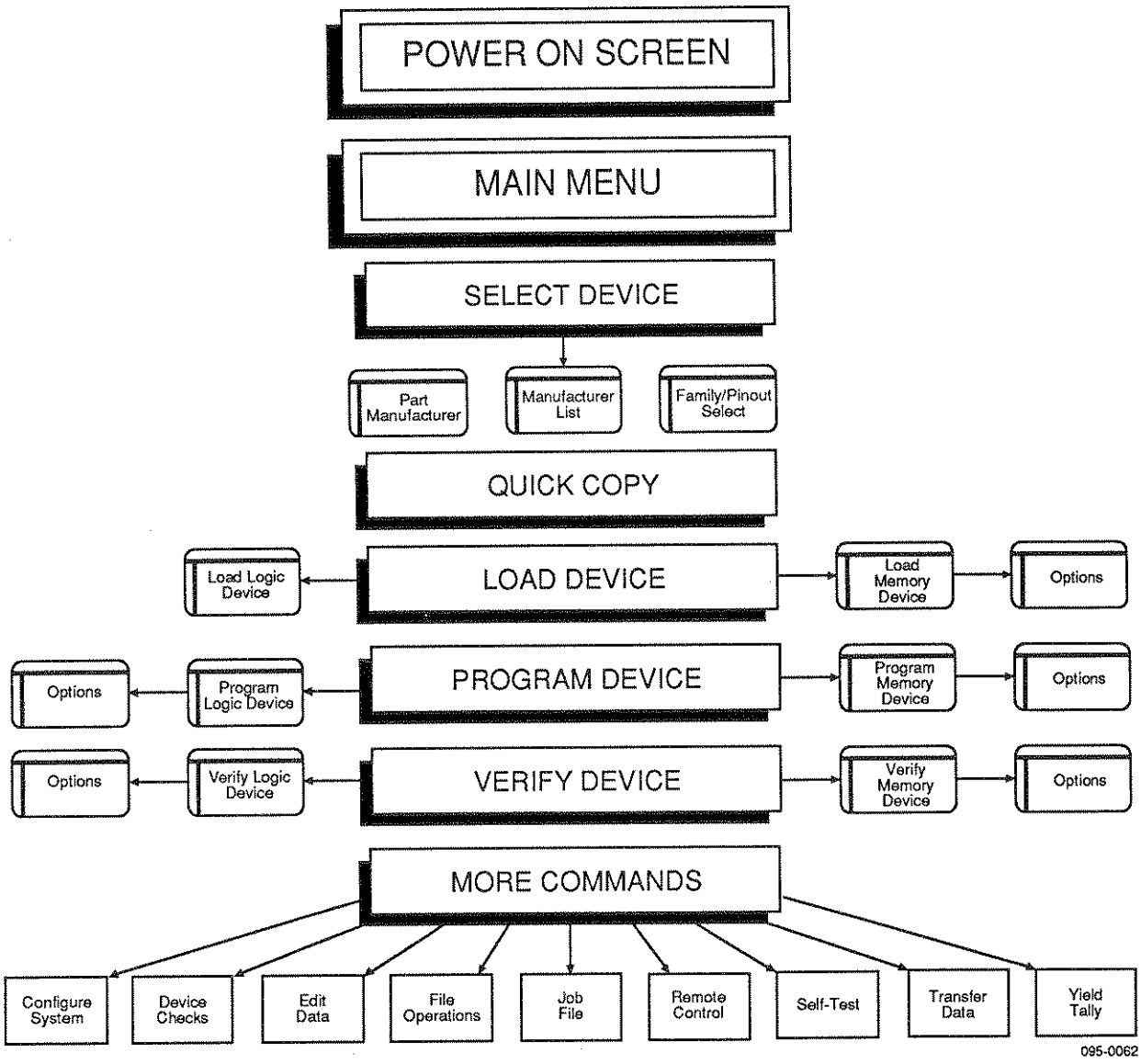
UniSite's system parameters are intitialized to certain settings at the factory. You can restore these factory defaults at any time by selecting configuration file number "0" from the More commands/Configure system/Restore menu. From the Restore System Parameters menu, press 0 ↵ to reselect the factory settings. The power up defaults (configuration file number 1) are the same as the factory defaults when the unit is shipped from Data I/O.

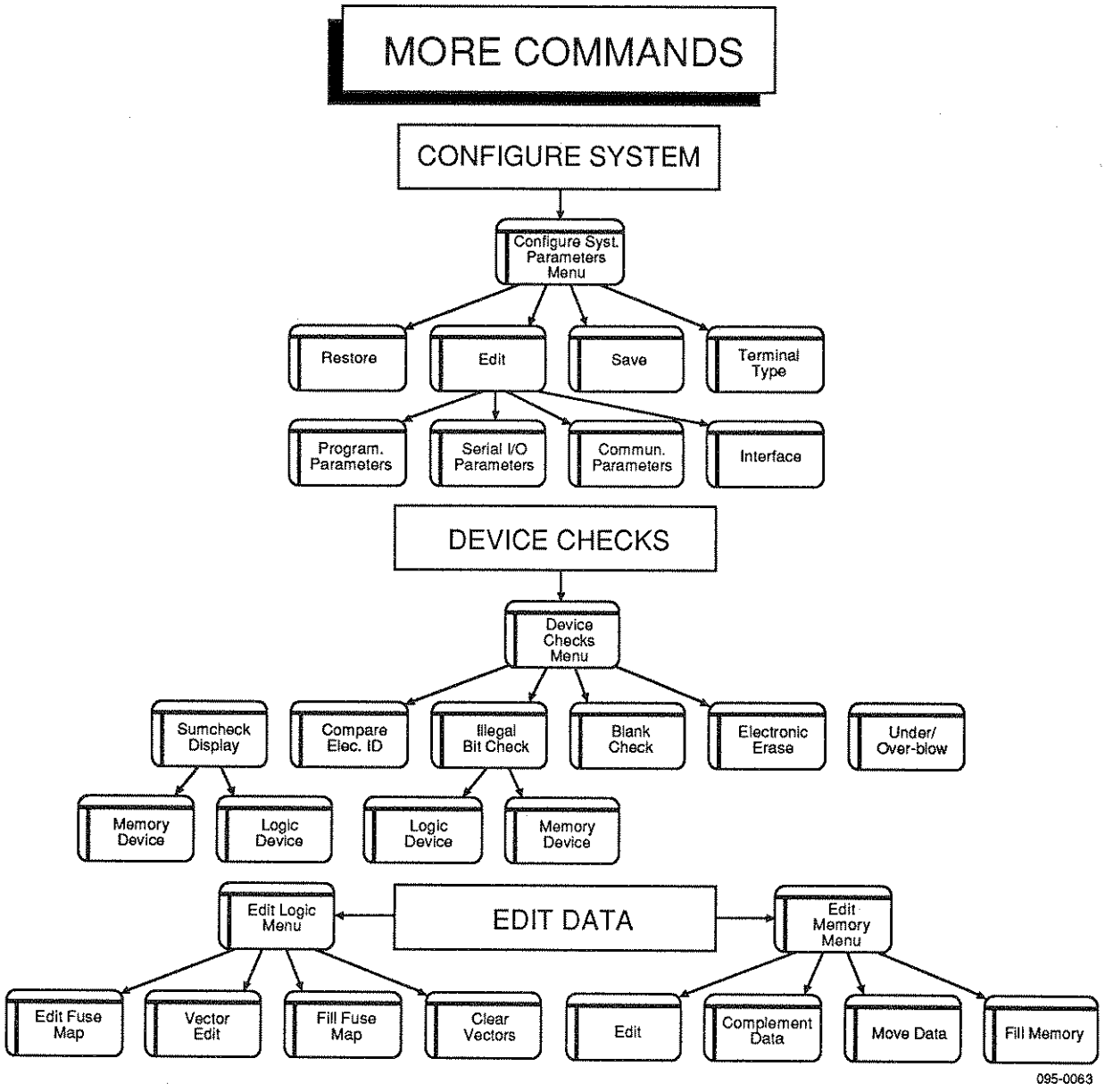
Note: Two screens are available for each device-related operation: a "simple" (non-default) and a "complex" (all parameters) screen. The simple screen is the one you see when you first enter a menu. If you press **PF4** *after entering the screen, you'll get the complex screen. However, if you've changed any of the default parameters (listed in the following table), those changed parameters will show up on the simple screen, as a reminder.*

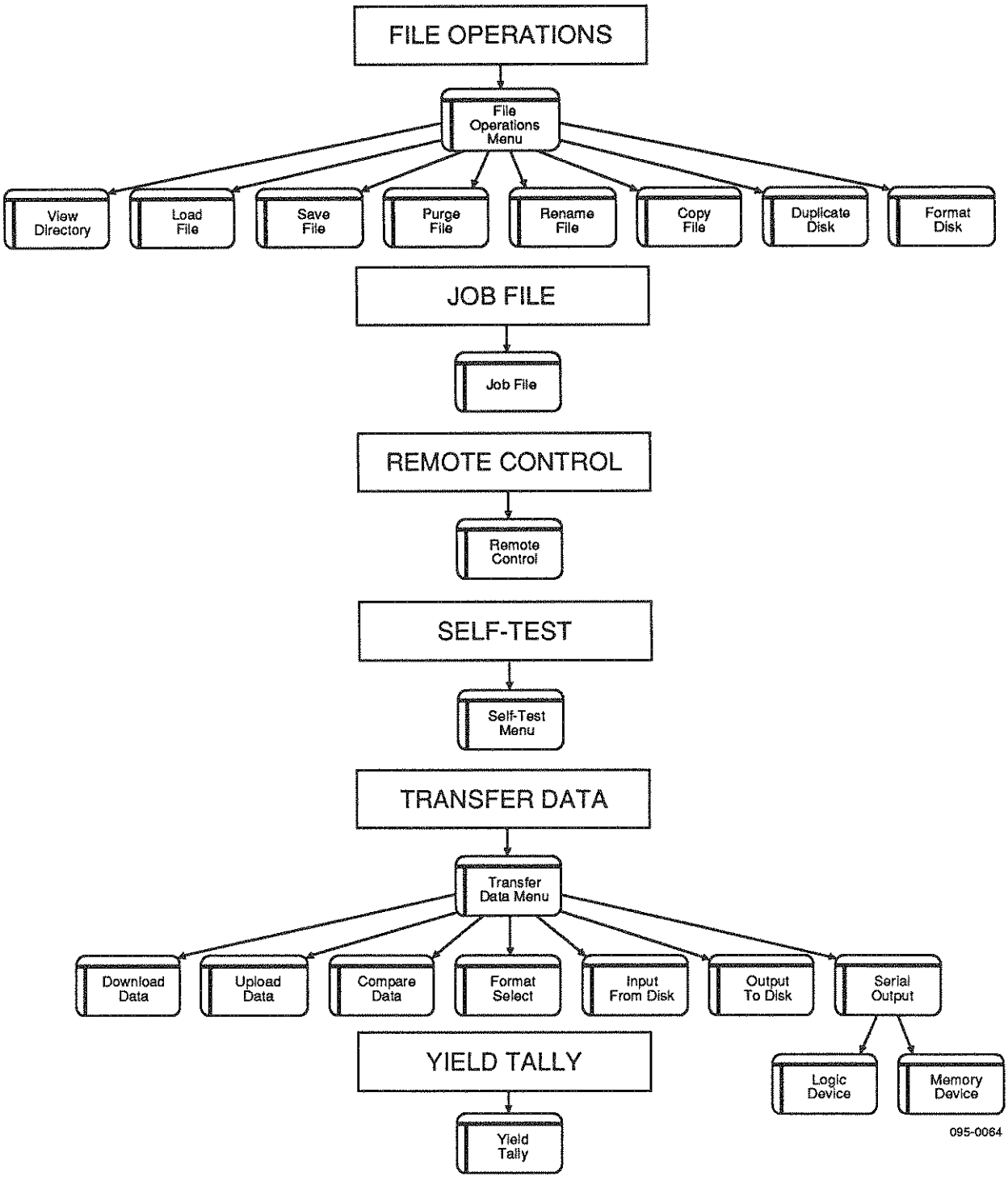
Parameter	Factory Default Setting
Blank check option	Yes
Continuity check option	Yes
Compare electronic ID	Yes,
Data source/destination	R (RAM)
Data word width	8
Device begin address	0
Device block size	1000
Enable download echo	No
Enable security fuse	No
Enable special data	No
Enable terminal beep	Yes
Enable yield tally option	No
Extended Algorithm	No
EE bulk erase option	No
EOF delimiter flag (download)	No
EOF delimiter flag (upload)	No
Family code	0 (no default)
File delimiter character (download)	1A (Ctrl Z)
File delimiter character (upload)	1A (Ctrl Z)
Filename	Blank
Fill RAM before downloading	No
Fill RAM with data (00 to FF)	00
High speed download	Yes
Host command (download)	Blank
Host command (upload)	Blank
Illegal bit check option	Yes,
Instrument control code (0, 1, 2)	0
I/O address offset	FFFFFFFF
I/O translation format	0 (no default)
I/O timeout	30 seconds
JEDEC I/O translate DIP/LCC option	Yes
Logic verification (all, fuse, vector)	A (All)
Main menu job files	No
Manufacturer	Blank (no default)

Parameter	Factory Default Setting
Memory begin address	0
Number of lines between form feeds	0
Number of nulls	0
Odd/even byte swap for 16 bit option	No
Part number	blank (no default)
Pinout code	0 (no default)
Power on CRC mode	No
Program security fuse	No
Reject option (commercial or single)	C (Commercial)
Remote Off code	0
Remote On code	0
Remote serial port configuration	9600 baud, 1 stop bit, 8 data bits, no parity, active CTS/DTR
Security fuse data (0 or 1)	0,
Serial set auto increment flag	No
Simple/complex screen in Load, Program, Verify	Simple
Single/gang/set mode	Single
Terminal serial port configuration	9600 baud, 1 stop bit, 8 data bits, no parity, active CTS/DTR,
Terminal type	VT100
Transmit pacing	0
User data size	0
User menu port*	T
Upload wait	0 seconds
Upload destination/download source	R (Remote)
Upload record size	16 (Output record size)
Verify Data Format (B, H)	H (Hex)
Verify passes (0, 1 or 2)	2

* *This parameter does not get restored when the Restore Configuration operation is performed; however it is utilized at power up time if it is saved as a power up parameter.*


POWER ON SCREEN
MAIN MENU
SELECT DEVICE
Part Manufacturer
Manufacturer List
Family/Pinout Select
QUICK COPY
Load Logic Device
LOAD DEVICE
Load Memory Device
Options
Options
Program Logic Device
PROGRAM DEVICE
Program Memory Device
Options
Options
Verify Logic Device
VERIFY DEVICE
Verify Memory Device
Options
MORE COMMANDS
Configure System
Device Checks
Edit Data
File Operations
Job File
Remote Control
Self-Test
Transfer Data
Yield Tally
095-0062


MORE COMMANDS
CONFIGURE SYSTEM
Configure Syst. Parameters Menu
Restore
Edit
Save
Terminal Type
Program. Parameters
Serial I/O Parameters
Commun. Parameters
Interface
DEVICE CHECKS
Device Checks Menu
Sumcheck Display
Compare Elec. ID
Illegal Bit Check
Blank Check
Electronic Erase
Under/ Over-blow
Memory Device
Logic Device
Logic Device
Memory Device
Edit Logic Menu
EDIT DATA
Edit Memory Menu
Edit Fuse Map
Vector Edit
Fill Fuse Map
Clear Vectors
Edit
Complement Data
Move Data
Fill Memory
095-0063


FILE OPERATIONS
File Operations Menu
View Directory
Load File
Save File
Purge File
Rename File
Copy File
Duplicate Disk
Format Disk
JOB FILE
Job File
REMOTE CONTROL
Remote Control
SELF-TEST
Self-Test Menu
TRANSFER DATA
Transfer Data Menu
Download Data
Upload Data
Compare Data
Format Select
Input From Disk
Output To Disk
Serial Output
Logic Device
Memory Device
YIELD TALLY
Yield Tally
095-0064

Select Device

Before you can perform any device-related operations with UniSite, you must first select a device using the Main Menu's Select Device command. The Select Device command is divided into two parts: Manufacturer List and Part Menu for Manufacturer. The Manufacturer List screen displays a list of device manufacturers supported by UniSite. When you select a device manufacturer from the Manufacturer List, you are then presented with a list of the devices supported by that particular manufacturer. If you select Fam/Pincode from the manufacturer list, you will go into the Family/Pinout Code selection screen. (See Family/Pinout Code Select Screen section.)

When you have selected a manufacturer and device, UniSite will return you to the Main Menu. (If the selected device has specific information associated with it, a message will appear on the status line of the screen. Press [PF3], [F3] or [?] to access help.) The device you selected will appear on the top portion of the screen, and from then on you will see only screens which pertain to that type of device. For instance, if you choose a logic device, then you will see only screens that are required to program, test, and verify a logic device.

Manufacturer List

The Manufacturer List screen displays a list of device manufacturers supported by UniSite. To select a manufacturer, type the number that appears next to the manufacturer you want.

The "Mode" field that appears to the right of the Select Manufacturer field is used to select Single device or Gang/set programming. Changing to a different mode will change the screen so that only manufacturers supported by that mode will be displayed. For example, if you change to "Gang/set" mode, only the manufacturers that have devices supported with the SetSite module will appear. This field should be set to "Single device" programming unless you are using Data I/O's SetSite module (which allows programming of up to eight DIP EPROMs or EEPROMs).

Part Menu for Manufacturer

This screen displays all of the devices made by the selected manufacturer that UniSite will support (in the selected mode). To select the device number, type the number that appears next to the device you want. Press [Ctrl] – [N] to advance to the next page of the device list and [Ctrl] – [P] to go to the previous page. After you have selected a device and pressed [↵], the Main Menu will be displayed.

Family/Pinout Code Select Screen

Family/pinout codes identify a device by its characteristics rather than its manufacturer/part number. The family code groups devices by their architecture. For example, 27128 DIP PROMs that share the same basic characteristics might have the same family code. Pinout codes identify the device by its pinout: most 16 pin devices have the same pinout code.

Family/pinout codes are listed in UniSite's device list. A new device list is shipped with each new software update.

To select a device by family/pinout codes, do the following:

1. Insert UniSite's Algorithm disk. Type in the two- or three-digit Family code corresponding on the device list to the part you want to program.
2. Move the cursor with the [→] key to the pinout code parameter.
3. Type in the two- or three-digit pinout code corresponding on the device list to the part you want to program. Press [↵] twice. If UniSite does not detect the Algorithm disk, this message will appear: "Cannot access system file. Insert algorithm disk." If this message appears, insert the Algorithm disk, press [↵] and continue with the procedure.
4. UniSite will now begin loading the algorithm. If the algorithm is found, you will be returned to the Main Menu, otherwise the message "Device algorithm not found" will appear and you will remain in the Family/Pinout Code select screen. At this point, you can get back to the Main Menu by pressing [PF1] .

Note: If you get a recurring "Device Insertion Error" with a device selected using family/pinout codes, try disabling the "Continuity check" feature. Use the More commands/Configure system/Edit/Programming parameters screen to change this option from Y to N, or if possible, use the Manufacturer List/Part Menu for Manufacturer screens for device selection instead of the family/pinout code method.

Cross Programming

Cross programming allows a single "generic" programmable logic device to be configured as any one of many PLD architectures. Consequently, the "generic" device can take on the function of many subset devices. The term "generic PLD" will be used to identify the superset device. As an example, a 16V8 generic PLD can be configured as a 16R4, 16R8, 16L8, etc.

The generic PLD and subset devices that it can support are not restricted to the same manufacturer. For example, a 16V8 generic PLD from manufacturer "A" can be programmed using a fuse pattern of a 16L8 from manufacturer "B." The cross programming feature allows the user to avoid the need to recompile source code for the generic PLD if the appropriate fuse pattern is available in a subset part.

To view the subset devices, select a manufacturer with the "XPGM" extension. This screen will show all devices that can be programmed into the generic PLD of the selected manufacturer.

Select the device of interest from the XPGM menu. This menu will list the Generic device and the subset target device, for example "16V8 AS 16L8." Once the cross program device is selected, a JEDEC file for the subset device (in this case a 16L8) can be downloaded into User RAM and programmed into the device using the normal programming procedure.

Quick Copy

UniSite's Quick Copy command allows you to load data from a master device and program another device, using only two terminal screens: Select Device and Quick copy. To use the Quick copy feature, do the following:

1. Select the device you wish to program, by selecting Select Device from the Main Menu. Continue through the manufacturer and device selection process and when the device is selected, the Main Menu screen will reappear.
2. Select the Quick Copy menu, by typing **Q**.
3. Insert the master device.
4. Press [↵] to load the master data into RAM. When the master device data has been loaded into RAM, the message "OPERATION COMPLETE. Sumcheck = xxxxxxxx Hit return" is displayed.

Note: If you are using the Quick copy function with SetSite, you must press ↵ again at this point. This allows you time to review the screen and Sumcheck information.

5. When the data has been loaded, remove the master device and press [↵] . The message "Insert blank device. Hit return" is displayed.
6. Insert the device(s) you want programmed.
7. Press [↵] to program the socketed device(s).
8. When the programming operation is completed, "OPERATION COMPLETE. Sumcheck = xxxxxxxx Hit return" will appear on UniSite's screen. Remove the programmed device(s).

Note: You may also use the Quick copy to load data for set programming, if you are using Data I/O's SetSite module. Data word width will automatically be set to device word-width.

LOAD Device

The Load Device command allows you to copy data from a socketed master device into RAM or a disk file. Depending on whether a logic or memory device has been selected, either the Load Logic Device screen or the Load Memory Device screen will appear when you select this command.

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Load Logic Device

If you select a logic device and then select the Load command, UniSite's Load Logic Device menu will appear. You may press PF4 to display options. The following parameters can be specified in the Load Logic Device screen.

- **Destination** — Specifies the destination for the fuse data that you wish to copy from the device: either RAM or disk. Select the data destination by either using the space bar or by directly typing in **R** or **D**.
- **Filename** — Specifies the name of the disk file where you want the fuse data to be written. This parameter will not appear if you have selected RAM (R) as your data destination. The Filename parameter must follow the MS-DOS convention: a specified drive, up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT".

Load Memory Device

If you select a memory device and then select the Load command, UniSite's Load Memory Device menu will appear. You may press PF4 to display available options in the Complex load screen. The following parameters can be specified in the Load Memory Device screen:

- **Destination** — Specifies the destination for the data that you wish to copy from the master device: either RAM or disk. Select the data destination by either using the space bar to toggle values or by directly typing **R** or **D**.
- **Filename** — Specifies the name of the disk file where you want the data to be stored. This parameter will not appear if you have selected RAM (R) as your data destination. The Filename parameter must follow the MS-DOS convention: an optional drive, up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:27256.DAT".
- **Data Word Width** — Sets the word width of the data to be loaded. For 8-bit (or above) devices, the minimum word width is equal to the device width, and the maximum is 64. For 4-bit devices, your word width choices are 4, 8, 16 and 32. This value should match the data bus word width in the target system for the device being programmed.
- **Next Device** — Designates the next device (next set member) in the set. For example, if you are using 8-bit devices and have specified a word width of 16 bits on the Load Memory Device screen, it will require two devices to store each 16-bit word. Typing **1** for the next set member directs UniSite to load the first device in the set at even-address bytes of the memory block. Typing **2** directs UniSite to load the second device at odd address bytes of the memory block.
- **Total Set Size** — Total set size defines how many virtual devices are in the set for device operations. For example, if you are loading 16-bit wide data from two 8-bit wide devices, your virtual device still equals one. (One 16-bit virtual device.) Any number between 1 and 99 can be entered. Automatic Set Size calculation will be attempted when any of the following parameters are changed: Device width, Data word width, Device block size or User data size. Total set size can be defined by the equation:

  Total Set Size = User data size / (Device block size X (Data word width / Device width)).
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block used to load from the device to the destination. This value is normally equal to the device size or a multiple of device size for loading a set. If zero or a value less than the device size is entered, it will be reset to device size for the load. User data size works with Total set size to determine the total amount of bytes to load from a set of devices.

- **Next Operation Begins At** — This is a read-only parameter, showing where in user memory the next data byte will be loaded to. This value is calculated from data word width, device block size, memory begin address, device width, and next set member parameters.

Options

The following options on the "all-parameters Load screen" normally appear ONLY if you press PF4 after entering the "non-default" Load screen. However, if you have changed any of the default parameters, those changed parameters will also show up on the "non-default" Load screen. The options shown with an * are visible on the screen only if the selected device supports the feature.

- **Memory Begin Address** — The memory begin address defines the first address, in hex, to where the first byte of data is loaded from a single device or from the device in the first socket during a SetSite load operation. If the Destination is RAM, it is a beginning RAM address. If the Destination is Disk, it is a beginning disk file address. The default address is 0.
- **Device Begin Address** — Type in the first hex master device address that will be loaded.
- **Device Block Size** — Device block size defines the size, in hex, of device data used in device operations. At device selection, device block size is automatically set to the device size and normally does not need to be changed. It is also automatically set to a smaller value if the device begin address is something other than zero. This parameter can be changed if desired. If a zero is entered, the device block size will be set to the device size.
- **Set Auto-increment** — This option, used in serial set mode, automatically directs UniSite to the next block in the set that is to be loaded. For example, if you have four 1K x 8 devices to load into a 4K x 8 block of memory, using the auto-increment option would direct UniSite to point to the first memory address of the next 1K block after each device had been loaded. For single device operations, this feature should be disabled and the "next device" should be set to 1.

* **Compare Electronic ID** — Compares the electronic ID of the socketed device against the electronic ID of the selected algorithm. Typing N disables this feature.

* **Odd/Even Byte Swap** — This option, when enabled (Y), allows the Most Significant Bytes (MSB) and the least significant bytes (LSB) of 16-bit words to be swapped when data is loaded from a 16-bit device. When the option flag is (N), the data is loaded from a 16-bit device and stored into UniSite User RAM with the Most Significant Byte (MSB) at an odd address. When it is (Y), the MSB is stored at an even address.

Program Device

The Program Device command allows you to copy data from RAM or a disk file into socketed blank device(s). Depending on whether a logic or memory device has been selected, either the Program Logic Device Screen or the Program Memory Device screen will appear when you select the Program device command.

Before you can program a device, you need to load the programming data into RAM or select a disk file as your data source. RAM data may be loaded from a master device, from a disk file or through the serial port.

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Program Logic Device

If you select a logic device and then invoke the Program command, UniSite's Program Logic Device menu will appear. Press PF4 to display available options. The following parameters can be specified in the Program Logic Device screen.

- **Source** — Specifies the source of the fuse data and test vectors that you wish to copy from; either RAM or disk. Select the data source by either using the space bar to toggle values, or by directly typing R or D.
- **Filename** — Specifies the name of the disk file you want the fuse data to be copied from. This parameter will not appear if you have selected RAM (R) as your data source. The Filename parameter must follow the MS-DOS convention: a specified drive (A: or B:), up to eight alphanumeric characters, followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT".
- **Security Fuse Data (0,1)** — Selects the data to be placed in memory for the security fuse of the device. You can place either a "0" or a "1" here without blowing the fuse. If you do want to program the security fuse, this parameter must be set to a "1" and the program security fuse option (also on this screen) must be enabled (Y).
- **Program Security Fuse** — Enables (Y) or disables (N) security fuse programming of the socketed logic device during a programming operation. If you do want to program the security fuse, the Security fuse data field must first be set to a "1" and then the Program security fuse option must be enabled (Y).

Options

The following options, on the "all-parameters Program screen", normally appear ONLY if you press [PF4] after entering the "non-default" Program screen. However, if you have changed any of the default parameters, those changed parameters will also show up on the "non-default" Program screen.

- **Illegal Bit Check** — Enables (Y) or disables (N) the illegal-bit test for UniSite. This test determines if a socketed device has already-programmed locations of incorrect polarity. An illegal-bit error will be generated for any programmed device bits whose corresponding bits in UniSite's RAM are not programmed.
- **Blank Check** — Enables (Y) or disables (N) the blank check test for UniSite. The blank check tests a socketed device to ensure it contains no bits that are already programmed.
- **Enable Yield Tally** — Directs UniSite to keep a running tally of the programming yields for the last sixteen types of devices programmed. These totals show how many devices passed and failed, and what specific errors, if any, have occurred.
- **Logic Verification (A,F,V)** — Selects whether you want to use fuse (F) verification or test vector (V) verification on your logic device. You may invoke both tests by selecting all (A). Fuse verification checks the fuse pattern physically programmed into the device with the pattern in UniSite's memory. Test vectors functionally test the part, using structured test vectors stored in memory.
- **Verify Passes (0,1,2)** — Selects the number of times you want the socketed device checked. Typing **0** passes directs UniSite to NOT test the device. Typing **1** will cause the device to be verified once, at the manufacturer's nominal Vcc. Typing **2** verifies the device at both the manufacturer's recommended high and low Vcc levels.
- **Reject Option (C,S)** — Selects the number of times that the socketed part will be pulsed with programming voltage, before it is rejected as unprogrammable. Typing **C** selects the commercial (device manufacturer's specification) number of pulses. Typing **S** (single) selects either a one-pulse or the military-specification number of programming pulses. In general, unless you are programming devices to a strict military specification, you should leave this option set at **C**.

Program Memory Device

If you select a memory device and then invoke the Program command, UniSite's Program memory device screen will appear. You may press [PF4] to display available options on the complex program screen. Items with an * are visible on the screen only if the selected device supports the feature. The following parameters can be specified in the Program Memory Device screen:

- **Source** — Specifies the source for the data that you wish to program into the socketed device: either RAM or disk. Select the data destination by either using the space bar to toggle values or by directly typing **R** or **D**.

- **Filename** — Specifies the name of the disk file that you want as your data source. This parameter will not appear if you have selected RAM (R) as your data source. The Filename parameter must follow the MS-DOS convention: a specified drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:27256.DAT".

- **Data Word Width** — Sets the word width of the data to be programmed. For 8-bit (or above) devices, the minimum word width is equal to the device width and the maximum is 64. For 4-bit devices, your word width choices are 4, 8, 16, and 32. This value should match the data bus word width in the target system for the device being programmed.

- **Next Device** — Designates the next device in the set. For example, if you are using 8-bit devices and have specified a word width of 16 bits on the Program memory device screen, it will require two devices to store each 16-bit word. Typing **1** for the next set member directs UniSite to program the first device in the set with even-numbered addresses of the memory block. Typing **2** uses odd-numbered addresses.

- **Total Set Size** — Total set size defines how many virtual devices are in the set for device operations. For example, if you are programming 16-bit wide data into two 8-bit wide devices, your virtual device still equals one. (One 16-bit virtual device.) Any number between 1 and 99 can be entered. Automatic Set Size calculation will be attempted when any of the following parameters are changed: Device width, Device block size or User data size. Total set size can be defined by the equation:

  Total Set Size = User data size / (Device block size X (Data word width / Device width)).

- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block used to program into a device from the source. This value is normally equal to the device size or a multiple of device size for set programming. If zero is entered, it will be reset to device size. User data size works with Total set size to determine the total amount of bytes to program into a set of devices.

- **Next Operation Begins At** — A read-only field that shows what address in user memory the next data byte will be programed from. This value is calculated from the data word width, device block size, memory begin address, device width, and next set member parameters.

* **Security Fuse Data (0,1)** — Selects the data to be placed in memory for the security fuse of the device. You can place either a "0" or a "1" here without blowing the fuse. If you do want to program the security fuse, this parameter must be set to a "1" and the program security fuse option (also on this screen) must be enabled (Y).

* **Program Security Fuse** — Enables (Y) or disables (N) security fuse programming of the socketed device during a programming operation. If you do want to program the security fuse, the Security fuse data field must first be set to a "1" and then the Program security fuse option must be enabled (Y).

Options

The following options on the "all-parameters Program screen" normally appear ONLY if you press [PF4] after entering the Program screen. However, if you have changed any of the default parameters (listed at the beginning of this section), those changed parameters will also show up on the "non-default" Program screen.

- **Memory Begin Address** — The Memory begin address defines the first address, in hex, from where the first byte of data is to be programmed into a single device or from the device in the first socket during a SetSite program operation. If the Source is RAM, it is a beginning RAM address. If the Source is Disk, it is a beginning disk file address. The default address is 0.
- **Device Begin Address** — Type in the first hex device address that will be programmed. The default is 0.
- **Device Block Size** — Device block size defines the size, in hex, of device data used in device operations. At device selection, device block size is automatically set to the device size and normally does not need to be changed. It is also automatically set to a smaller value if the device begin address is something other than zero. This parameter can be changed if desired. If a zero is entered, the device block size will be set to the device size.
- **Set Auto-increment** — This option, when enabled, directs UniSite (in serial set programming mode) to the starting memory address of the next block in the set that is to be programmed. For example, if you have four 1K x 8 devices to program from a 4K x 8 block of data, using the auto-increment option would direct UniSite to point to the first address of the next 1K block after each device had been programmed. For single device operations, this feature should be disabled and the "next device" should be set to 1.

* **Illegal Bit Check** — Enables the illegal-bit test for UniSite. This test determines if a socketed device has already-programmed locations of incorrect polarity. An illegal-bit error will be generated for any programmed device bits whose corresponding bits in UniSite's memory are NOT programmed.

* **Blank Check** — Enables the blank check test for UniSite. The blank check tests a socketed device, to ensure it contains no bits that are already programmed.

* **Compare Electronic ID** — Compares the electronic signature of the socketed device against the electronic signature of the selected algorithm. Typing N disables this feature.

- **Enable Yield Tally** — Directs UniSite to keep a running tally of the programming yields for the last sixteen types of devices programmed. These totals show how many devices passed and failed, and what specific errors, if any, have occurred.

* **Odd/Even Byte Swap** — This option, when enabled (Y), allows the Most Significant Bytes (MSB) and the Least Significant Bytes (LSB) of 16-bit words to be swapped when data is programmed into a 16-bit device. The data is programmed into a device retrieving the Most Significant byte from an odd memory address when the flag is (N) and an even memory address when it is (Y).

* **Reject Option (C,S)** — Selects the number of times that the socketed part will be pulsed with programming voltage, before it is rejected as unprogrammable. Typing **C** selects the commercial (device manufacturer's specified) number of pulses. Typing **S** (single) selects either a one-pulse or the military specification number of programming pulses. In general, unless you are programming devices to a strict military specification, you should leave this option set at "C".

* **Verify Passes (0,1,2)** — Selects the number of times you want the socketed device verified after programming. Typing **0** passes directs UniSite to NOT test the device. Typing **1** will cause the device to be verified once, at the manufacturer's nominal Vcc value. Typing **2** verifies the device at both the manufacturer's recommended high and low Vcc levels.

* **Enable EE Erase Device Feature** — Type **Y** in this field to enable erasing of electronically erasable PROMs.

* **Program Signature** — A user accessible field to enable/disable the Program Signature on the Program Memory Device screen if the part selected has this capability. Typing a (Y) enables this function and typing a (N) disables it.

* **Software Data Protection** — Enables (Y) or disables (N) the software data protection option for devices that support this option. When enabled, this option prevents writing to a device.

* *The options are visible on the screen only if the selected device supports the feature.*

Enhanced Security Fuse Capability

There is enhanced security fuse capability for EMICRO parts to allow security fuse data to be stored in a data file. The device that currently supports this is the Intel 8742AH.

Security Fuse Data Field

Security fuse data field can not be restored by using the More Commands/Configure system/Restore function. Security fuse data will instead be restored using a data file.

General Security Fuse Information

Whenever a disk file is specified as the data source, the programming screen should display the security fuse data from the disk file. When the security fuse data is changed, the data in the disk file is updated. (This applies to logic and EMICRO devices with security fuses.)

When the security fuse is changed with a disk file as the data source, and a disk error occurs such as "disk full" during the update, the entry is not successful and the old value remains. For memory devices, if the disk file is not big enough to cover the location for security fuses, the unprogrammed state of the fuses is defaulted.

Verify Device

The Verify device command allows you to compare data in the programmed device with that in RAM or in a disk file. Depending on whether a logic or memory device has been selected, either the Verify Logic Device screen or the Verify Memory Device screen will appear when you select the Verify device command.

To access this command, select Verify device from the Main Menu, as shown in the following illustration. Before you can verify a device, you need to load the data into RAM (from a master device, disk file or through the serial port) or have selected a disk file as the data source.

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Verify Logic Device

If you select a logic device and then invoke the Verify command, UniSite's Verify Logic Device screen will appear. Press PF4 to display available options in the complex verify screen. The following parameters can be specified in the Verify Logic Device screen:

- **Source** — Specifies the source of the fuse data and test vectors that you wish to verify, either RAM or disk. Select the data source by either using the space bar to toggle values or by directly typing R or D.

- **Filename** — Specifies the name of the disk file you want the fuse data and test vectors to be verified with. This parameter will not appear if you have selected RAM (R) as your data source. The Filename parameter must follow the MS-DOS convention: a specified drive (A: or B:), up to eight alphanumeric characters, followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT".

Options

The following items on the "all-parameters Verify screen" normally appear ONLY if you press [PF4] after entering the "non-default" Verify screen. However, if you have changed any of the default parameters (listed at the beginning of this section), those changed parameters will also show up on the "non-default" Verify screen.

- **Logic Verification** — Selects whether you want to use fuse (F) verification or test vector (V) verification on your logic device. You may invoke both tests by selecting all (A). Fuse verification checks the fuse pattern physically programmed into the device with the pattern in UniSite's memory. Test vectors functionally test the part, using structured test vectors stored in memory.
- **Verify Passes (1,2)** — Selects the number of times you want the socketed device checked. Typing **1** will cause the device to be verified once, at the manufacturer's nominal Vcc. Typing **2** verifies the device at both the manufacturer's recommended high and low Vcc levels..

Verify Memory Device

If you select a memory device and then invoke the Verify command, UniSite's Verify Memory Device screen will appear. Press [PF4] to display available options on the complex verify screen. The following parameters can be specified in the Verify Memory Device screen:

- **Source** — Specifies the source of the data that you wish to verify with the device: either RAM or disk. Select the data source by either using the space bar to toggle values or by directly typing **R** or **D**.
- **Filename** — Specifies the name of the disk file where you want the data to be verified from. This parameter will not appear if you have selected RAM (R) as your data source. The Filename parameter must follow the MS-DOS convention: a specified drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:27256.DAT".
- **Data Word Width** — Sets the word width of the data to be verified. For 8-bit (or above) devices, the minimum word width is equal to the device word width and the maximum is 64. For 4-bit devices, your word width choices are 4, 8, 16 and 32. This value should match the data bus word width in the target system for the device being programmed.

- **Next Device** — Designates the next device in the set. For example, if you are using 8-bit devices and have specified a word width of 16 bits on the Verify Memory Device screen, it will require two devices to verify each 16-bit word. Typing **1** for the next set member directs UniSite to verify the first device in the set with even-numbered addresses of the memory block. Typing **2** uses odd-numbered address.

- **Total Set Size** — Total set size defines how many virtual devices are in the set for device operations. For example, if you are verifying 16-bit wide data into two 8-bit wide devices, your virtual device still equals one. (One 16-bit virtual device.) Any number between 1 and 99 can be entered. Automatic Set Size calculation will be attempted when any of the following parameters are changed: Device width, Device block size or User data size. Total set size can be defined by the equation

  Total Set Size = User data size / (Device block size X (Data word width / Device width)).

- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block used to verify the device with the source. This value is normally equal to the device size or a multiple of device size for verifying a set. If zero is entered, it will be reset to device size. User data size works with Total set size to determine the total amount of bytes to verify with a set of devices.

- **Next Operation Begins At** — This read-only field shows what address in user memory the next data byte will be verified with. This value is calculated from the data word width, device block size, memory begin address, device width, and next set member parameters.

Options

The following items on the "all parameters Verify screen" normally appear ONLY if you press [PF4] after entering the simple Verify screen. However, if you have changed any of the default parameters (listed at the beginning of this section), those changed parameters will also show up on the "non-default" Verify screen.

- **Memory Begin Address** — The Memory begin address defines the first address, in hex, from where the first byte of data is verified against a single device or against the device in the first socket during a SetSite verify operation. If the Source is RAM, it is a beginning RAM address. If the Source is Disk, it is a beginning disk file address. The default address is 0.

- **Device Begin Address** — Type in the first hex device address that will be verified.

- **Device Block Size** — Device block size defines the size, in hex, of device data used in device operations. At device selection, Device block size is automatically set to the device size and normally does not need to be changed. It is also automatically set to a smaller value if the device begin address is something other than zero. This parameter can be changed if desired. If a zero is entered, the device block size will be set to the device size.

- **Set Auto-increment** — When enabled, this option directs UniSite (when in a set verify mode) to the starting memory address of the next data block that is to be verified. For example, if you have four 1K x 8 devices to verify against a 4K x 8 block of data, using the auto- increment option would direct UniSite to point to the first address of the next 1K block after each device had been verified. For single device operations, this feature should be disabled and the "next device" should be set to 1.

* **Compare Electronic ID** — Compares the electronic signature of the socketed device against the electronic signature of the selected algorithm. Typing **N** disables this feature.

* **Odd/Even Byte Swap** — This option, when enabled (Y), allows the Most Significant Bytes (MSB) and the Least Significant Bytes (LSB) of 16-bit words to be swapped, when data is verified between a 16-bit device and memory. When the option is (N), data is verified with the Most Significant Byte at an odd address. When it is (Y), the MSB is at an even address.

- **Verify Passes (1,2)** — Selects the number of times you want the socketed device checked. Typing **1** will cause the device to be verified once, at the manufacturer's nominal Vcc. Typing **2** verifies the device at both the manufacturer's recommended high and low Vcc levels.

More Commands

Use the More commands to access UniSite's less often used commands (commands that do things OTHER than loading, programming and verifying devices).

The More Commands menu includes:

- **Configure System** — Allows you to restore, edit, and save UniSite's communications, interface, serial I/O and programming parameters (items shown on the default parameters list at the beginning of this section), and select a terminal type. You could use these commands to set up unique parameter files for each device type you want to program and then save those values in the More commands/Configure system/Save screen. These values can be called back at a later date using the More commands/Configure system/Restore screen.

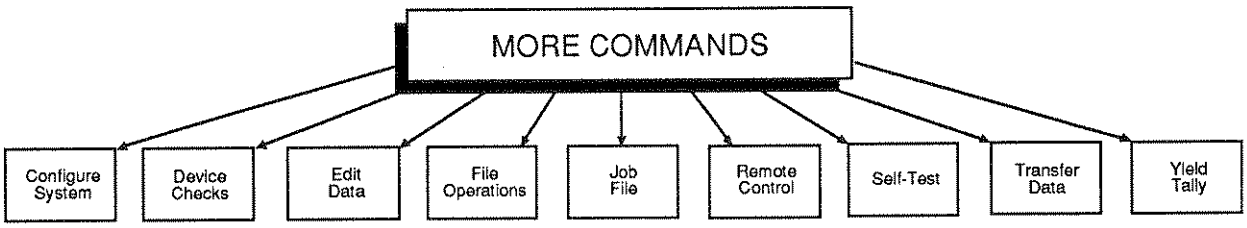
- **Device Checks** — Performs various device tests on socketed devices.

- **Edit Data** — Allows you to edit RAM or disk data. Separate editing features exist for logic and memory devices.

- **File Operations** — Performs various operations on UniSite's disk files, such as loading, saving or renaming a file.

- **Job File** — Allows you to playback a series of keystrokes, useful if you program the same devices a lot. Up to ten job files may be stored on any disk.
- **Remote Control** — Switches UniSite into remote mode, where it will accept commands sent from a remote computer. The CRC (Computer Remote Control) section lists the commands recognized by UniSite in remote mode.
- **Self Test** — Performs various checks on UniSite's circuitry.
- **Transfer Data** — Allows you to upload or download data to or from UniSite.
- **Yield Tally** — Allows you to view or clear programming statistics.

The figure shown below illustrates the relationship between the screens available from More commands.



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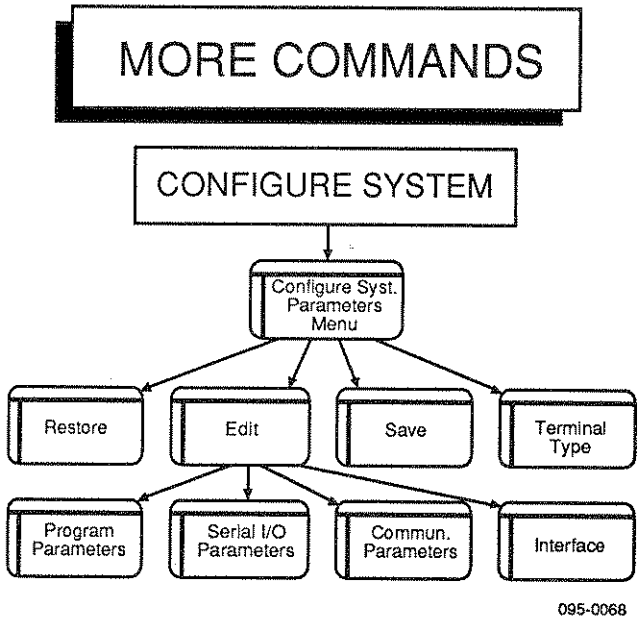
Configure System

The Configure System command allows you to accomplish three basic tasks:

- Establish communications protocols between UniSite and the other equipment in your system, such as a terminal, remote or host computer.
- Configure the remote and terminal ports (connectors) so they will be compatible with the port of your terminal, remote or host computer.
- Edit, save or restore a set of programming features unique to the device type you want to program.

The excerpt of the command tree shown below illustrates the relationship between the screens of this command. To access this menu, select More commands from the Main Menu and then Configure systems from the More commands menu. Features of the Configure systems menu are described on the following pages.



Edit

If you select Edit from the Configure system menu, UniSite will display the Edit parameter menu. From this screen you can elect to choose Programming, Serial I/O, Communication or Interface Parameter screens which are described in the following subsections. Default parameter settings are shown in the table at the beginning of this section.

Programming Parameters

Use the Edit Programming Parameters screen to specify programming options, device check, options, and to enter memory block parameters. The options that you selected or the parameters that you enter will be used in the current programming session. If you want to use them in a future programming session, use the Save screen; use of the Save screen will be explained in a later subsection.

- **Filename** — Specifies the disk data file which is used for load, program, and verify operations when the programming data source is set to D (disk). Enter the drive specification (A: or B:), then the filename (using eight characters or less and a three-character file extension preceded by a (.), then press ↵ .

- **Source/Destination** — Specifies the location of the user memory data to be programmed, loaded, verified, downloaded, uploaded or edited. Press the space bar to alternate the choice between D (Disk) and R (RAM)or type the desired character. When D is selected, the filename field is used to allow the filename specification.

- **Security Fuse Data** — Specifies in which state you want the security fuse to be programmed. Press the space bar to alternate the variable between 1 and 0, or type the desired character. The security fuse will not be programmed until the Program security fuse feature is enabled; this feature is enabled on this same screen and is described later in this subsection.

- **Reject Option** — Specifies the maximum number of programming pulses required to program a device. Pressing the spacebar toggles between:

  C Commercial reject count

  S Single or military reject count

  Selecting S indicates no more than one pulse will be allowed to program any bit in the device in most cases while for other devices, S will select the military reject count as recommended by the manufacturer. If you selected C (commercial) as the variable for this option, then the device manufacturers recommended number of programming pulses will be used.

- **Logic Verification** — Specifies what type of logic verification you want performed on your device. You can choose F(Fuse), V (Vector), or A (All). If you type A, both fuse verification and structured test will be performed. Pressing the space bar steps UniSite through the three choices, or you can just type in the desired character.

- **Verify Passes (0,1,2)** — Specifies the number of passes used to verify that your data has been programmed into the part. You can choose from the following options:

  0 No passes (invalid in the Verify screen)

  1 A single pass with Vcc at the nominal value

  2 Two passes, one at the maximum allowed Vcc, and one at the minimum allowed Vcc value

- **Verify Data Format** — (B,H) Allows user to select the mis-verify data display format, either binary (B) or hex (H), for the VERIFY Memory Device screen.

- **Data Word Width** — Should match the data bus word width in the target microprocessor system for the device being programmed. For 8-bit (or above) devices, any word width between 4 and 64 (inclusive) may be typed in. For 4-bit devices, your word width choices are 4, 8, 16 and 32. When performing a Quick copy function, the data word width is set to the device word width and restored to the original value automatically afterwards. UniSite always changes this parameter to match the selected device's width, with one exception: for example, if the current data word width is 16, your selected device's word width is 8 and the previously-selected device's word width is also 8, this parameter will not change.

- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block used in device operations. This value is normally equal to the device size or a multiple of device size for SetSite operation. User data size works with Total set size to determine the total amount of bytes for a set operation. This parameter can also indicate the number of bytes in a data transfer operation.

- **Memory Begin Address** —The Memory begin address defines the first address in RAM, in hex, to load data into from a device or the first address from where a device is programmed/ verified. If the user memory is RAM, it is a beginning RAM address. If the user memory is Disk, it is a beginning disk file address. The default address is 0.

- **Device Begin Address** — Specifies the device first address used in device operations. Enter the address, then press [↵] . This option is used for memory devices only.

- **Device Block Size** — Device block size defines the size, in hex, of device data used in device operations. At device selection, device block size is automatically set to the device size and normally does not need to be changed. It is also automatically set to a smaller value if the device begin address is something other than zero. This parameter can be changed if desired. If a zero is entered, the device block size will be set to the device size.

Note: The rest of the parameters on this screen are optional device checks and require only the entry of a Y(Yes) or N(No).

- **Illegal Bit Check** — Checks the device for bits that are already programmed that don't have corresponding bits set in memory.

- **Blank Check** — Checks the device that is to be programmed, for any bits that are already programmed.

- **Compare Elec ID** — Compares the electronic ID of the device against the electronic ID of the selected algorithm.

- **Enable Yield Tally** — Maintains statistics on programmed devices. You many view the statistics by selecting Yield Tally from the More Commands menu. A more complete description of this feature can be found later in this section (see Yield Tally).

- **Program Security Fuse** — Enables (Y) or disables (N) security fuse programming of the socketed logic device during a programming operation. If you do want to program the security fuse, the Security fuse data field must first be set to a **1** and then the Program security fuse option (also on this screen) must be enabled (Y).

- **Erase EE Device** — Bulk erases the electronically erasable parts before UniSite attempts to program them.

- **Odd/Even Byte Swap** — Swaps data, when enabled, at odd and even address locations during a load, program or verify operation. The organization of bytes in RAM is not altered. Swapping bytes is useful when manipulating 16-bit data, when the target system has a different architecture than the original file convention. For example: Motorola 16-bit data files store the Most-Significant Bytes (MSB) at even-byte locations; Intel stores them at odd-byte locations. UniSite maintains its RAM and file data with the convention that the (MSB) of a 16-bit word resides in the odd byte of memory (Intel convention).

  The default for this option on the device screens is (N) but when the option flag is (Y), the data is loaded from a 16-bit device and stored into UniSite User memory with the MSB at even addresses.

  Similarly, when programming a device, the data is programmed into a device retrieving the MSB from an odd memory address when the flag is (N) and an even memory address when it is (Y).

- **Continuity Check** — Checks for open device pins before UniSite programs the device. Because the continuity check's default condition is the enabled state, selection of a new device type will automatically enable a continuity check.

- **Extended Algorithm** — When enabled, this feature will allow extended device support. Most users will not need to be concerned with this feature; it is used only if there are custom test algorithms. A user-accessible file ALG.EXT containing algorithms is used by UniSite to provide custom algorithm selection by the user. However, when the ALG.EXT file is used, only those devices found in ALG.EXT can be selected. ALG.EXT files are algorithm files issued by Data I/O to handle device approvals and special device algorithm updates. It can be copied to either the System disk or the Algorithm disk. When ALG.EXT file cannot be found, the error message "Cannot access system file. Insert algorithm disk." is displayed.

  This parameter is added to allow the user to use the custom algorithms in ALG.EXT or to disable this feature and use the current device selection. The factory default setting of this parameter is (N).

- **Serial Vector Test** — When enabled, this test applies each vector input states serially, starting with pin one and stepping through the remaining pins. This test is a diagnostic tool designed to help debug and classify test vector failures. Specifically, this test is designed to isolate test vectors that are sequence dependent. If a sequence-dependent vector is found, it should be broken into two or more vectors to make them sequence independent.

  The JEDEC specification for test vectors requires that test vectors be sequence independent. If sequencing between pins is important then the test vector should be separated into two or more vectors, to make them sequence independent. This test will help isolate vectors that are sequence dependent and should be expanded.

  This switch is available only for logic devices and defaults to N on power up. The switch is also returned to N when parameters are restored or when another device is selected.

- **High Speed Logic Drivers** — When enabled, this test increases the speed of the logic transitions between "0" to "1" and "1" to "0" of the test vector input states. This test is a diagnostic tool designed to help debug and classify test vector failures. Specifically, this test is designed to help identify vector transitions that are speed dependent. When isolated, these vectors should be edited to use the high speed clocking functions provided by test vector characters C, K, U, and D.

  The speed of the logic transitions is increased by driving the "0" and "1" levels using the high speed logic drivers instead of a current limited drivers.

  The JEDEC specification for test vector "0" and "1" inputs states defines that these inputs be current limited, so that the outputs of the device under test can over drive the "0" or "1" level without damaging the device. However, the current-limited drivers normally used to drive "0" and "1" have inherently slow transition speeds. Enabling this test will help identify vectors that are sensitive to transition speeds.

  This switch is available only for logic devices and defaults to N on power up. The switch is also returned to N when parameters are restored or when another device is selected.

CAUTION: ***If used improperly, this test may cause Pindriver over current errors or may damage the device output pins. This test should only be used as a diagnostic test to debug test vector problems.***

- **Compensated Vector Test** — When selected, this feature enables load compensation on PLD output pins under test during structured vector testing. This may eliminate "structured test errors" when testing PLDs sensitive to output loading, where many of the devices register transitions simultaneously. This switch is available only for logic devices and defaults to N at power up. The switch is also returned to N when parameters are restored or when another device is selected.

Serial I/O Port Configuration

Use this screen to set up the terminal and remote ports so they can be compatible with your terminal or host computer.

A change in the serial port parameters does not become effective until you press [↵] . If terminal settings are changed, a message will appear prompting you for another [↵] after you have altered your terminal to match the new settings. Output to the terminal is suspended until you enter the second [↵] .

- **Baud Rate** — You may select baud rate and parity for both the terminal and remote ports from this screen. When UniSite is turned on, the baud rate will default to the baud rates you have designated as power on defaults. If the default baud rate is incompatible with your terminal, you may change the baud rate after power up by invoking the Auto baud feature.

- Press [Brk] [A] at the power-on screen; UniSite can detect this sequence even though its baud rate may not match that of the terminal. When UniSite detects the [Brk] [A] sequence, it calculates the terminal's baud rate and then changes its own rate to match it. After UniSite has matched baud rates, the power-up screen will then appear. After the terminal and UniSite are communicating, you can manually change the baud rate by selecting serial I/O from the Configure system/Edit parameter menu. Step through the baud rates supported by UniSite, by pressing the space bar or by entering the first digit. Use the arrow keys to move the cursor to the next port.

  UniSite supports the following baud rates: 50, 75, 110, 134.5, 150, 200, 300, 600, 1050, 1200, 1800, 2000, 2400, 4800, 7200, 9600 and 19.2K. However, not every baud rate on one port will work when other baud rates are selected for the other port. If incompatible baud rates are selected, an error message will appear and a beep will sound. The following table shows which rates are not compatible.

If this rate is used for either port	This rate will not work on the other port
50	75
200	150
1500	2000
7200	1800

- **Parity** — You may select parity from this screen by moving the cursor to the line for selecting parity and pressing the space bar or typing the character desired. Three options are available for the parity setting: N (No), O (Odd), and E (Even).

- **Data Bits** — Select the number of data bits UniSite will recognize during serial port transfers, either 7 or 8. Use the space bar to choose the value desired, or type in the value directly.

- **Stop Bits** — Select the number of stop bits Unisite will recognize between data bytes. Two stops bits are generally used for baud rates of 110 or lower.

- **Enable CTS/DTR** — This field indicates whether or not CTS/DTR (Hardware Handshake) is enabled.

Communication Parameters

The More commands/Configure system/Edit/Communication screen allows you to alter UniSite's input/output characteristics, used when uploading or downloading data.

- **Source/Destination (R,T)** — Select the source/destination port of the data to be transferred, either the remote (R) or the terminal (T) port.
- **I/O Translation Format** — Type in the two-digit decimal code that corresponds to the format in which the data will be transferred. For a detailed list and sample of each format, see the Data Translation Formats section of the manual.
- **I/O Addr Offset** — Specifies the transfer data offset beginning address. The offset address is subtracted from the I/O addresses, during downloading, so that data will be properly located in user RAM or on disk. Typically, this is the lowest address encountered. Similarly, this address is also added to the user memory address during uploading. This entry and all the memory block information is expressed as a hexadecimal number. If the I/O Addr Offset is set to "FFFFFFFF", the default I/O offset is set to the first incoming address of the transfer data on input and to 0 on output.
- **I/O Timeout** — Limits the amount of time that UniSite will wait for a data transfer to begin. It has a range of 0 to 99 seconds. 0 disables the timeout completely.
- **Upload Wait** — Sets the period of time that UniSite will wait before it begins sending data to the host computer after the host upload command is sent. The range of this parameter is 0 to 99 seconds.
- **Transmit Pacing** — Allows you to enter an upload delay value. This value represents a time-delay that will be inserted between characters transmitted to the host computer during the upload process. The time delay is specified in tenths of milliseconds. For example, 12 equals 1.2 milliseconds. The minimum delay possible is 4 (.4 milliseconds). The maximum delay possible is 99 (9.9 milliseconds). A 0 value entered means no delay.
- **Download Echoing** — Displays the data that is being downloaded. This may slow down UniSite in receiving data and is not recommended for high baud rates, such as 9600 and above. Download echoing may not be used with the binary formats.
- **Output Record Size** — Specifies the number of data bytes contained in each data record during upload. The range of this parameter is 0 to 256 bytes. Some formats have fixed record lengths for which this parameter does not apply.

- **Number of Nulls** — Sets the number of null characters sent between each record in a data file after a carriage return and line feed. The range of this parameter is 0 to 254 nulls. 255 specifies no nulls and inhibits the line feed.

- **Instrument Control Code** — Specifies how the data transfer will be controlled. Selecting 0 specifies regular Xon /Xoff handshaking, selecting 1 or 2 specifies special handshaking sequence (see the Translation Formats section in this manual).

- **Fill Memory Option** — Specifies what data the user memory will be filled with before downloading begins. This option is used for "Download data" and "Input from disk" operations. The choices are N (none), D (default), and U (user specified). If you select N (none), the memory will not be changed and what ever is present in the memory will remain there to be overwritten by the downloaded data. If you select D (default), the user memory will be filled with the data appropriate to initialize unused locations to the "unprogrammed" state for the device type selected. If you select U (user specified), then the user memory will be filled with whatever you specify in the Fill data option.

- **Fill Data** — Allows you to type in the hexadecimal data to be placed at unused locations of the user memory during download. To invoke this option, you must also specify **U** as your selection for the Fill memory option. User memory may also be filled with the specified data during the Edit operation.

- **High Speed Download** —When enabled (Y) UniSite will perform downloads using a baud rate of 115.2Kbd on the remote port if the data format selected is one of those supported by HiTerm for high speed downloads. Refer to the HiTerm User's Guide for a list of supported formats. This feature should be used in conjunction with the HiTerm software provided by Data I/O to run on IBM compatible computers. This high speed feature is available only on UniSite's Remote port so UniSite must be configured to have the terminal functions on the Remote port to perform high speed downloads with HiTerm. Enabling the high speed download parameter will cause the User Menu Port parameter to be changed to "R" (Remote) if it was not already set to that value. Refer to the description of the User Menu Port parameter for details.

- **User Menu Port** — Specifies which of UniSite's two ports (Terminal or Remote) should be used by UniSite for sending user menu information and for receiving the user's commands. This is the port that the user's terminal or PC is connected to. After the parameter is changed and a ↵ is entered, the user should move the cable going between the terminal or PC and UniSite to the UniSite port specified. Ensure that the baud rates of the terminal and the port you are switching to match.

- **JEDEC I/O Translate DIP/LCC Vectors** — Use this feature if you have created test vectors for a DIP (dual, in-line package) device but actually want to program its LCC (leadless chip-carrier) packaged version. If this feature is invoked, UniSite will alter the test vectors during I/O translation, accommodating for the different pinouts of the two packages. During downloading, vectors are converted from DIP to LCC; uploading converts test vectors from LCC to DIP. Type Y to enable DIP-to-LCC test vector transformation.

- **Upload: Use End-of-File Delimiter** — Inserts an end-of-file delimiter (character) following an uploaded file. This delimiter signals the host system that the transmission of that particular file is complete. During an uploading operation, an end-of-file character would be transmitted to the host. If you wish to invoke this feature, you must select both this option (by typing Y) and the two-digit hex data for the ASCII character you want to use as the end-of-file character. Any value between 01 and 1F, inclusive, may be selected.

Note: This feature may be used only if you are using a format that uses an end-of-text character; it cannot, for example, be used for binary files.

- **Upload End-of-File Delimiter (1-1F)** — Selects the two-digit hex data of the ASCII character you want to use as the end-of-file character in uploading data to a host computer. Any value between 01 and 1F, inclusive, may be selected.

- **Download: Use End-of-File Delimiter** — Inserts an end-of-file delimiter (character) following a downloaded file. This delimiter signals the UniSite that the transmission of that particular file is complete. During a downloading operation, characters after the last record and before the end of the file would be ignored. If you wish to invoke this feature, you must select both this option (by typing Y) and the two-digit hex data from the ASCII character you want to use as the end-of-file character. Any value between 01 and 1F, inclusive, may be selected.

- **Download End-of-File Delimiter (1-1F)** — Select the two-digit hex data of the ASCII character you want to use as the end-of-file character in downloading from a host computer. Any value between 01 and 1F, inclusive, may be selected.

- **Upload Host Command** — Type in the command you want to use to tell the host system what to do with the data to be uploaded. The command may be up to 58 characters in length. You can use host operating system (such as UNIX) commands on this line: for example, you could have an upload command such as "CAT > 27128RUN." UniSite will append a ↵

- **Upload Host Command** — Type in the command you want to use to tell the host system what to do with the data to be uploaded. The command may be up to 58 characters in length. You can use host operating system (such as UNIX) commands on this line: for example, you could have an upload command such as "CAT > 27128RUN." UniSite will append a ↵ to the command. If you are performing an upload to a PC running the HiTerm software, enter the command "**transfer filename**" or "**tr filename**".
- **Download Host Command** — Type in the command you want to send to the host system to initiate a file transfer download to UniSite. The command may be up to 58 characters in length. You can use host operating system (such as UNIX) commands on this line: for example, you could have a download command such as "CAT 27128RUN." If you are performing a download from a PC running the HiTerm software, enter the command "**transfer filename**" or "**tr filename**".

Interface Parameters

- **Power On CRC Mode** — This feature allows you to power up UniSite and have it automatically enter computer remote control mode. Type **Y** to enable automatic power-up in remote control; type **N** to disable.
- **Enable Terminal Beeps** — Type **Y** to enable an audible tone each time an error message is generated by UniSite.
- **Remote On Code** — Use this feature if you want to use ASCII characters to enable the remote serial port. Type in the two-digit hex data that represents the ASCII character you want to use to enable remote control.
- **Remote Off Code** — Use this feature if you want to use ASCII character to disable the remote serial port. Type in the two-digit data that represents the ASCII character you want to use to disable remote control.
- **Main Menu Job Files** — Enable this feature if you want to be able to start a Job File from the Main Menu rather than having to go to the Job Files menu. Type **Y** to allow initialization of Job Files from the Main Menu.

Save

Save System Parameters

"System parameters" are defined by UniSite as consisting of all the features on the Programming, Serial I/O, Communication and Interface screens. Using the Save screen, you can save a set of system parameters for future use. The device algorithm selected will also be saved. This feature is useful if you want UniSite to power up with a particular set of parameters pre-set, or multiple users prefer to have their own set of parameters easily available.

To use the Save feature, you need only go through the various Configure/Edit menus and select the characteristics you need. When you are finished selecting, go to the Save screen and select a name and item number for the characteristics just chosen. For example, you could call a particular set of characteristics "27512.CFG."

File number 0 is reserved for the factory defaults and is write-protected. File number 1 is the set of system parameters which you can specify for UniSite to power up with. File number 2 is used for CRC user-defined defaults that can be restored using the Restore System Parameters screen or the Remote CRC command 'FD']. Files 3 thru 9 are files you can name for particular jobs or users.

Restore

Restore System Parameters

"System parameters" are defined by UniSite as consisting of all the features on the Programming, Serial I/O, Communication, and Interface screens. Use the Restore screen to restore a set of system parameters that you saved using the Save feature. The saved device algorithm will also be restored (so you need not select the device again).

The Restore menu contains a list of all the files that have been entered on the Save menu. To use the Restore feature, enter the file number that corresponds to the filename that you want to use and press ↵ . UniSite will then load the system parameters that you selected.

UniSite always powers up using the set of parameters designated as the "Power On Defaults" (item one on the Restore System Parameters screen). If you do not want to use the Power On Defaults, you must select an alternate.

Terminal Type

To change the terminal type during UniSite operation, use the following steps:

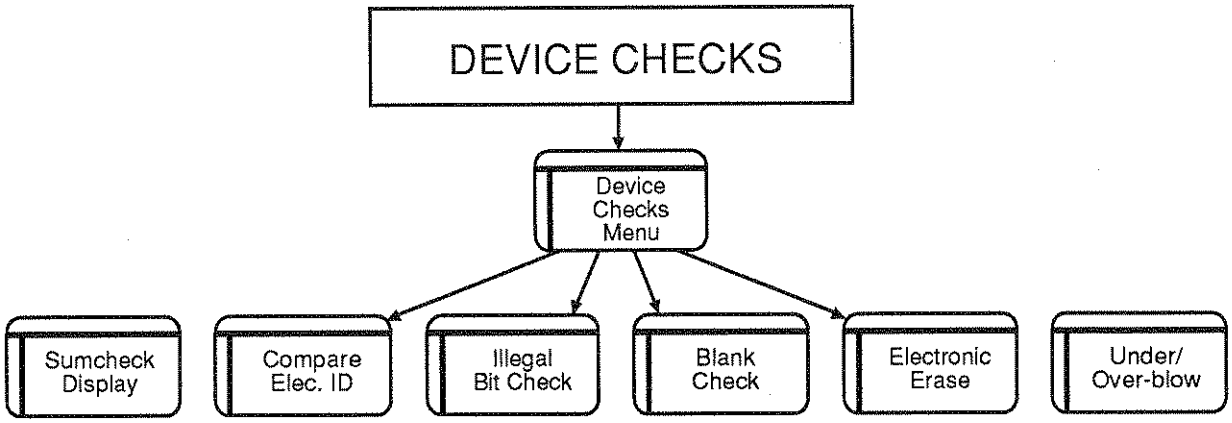
1. Select the Serial I/O Parameters screen from the More commands/Configure system/Edit menu and observe the baud rate of the port that you intend to use to connect the new terminal. Change the baud rate setting on the new terminal to match the port's baud rate if they aren't the same values.

2. Go to the More commands/Configure system/Terminal type menu and enter the number which corresponds with the new terminal type. After you select the correct terminal type you will be asked if you want to save the new terminal type as the power on default type. Type Y or N. At this point, the old terminal may display random characters since UniSite is now configured for the new terminal type.

3. Disconnect the old terminal and connect the new terminal to UniSite.
4. Power up the new terminal and press Ctrl R . The screen will display the Configuration system screen. You can then resume normal operation.

Device Checks

The More commands/Device checks menu allows you to perform device checks on devices you wish to program or on blocks of data in user memory. The relationships of the screens are illustrated in the figure shown below.



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To execute the commands described in this subsection, you must do the following:

1. Be sure that the device to be checked is inserted and locked into the device socket.
2. Press ↵ to execute the command.

Sumcheck Display

The results of this command depend on whether a memory or a logic device has been selected. The sumcheck allows you to check to see that the user memory data matches that which is known for the original source, for example:

Logic Device Sumcheck

The following fields will appear on this screen:

- **Source** — Select the source of the data to calculate the sumcheck on, either RAM (R) or the disk (D).
- **Filename** — This field only appears if you have specified the disk as the data source. Type in the filename to calculate the sumcheck of.

  When you have specified the data source, press ↵ and UniSite will calculate the 4-digit sumcheck of the fuse pattern.

Memory Device Sumcheck

For memory devices, the display will show the user memory block sumcheck for the device, or for each device in a set (as well as the total set's sumcheck). The total RAM sumcheck will also be displayed in the message area. The following fields will appear on this screen:

- **Source** — Select the source of the data to calculate the sumcheck on, either RAM (R) or the disk (D).
- **Filename** — This field appears only if you have specified the disk as the data source. Type in the filename to sumcheck.
- **Memory Begin Address** — The Memory begin address defines the first address, in hex, from where the first byte of data is to be sumchecked. If the source is RAM, it is a beginning RAM address. If the source is Disk, it is a beginning disk file address. The default address is 0.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block to sumcheck from the source. This value is normally equal to the device size or a multiple of device size for sumchecking a set. If zero is entered, it will be reset to device size for sumchecking RAM or the file size for a file operation. User data size works with Total set size to determine the total amount of bytes to sumcheck from the source.
- **Data Word Width** — Sets the number of bits in the data word width. For 8-bit (or larger) devices, the minimum word width is equal to the device width, and the maximum is 64. For 4-bit devices, your word width choices are 4,8,16 and 32. This value should match the data bus word width in the target system for the device being programmed.
- **Next Operation Begins At** — This field cannot be altered and appears only to inform you of where (what hex address) the next operation will begin.
- **For Member X OF Y** — Type in the individual member "X" and total members of the set, "Y", that you want to sumcheck.
- **Individual Sumcheck** — This is the individual sumcheck for member "X" that was typed in above.
- **Set Sumcheck** — This is the total sumcheck for the entire set of "Y" devices.

Compare Electronic ID

This feature is useful when used to compare electronic IDs of devices to prevent accidentally damaging a device by typing in the wrong device type or family and pinout code.

Note: You cannot use an electronic ID to automatically select the proper algorithm to program a device.

If UniSite compares the socketed device, and it has an electronic ID that corresponds to a family and pinout code or device type other than the one you selected, UniSite will signal an error. The electronic ID of the device in the socket will then be displayed in this manner:

UniSite will display (in hexadecimal) the first two of the 16 locations of the device's electronic ID. Location 0 identifies the manufacturer; location 1 identifies the device.

Illegal Bit Check

The illegal-bit test checks a device for previously programmed locations that have incorrect polarity with respect to the data in user memory. Illegal bits prevent the data in user memory from being programmed into the device correctly. If UniSite detects an illegal bit, it will print an error message indicating this condition. If the device is erasable, the illegal bit can be corrected by erasing the device. The Illegal bit check is not performed for Electronically Erasable devices.

Logic Device Illegal Bit Check

- **Source** — Specify the source to use when checking for illegal bits, either RAM (R) or the disk (D).
- **Filename** — This field appears only if you have specified the disk as the data source. Type in the file to use when testing for illegal bits.

Memory Device Illegal Bit Check

- **Source** — Specify the source to use when checking for illegal bits, either RAM (R) or the disk (D).
- **Filename** — This field appears only if you have specified the disk as the data source. Type in the file to use when testing for illegal bits.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block used to check for illegal bits of a device from the source. This value is normally equal to the device size or a multiple of device size for checking illegal bits of a set. If zero is entered, it will be reset to device size for RAM or file size for a file operation. User data size works with Total set size to determine the total amount of bytes to check in a set.
- **Total Set Size** — The total number of parts in the set to check for illegal bits.

- **Data Word Width** — Sets the number of bits in the data word width. For 8-bit (or larger) devices, the minimum word width is equal to the device width, and the maximum is 64. For 4-bit devices, your word width choices are 4,8,16 and 32. This value should match the data bus word width in the target system for the device being programmed.
- **Next Device** — Type in the number corresponding to the next device in the set to check for illegal bits.
- **Next Operation Begins At** — This field cannot be altered and appears only to inform you of where (what hex address) the next operation will begin.

Blank Check

The Blank check command allows you to check a device before you attempt to program it to make sure that it is blank. When you execute this command, the Blank device check screen displays whether the socketed device is blank.

Electronic Erase

If you select this command, UniSite will bulk erase an electronically erasable device. To access this command, select More commands/Device checks/Electronic erase.

To erase a device, simply insert the device you want to erase and press [↵] . UniSite will erase the device and a message will appear, indicating that the operation has completed.

Note: This screen cannot be entered if you have selected a device that cannot be electronically erased (a bipolar PROM, for example). A blank check will be run after a bulk erase operation if the blank check switch is enabled and if the device you are using supports blank check.

Under/Over-Blow (Logic Devices Only)

The under/overblow feature compares the fuse map of a socketed device with the fuse map either resident in RAM or in a disk file, to ensure that the two match. An "underblow" condition means that the device's fuse is intact, but the data in memory indicates that it should have been blown. An "overblow" means that the device's fuse is blown, but should have remained intact.

- **Source** — Select the source of the data to be compared against that of the socketed device, either RAM (R) or Disk (D).
- **Filename** — Specifies the name of the disk file which is to be compared to the socketed device. This parameter will not appear if you have selected RAM (R) as your source. The filename parameter must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT". To use the under/overblow feature, do the following:

1. Select the device type. Insert the logic device you want to check into UniSite's socket.

2. After you selected the under/overblow source data, press [↵] .The under/overblow screen will then be displayed. If the data from RAM or disk file specified on the previous screen does not have proper fuse data (for the specified device type), a message will appear that says the file is not initialized. Type **C** to initialize the file.

3. Data shown on the screen is displayed in a format similar to that of the fuse editor, with two exceptions: additional character symbols are used to display overblown (B) and underblown data (U), and, unlike the fuse editor, no data can be edited. The fuse number corresponding to the cursor's location will appear at the top of the screen. To move the cursor, use the arrow keys. See the following table for a list of screen commands.

Note: When you have finished looking at the data, press **PF1** *to return to the Main Menu or* **PF2** *to return to the Device checks menu.*

Under/Overblow Commands

Keystroke	Command	Description
Ctrl N	Next Block	Displays the next page of under/overblow data.
Ctrl P	Prev Block	Displays the previous page of under/overblow data.
Ctrl F	Search Pattern	Searches for one of four character symbols within the under/overblow data. The four valid characters you can search for are: "X" (intact fuse) "-" (blown) "B" (overblown) "U" (underblown) After you select the search character, the search will begin at the current cursor position and will continue until either a match is found or the end of the fuse map is reached.
Ctrl B	Jump to Fuse	Moves the cursor quickly to a specific fuse. When you type this command, a highlighted area will appear just after the "^B: Jump to Fuse" prompt at the bottom of the screen. Then, type in the fuse number that you want to jump to and press ↵ .
PF2	Exit	Exits the Under/Overblow screen and returns UniSite to the Device checks menu.
PF1	Exit to Main	Exits the Under/Overblow screen and returns UniSite to the Main Menu.

Edit Data

You may use UniSite's Edit Data command to make changes to RAM or to disk data. Separate editors exist for memory and logic devices: a fuse map and test vector editor for logic devices, and a memory editor for memory devices. When you select the Edit Data command, UniSite displays a menu corresponding to the type of device that is currently selected. For example, if you select a logic device from the Select Device Menu and then go to the Edit Data Menu, UniSite will display the Edit Logic Menu. In addition to the three editors, certain other functions are also available from the Edit Data menu. The Edit Memory Menu includes "complement", "move data" and "fill memory" commands. The Edit Logic Menu provides "fill fuse map" and "clear vectors" commands.

Edit Logic Menu

If you select a logic device and then invoke the editing command, UniSite's Programmer Fuse Map Edit menu will appear. This menu contains the Edit Logic, Vector Edit, Fill Fuse Map and Clear Vectors features. To choose one of these features, type in the first letter of the one you wish to invoke. For example, to select the Vector Edit feature, type **V**.

The Programmer Fuse Map Edit menu allows entry of three parameters which specify information about the fuse map: source, filename and data representation.

Edit Fuse Map

- **Source** — Specifies the source of the fuse data that you wish to edit; either RAM or disk. Select the data source by either using the space bar or by directly typing in **R** or **D**.
- **Filename** — Specifies the name of the disk file which contains the fuse data to be edited. This parameter will not appear if you have selected RAM (R) as your data source. The Filename parameter must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alpha-numeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT".
- **Data Representation** — Specifies how the data in RAM or data file appears on the terminal's screen. The two choices for this parameter are "X" and "-", or "0" and "1". Move the cursor to the data representation window and press the space bar to toggle the parameter to the representation desired. "X" and "0" represent an unprogrammed state; "-" and "1", a programmed state.

To edit fuse data, do the following:

1. After you have specified the three edit logic parameters, press ↵ . This will invoke the fuse editor and the screen will change to show the data in the form of a logic fuse map.
2. If the data from RAM or the disk file specified on the previous screen does not have proper fuse data (for the specified device), a message will appear that says the file is not initialized. Type **C** to initialize the fuse map to the unprogrammed state.
3. After typing **C**, editing can begin. Either data or commands can be entered. The logic fuse map may be edited by using the arrow keys to move the cursor to the fuse that you want to change, and then either pressing the space bar to toggle to the desired character or typing in the desired ("0" and "1" or "X" and "-"). The commands shown in the following table are available in the fuse editor:

Note: When you have completed editing the Fuse Map, press **PF1** *to return to the Main Menu or* **PF2** *to return to the fusemap edit LOGIC menu. In general, any page movement command (i.e.* **CTRL -B** *or* **CTRL -N** *or exit command* **PF1** *or* **PF2** *will cause all currently displayed edit data to be written out to the source specified.*

Fuse Editor Commands

Keystroke	Command	Description
Ctrl P	Prev Block	Displays the previous block of fuse data.
Ctrl N	Next Block	Displays the next block of fuse data.
PF2	Exit Editor	Exits the fuse editor.
Ctrl B	Jump to Fuse	Moves the cursor to a specific fuse very quickly. When this command is entered, the cursor will move to the window area next to the "^B: Jump to Fuse" prompt at the bottom of the screen. Enter the fuse number that you want to jump to and press ↵ .
Ctrl U	Restore Block	Returns the current page of fuse data to its original state (before editing that page). Only the data visible on the screen will be effected by this command. This command only works if you have not moved off the currently displayed page of edit data since any changes were made.

Vector Edit

The vector editor allows you to edit test vectors you have created for a particular logic device. The Vector Edit Menu has three parameters that specify information about the test vectors: source, filename and edit begin vector.

- **Source** — Specifies the source of the test vectors that you wish to edit; either RAM or disk. Move the cursor to the Source window. Select the editing source by either using the space bar or by directly typing in **R** or **D**.
- **Filename** — Specifies the name of the disk file from which to take the test vector data. This parameter will not appear if you have selected RAM (R) as your editing source. The Filename must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT".
- **Edit Begin Vector** — Provides a space to enter the number of the first test vector that you want to edit. Move the cursor to the edit begin vector window and enter the desired vector number. The vector number you type in must be less than or equal to the last vector in RAM or the disk file.

To edit test vectors, do the following:

1. After you have specified the three test vectors parameters, press ↵ . This will invoke the vector editor and the screen will display the selected device test vectors.
2. If the data from RAM or the disk file specified on the previous screen does not agree with the device type selected, a message will appear that says the file is not initialized. Type **C** to initialize it.

3. After typing **C**, editing can begin. Either data or commands can be entered. Only certain test conditions may be typed in, and only certain keyboard commands may be used in the vector editor. The test conditions and the allowed commands are listed in the following tables:

Note: When you have completed editing the test vectors, press **PF1** *to return to the Main Menu or* **PF2** *to return to the previous menu.*

Test Conditions

Vector symbol	Description
0	Drives the specified input pin low.
1	Drives the specified input pin high.
2 - 9	Super-voltages, defined by the device's manufacturer.
B	Buried register preload.
C	Drives the specified input with a sequence of logic states, in this case: low, high and low (high clock).
D	A single transistor that drives the specified input low using a fast slew rate; equivalent to "K" without returning to the high state. If more than 16 Ds or Us are used in any one test vector, the exceeding condition will be ignored during test.
F	Specifies that a particular input or output pin is to be floated (tristated).
H	Verifies that the specified output pin is high.
K	Drives the specified input with a sequence of logic states, in this case: high, low, and high (low clock).
L	Verifies that the specified output pin is low.
N	Specifies that a particular input or output pin is floating (tristated). UniSite's "F" and "N" conditions perform the same function.
P	Identifies a preload vector and invokes a preload algorithm. This character is allowed on the clock pin ONLY; otherwise, it is treated as an "X".
U	A single transition that drives the specified input high using fast slew rate; equivalent to "C" without returning to the low state. If more than 16 Ds or Us are used in any one test vector, the exceeding condition will be ignored during test.
X	Ignores the state of an output pin. UniSite will apply a logic level specified by a JEDEC file. "X" field value (1 or 0) or a low is used as the default value.
Z	Verifies the specified input or output pin has high impedance. UniSite will toggle pin using a small current during this test.

Note: C, K, U, and D are clock functions that allow setup time.

Vector Editor Commands

Keystroke	Command	Description
Ctrl B	Jump to Vector	Moves the cursor to a specific vector very quickly. When this command is entered, the cursor will move to the window area just after the "^B: Jump to Vector" prompt at the bottom of the screen. Enter the vector number to jump to and press ↵.
Ctrl D	Delete Vector	Deletes the current vector where the cursor is located.
Ctrl I	Insert Default	Inserts a default vector. The default vector consists of a vector of all "X"s, which is the character that expresses the "ignore input and output" test condition. Use the default vector for creating new test vectors. To create a new test vector, insert a default vector and change that vector to contain the test conditions that you specify; the legal test conditions are listed in the previous table. When you enter this command, the default vector will be placed in front of the vector highlighted by the cursor.
Ctrl N	Next Block	Displays the next block of vectors.
Ctrl P	Prev Block	Displays the previous block of vectors.
Ctrl U	Restore Block	Restores the current page of vector data to its original state (before editing this page began). Only the data visible on the screen will be affected by this command. This command will only be effective if, since any change, there had been NO page movement commands.
Ctrl V	Repeat Saved	Inserts the vector that was last saved using the Ctrl – W Vector command. When you execute this command, the saved vector will be placed in front of the vector highlighted by the cursor.
Ctrl W	Save Vector	Saves the current vector (where the cursor is located) to a temporary buffer.
PF2	Exit Editor	Exits the vector editor and returns UniSite to the previous screen.

Fill Fuse Map

If you select Fill Fuse Map from the Edit Logic menu, UniSite provides you with a screen that will prompt you to enter the variable with which to fill the fuse map. If you are downloading fuse map data into memory, you can use this command to fill any unused portions of the device's fuse map. This operation can also be performed automatically in either of two ways: by using the "F" field in the JEDEC file, or by enabling the Fill memory option on the Communication parameters screen.

1. Move the cursor to the "fill variable" field and enter the desired one-digit value (0 or 1) or toggle the variable by hitting the space bar. "0" represents an unprogrammed state, while "1" represents a programmed state.

2. When the desired fill variable is displayed, press ↵ . This will execute the fill fuse map function, filling the fuse map with the specified variable. When the operation completes, the message "Done" appears.

Clear Vectors

If you select Clear Vectors from the Edit Logic menu, UniSite provides you with a screen that will prompt you to clear the test vectors. To clear vectors, press ↵ .

Note: Only vectors in UniSite's RAM will be cleared. This command cannot be used to clear vectors stored on a disk.

Edit Memory Menu

If you have selected a memory device and then invoke the editing command, UniSite's Edit Memory Menu will appear. This menu contains the Edit Memory, Complement, Move Data and Fill Memory commands.

The Edit Memory Menu allows entry of several parameters that specify information about the data: source, filename, data word-width, edit address offset, and edit begin address. These parameters are described below. Default parameter values are listed in a table at the beginning of this section.

- **Source** — Specifies the source of the fuse data that you wish to edit; either RAM or disk. Select the data source by either using the space bar or directly typing in **R** or **D**.
- **Filename** — Specifies the name of the disk file which contains the data to be edited. This parameter will not appear if you have selected RAM (R) as your data source. This parameter must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:27256.DAT".
- **Data Word Width** — Selects either a 4-, 8- or 16-bit data word width. To select this parameter, move the cursor to the data word width window and type either **4**, **8** or **16**. The space bar can also be used here to toggle between the 4-, 8- and 16-bit options.
- **Edit Address Offset** — Specifies the address you want assigned to the first byte of data in user memory. Using the address offset can save much calculation time on files written on a host system and then downloaded to UniSite. For example, if your host system data file was written using a begin address of 1000H, you could specify an offset of 1000H - edit data would then be displayed on UniSite's screen beginning with address 1000H.
- **Edit Begin Address** — Specifies the first address you wish to edit. Move the cursor to the edit begin address window and enter the 1- to 6-digit hex address. This address must be equal to or greater than the edit address offset. The edit address offset value subtracted from the edit begin address value cannot be greater than the user RAM size.

1. After you have specified the memory editing parameters, press ↵. Depending on the selected word width, either the 4-, 8-, or 16-bit word width memory editor screen will appear.

2. To change data on the screen, move the cursor to the memory location to change and type the new characters over the old ones. Enter the data either in hex or ASCII mode: select the mode using the TAB command (see below). When the cursor is moved around, its location is represented at the top of the screen as a hex address.

Only certain keyboard commands may be used in the memory editor. The allowed commands are listed in the following table.

Note: When you have completed editing, press **PF1** *to return to the Main Menu or* **PF2** *to return to the edit menu.*

Memory Editor Commands

Keystroke	Command	Description
Ctrl B	Jump to address	Moves the cursor quickly to a specific memory edit address. When this command is entered, the cursor will move to the "Jump to address" window area just after the "^B: Jump to address" prompt at the bottom of the screen. Enter the memory address that you want to jump to and press ↵ .
Ctrl D	Delete byte	Delete the entire byte with 8-bit data and the entire word with 16-bit data. (The entire word or byte will be deleted no matter where the cursor is placed within the byte or word.) All the data after the current character position will be moved one address position down. The end of RAM will have an FF inserted. If a disk file is used, the file will get smaller.
Ctrl E	Exchange	Allows you to search for a certain pattern and then replace that pattern with another one: 1. Press Ctrl – E . The cursor will move to the "exchange" prompt at the bottom of the screen. 2.Type in the pattern you wish to search for (any hex value up to 8 digits), followed by ↵ . The cursor will then move to the "with" prompt at the bottom of the screen. 3. Type in the pattern you want inserted in place of the existing pattern, followed by ↵ . If the pattern cannot be found, a message is displayed on-screen and the cursor remains in its original position. When exchange data is entered in 4-bit mode, the upper nibble of data is blank so only up to four characters can be entered in the field.
Ctrl F	Search pattern	Allows you to search for a particular hex pattern of up to 8 digits: 1. Press Ctrl – F . The cursor will move to the "search" prompt at the bottom of the screen. 2. Type in the pattern you wish to search for (any hex value up to 8 digits), followed by ↵ . If the pattern cannot be found, a message is displayed on-screen and the cursor remains in its original position. The search option functions in 4-bit mode. When data is entered, the upper nibble of data is blank so only up to four characters can be entered in the field.
Ctrl N	Next Block	Displays the next block of memory data to edit.
Ctrl P	Prev Block	Displays the previous block of memory data to edit.

Keystroke	Command	Description
Ctrl T	Start/Stop	Toggles the state of the Insert mode.
	Insert	When the "Insert" field to the right of "Start/Stop" is in reverse video, the Insert mode is active. When it is not, insert mode is not active. When Insert mode is active, data input is inserted at the current cursor position in bytes for 8-bit data or words for 16-bit data and all data after the cursor position is moved up into higher memory or file addresses. Data at the end of RAM is lost; if a disk file is used, the file will get larger. The insert will not be complete until the last hexadecimal character (8- or 16-bit) is entered. By disengaging the insert function and moving to the next byte or word before all hexadecimal characters are entered, the previous byte/word is restored. In insert mode, the cursor moves by byte (8-bit data) or word (16-bit data). When not in insert mode, the arrow keys move the cursor by character.
Ctrl U	Restore Block	Returns the currently displayed page of data to its original state (before editing began). The page will only be restored if, since any changes on this page, there had been no page movement commands.
PF2	Exit Editor	Exits the memory editor and returns UniSite to the Edit menu.
Tab	Toggle Hex/	Toggles the mode for data entry. When in hex mode, the ASCII modes data entry is on the left side of the screen and the only valid entries are the hex character set. When in ASCII mode, the data entry is on the right side of the screen and any valid, printable ASCII character can be entered. ASCII code is not allowed when in 4-bit mode.

Complement Data

The Complement function converts each bit of data within the specified block of data to its opposite value (one's complement). The Complement menu allows you to modify two parameters: memory address and block size. These parameters are described below.

- **Memory Address** — The memory address at which the complement operation will begin. The value entered may be any 1- to 6-digit hex address. The address cannot be greater than the user RAM size.
- **Block Size (Bytes)** — The number of bytes (in hex) that will be complemented. Move the cursor to the block size window and enter the block size (from 1 to 6 hex digits). The block size, added to the memory address, cannot exceed the user memory size. After the above parameters have been entered, press ↵ to execute the complement function. "Done" will appear when the operation is completed.

After the parameters have been entered, press ↵ . The Complement data function will execute and the "Done" completion message will appear.

Move Data

The move data function is used to move a block of data from one location to another. There are three parameters to enter in the move data menu: from memory address, to memory address, and block size (bytes):

- **From Memory Address** — The first memory address of the data block you want to move data from. Any 1- to 6-digit hex address may be entered. The address cannot be greater than the User RAM size.
- **To Memory Address** — The first address of the data block you want to move data to. Any 1- to 6-digit hex address may be entered. The address cannot be greater than the User RAM size.
- **Block Size (Bytes)** — The size (in hex) of the data block to be moved. If the sum of the block size and either the "from memory" or the "to memory" address values exceeds user memory size, a warning message will be displayed.

After the parameters have been entered, press ↵ . The Move data function will execute and the "Done" completion message will appear.

Fill Memory

The Fill Memory function fills a specified block of data with a 2-digit hex value. The Fill Memory menu allows modification of three parameters: memory begin address, block size and fill variable. These parameters are described below.

- **Memory Begin Address** — The memory address at which the fill operation will commence. The value entered may be any 1- to 6-digit hex address. The address cannot be greater than the user RAM size.
- **Block Size (Bytes)** — The number of bytes (in hex) that will be filled. Move the cursor to the block size window and enter the block size (from 1 to 6 hex digits). The block size, added to the memory address, cannot exceed the user memory size.
- **Fill Variable** — The 2-digit hex data variable that will be used to fill the specified block. Any value between 00 and FF may be entered.

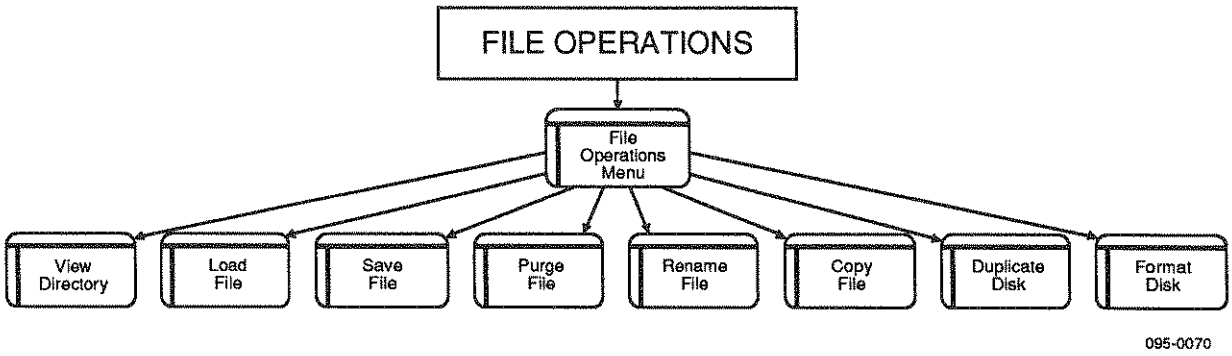
After the above parameters have been entered, press ↵ to execute the fill function. "Done" will appear when the operation is completed.

File Operations

By selecting the File operations command, you can access several file manipulation and directory functions (see the following figure). To access this command, select More commands from the Main Menu, then File operations from the More commands menu.

These functions will help you move and copy files; view file directories, and organize and maintain your disks. The following sections describe each of the File Operation functions in the order that they appear on the file menu screen (refer to the following screen).

Note: To perform File Operations with logic data, the device must first be selected.



The Filename parameter must follow the MS-DOS convention: a specified drive (A: or B:), up to eight alphanumeric characters, followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT".

Note: Remember that you may also use the "" wildcard designation for a filename: for example, typing "COPY 27*.DAT A:" copies BOTH the files 27128.DAT and 27512.DAT.*

A file disk has a capacity of 730K bytes or 112 files, whichever comes first.

View Directory

This command allows you to display the entire file directory of the disk drive(s), If you have two disk drives, the files in drive A will be displayed first. Twenty-eight files may be displayed at one time. If your disk(s) have more than twenty-eight files, they will be displayed on the next page. Press Ctrl – N to advance to the next page.

Load File

This command allows you to load an entire disk file into RAM. The screen will prompt you to type the name of the file you want loaded into memory. When you have typed the filename, press ↵ to execute the command. The entire file is always loaded. Once the disk file is in RAM, you may perform several operations on the file, such as edit or program device; refer to these subsections of the Command section for more information on editing and programming. Note that the User data size field does not appear on the Load file screen. However, this parameter will still be updated to reflect the size of the file loaded for use in other screens.

If you previously selected a memory device from the Load device menu, this screen will also prompt you to specify the beginning address (of the programmer memory) to place the data. The user data size will be automatically set to the file size of the selected file. After typing in the required information, press ↵ to execute the command.

If you selected a logic device, the fuse map and vectors from the disk will be loaded. After typing in the required information, press ↵ to execute the command.

If your files contain data formatted in other than RAM Image Binary (Intel Hex, for example), use the "Transfer data/Input from disk" menu.

Save File

This command allows you to save the RAM user data onto a disk. When the screen prompt appears, enter the name of the file; this may be a new filename or an existing filename that you want to overwrite. If you are writing to an existing file, be aware that the data previously in the file will be replaced by the new data.

If you are saving information for a memory device, you will be prompted for the beginning address and user data size of the programmer memory where the data resides.

If you are saving information for a logic device, only the fuse map, security fuse state, and vectors will be saved.

If you are not sure that you want to overwrite an existing file, name your new file something else. Once you are sure you want to either overwrite an existing file or have named a new file, press [↵] ; UniSite will then write the data on disk.

A saved file is stored in RAM Image Binary format. If you want to store a file in some other format, use the "Transfer data/Output to disk" function.

Purge File

This command allows you to delete files from a disk directory. This is a useful command if you want to delete files that you no longer use to make more room on your data disk for new files.

To purge a file, type the name of the file and press [↵] . Then move your cursor to the next line. This is an added step that offers file protection. If you are sure you want to delete the file, press the space bar to toggle the N (no) to a Y (yes). Press [↵] to start the operation.

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*Note: You may use the "wildcard" * designation to purge multiple files. For example, to purge both the files "27512.DAT" and "27128.DAT", you could type in "27*.DAT."*

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*CAUTION: **If you do not want to delete the file, do not press Return when the Y is displayed. At this point you can either choose another file or exit the purge option by pressing PF1 to get to the Main Menu or PF2 to go back to the previous screen.***

Rename File

To access this command, select More commands from the Main Menu, then File operations from the More commands menu.

If you want to change the name of the existing file on the disk, select Rename file from the File menu. This function is used for taking a previously named data file and changing the file name to more adequately reflect the contents of the file.

Note: You may not rename a file to a different disk drive than the current one displayed on the screen. To change the name of the file, type the name of the file you want to change and the new name for the file at the screen prompts and press Return . The new file will then appear in the directory.

Copy File

Use UniSite's Copy file menu to make a duplicate of a disk file. This operation may be used on either a single- or a dual-drive UniSite. When you use the Copy file menu, you will be prompted for three parameters, described below:

- **Copy File From** — Type in the name of the disk file you want to copy. The filename must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT". Remember that you may also use the "*" wildcard designation for a filename: for example, "copy 27*.DAT" copies both the files 27128.DAT and 27512.DAT.
- **To** — Type in the name of the file to which you want the indicated data file copied.
- **Single Drive File Copy?** — Type **Y** if you are using a single-drive UniSite to do this copy operation, and want the indicated file to be copied to a second disk.

After the parameters are entered, type ↵ to begin the copy operation.

Note: You will be prompted to swap disks when necessary. You may NOT use the wildcard designation if you are using a single-drive UniSite.

For a dual disk drive system:

1. Insert the disk you want to copy (source disk) and the blank, formatted disk into the disk drives.
2. When you are ready, press ↵ to begin the copy operation.

Duplicate Disk

Use this command to copy an entire disk. This feature is useful for creating backup disks.

CAUTION: ***If the destination disk is a UniSite System disk or Algorithm disk, a message will be displayed, as a reminder: because the original contents of the destination disk will be lost when the operation is executed, you will lose all data on that disk. Press Return if you are sure; Ctrl Z will halt the Duplicate operation and you can remove the System or Algorithm disk before it is altered.***

For a single disk drive system:

1. Insert the disk you want to copy (your source disk) into the disk drive. The source disk and destination disk prompts are fixed at A.
2. When you are ready, type **Y** at the "Are You Sure?" prompt, followed by ↵ .

Note: You will be prompted when to swap disks.

For a two-drive UniSite:

1. Insert the disk you want to copy (your source disk) into drive A.
2. Insert the blank disk into drive B.
3. When you are ready, type **Y** at the "Are You Sure?" prompt, followed by ↵ .

You may enable/disable the disk verification procedure at the end of a disk copy operation. If you wish to speed up disk duplication, but potentially be unaware of duplication problems, type **N** in this field. When the screen is entered, and after every disk duplication operation, the default state of the switch returns to "YES".

Format Disk

Use this command to prepare a data disk for use. A disk must be formatted before it can be used.

CAUTION ***If the destination disk is a UniSite System disk or Algorithm disk, a message will be displayed, as a reminder: because the original contents of the destination disk will be lost when the operation is executed, you will lose all data on that disk. Press Return if you are sure;*** **Ctrl Z** ***will halt the Format operation and you can remove the System or Algorithm disk before it is altered.***

Use the following procedure to format a UniSite disk:

1. Insert the disk to be formatted into either disk drive.
2. Press the space bar to change the drive that the new disk will be in when formatting. For single disk drive systems, you are restricted to drive A.
3. When you have specified the drives to be used and are ready to format the disk, type **Y** at the "Are You Sure?" prompt.
4. If you want UniSite to perform a disk integrity check while the disk is being formatted, move the cursor down and type **Y** at the "Disk Integrity Check" prompt. This test looks for bad sectors by writing hex test patterns to the disk. These patterns are then read back and if they do not match, those sectors of the disk are locked out (they cannot be accessed).
5. Press [↵] when you are ready to format the disk.
6. UniSite will then check the installed disk to make sure it is not a System disk. If it is, a warning message will appear: press [Ctrl] – [Z] to abort the operation, [↵] will format the System disk.
7. After the disk has been formatted, every sector of the disk will be verified by a Read operation. A "Done" message will then appear, indicating that the operation is completed.

Job File

Using UniSite's Job file feature, you can record a series of keystrokes which can then be "replayed." Job files allow you to perform setup or programming operations without having to re-key in all the parameters each time a new device is selected. For example, if you regularly program five different devices, you could have five different job files on disk, each with that particular device's specified options.

You may store up to 10 job files on each UniSite System disk. Each job file may contain up to 499 keystrokes, although most contain 15 to 20 keystrokes. Job files are listed on the File operations/ View directory screen as "JFN.JOB" files (N is a number between 0 and 9). For example, if you have three job files on a disk, they may show up as JF0.JOB, JF4.JOB and JF8.JOB. If you have job files on another disk, insert the disk and press PF4 to display the job file directory for the current disk. Whenever you change disks with job files on them, pressing PF4 will display the current job file directory.

Because UniSite's Job files function does NOT stop and prompt the user until the file has been completely played back, you should not imbed any Quick copy commands in the Job files you write. For the same reason, your Job files should also not include any operations that require insertion/removal of a disk or module.

Note: Because screens may change when the software is updated, a particular job file may only be used with the version of software it was created with. For example, if you created a job file with one version of software, it would need to be re-created in order to work with the next version of software released.

To start recording keystrokes, press [Esc] [Ctrl] – [J] . When you have entered all needed keystrokes for the job file, press [Esc] [Ctrl] – [J] again. The following procedure shows how to record a job file:

1. Go to the menu where you want to begin recording keystrokes.
2. Press [Esc] [Ctrl] – [J] to start recording the job file. Each keystroke entered from now on will be recorded into a file.
3. Type in all the parameters you want recorded. For example, you might want to select a certain device and then choose its programming parameters, by using the Select device and Program device menus.
4. When you have entered all the needed keystrokes, press [Esc] [Ctrl] – [J] again. The Job file screen will appear.
5. Type in a number that will correspond to the file just created, followed by [↵] . For example, if you want this file to appear as file number five on the Job Files screen, press 5 [↵] .
6. Move the cursor down to the "enter description" area and type in a name for the file that has just been recorded. Type in the description up to 31 characters, followed by [↵] . For example, you could type **27128 Device.** The job file is now saved. The last screen accessed during job file recording will now be displayed.

If you try to give a job file a name that already has been used, UniSite will prompt you to either press [↵] to overwrite the existing file, or [Ctrl] – [Z] to preserve the existing job file.

To play back a job file, do the following:

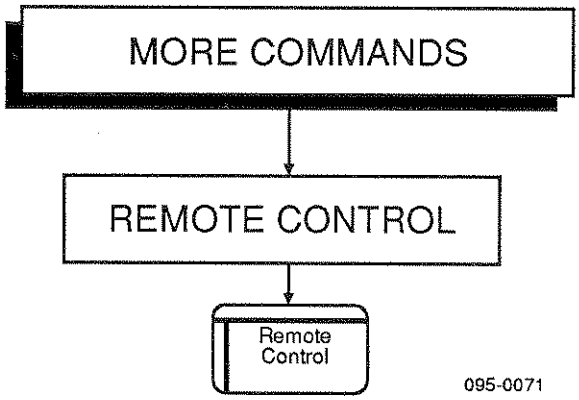
1. Go to the Job Files screen, by pressing [PF1] [M] – [J] (Main Menu/More commands/Job file).
2. Select the job file you want to play back, and then press [↵] . For example, to play back the fifth file on the list, press [5] [↵] .
3. UniSite will now "play back" the keystrokes that were recorded. Each screen that was displayed while you were recording keystrokes will now be shown (briefly).

4. When the job file has been played back, the message "Jobfile playback ended" will appear. The last screen that was recorded while you were creating the job file is now displayed. If an error occurs while the job file is playing back, an error message will be displayed and the job file will need to be restarted.

Remote Control

When you have selected Remote Control, as shown by the following command tree excerpt, the Remote control screen will appear. You will use this function when you want to control UniSite from a remote computer. The Getting Started section in this manual gives complete cable hookup procedures. See the Computer Remote Control section of this manual for more information on operating UniSite in remote mode.

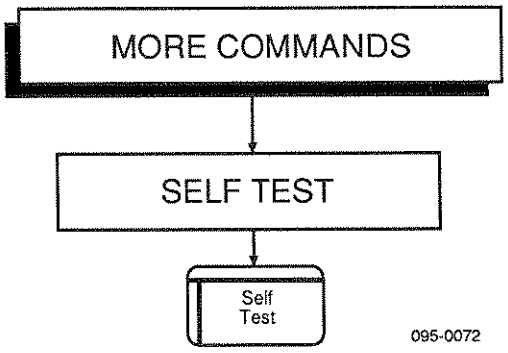
You may exit remote control by either typing [CTRL] – [Z] on the terminal's keyboard, or sending a [Z][↵] command from the host.



Self-Test

The self-test command allows you to test various UniSite systems, in order to verify proper operation or isolate problem areas. To access this command, select More Commands from the Main Menu. When the More commands menu appears, type [S] to display the self-test screen.

An automatic self-test is also performed each time UniSite is powered up. If any errors occur during this power-up test, the self-test screen will be displayed, showing the areas that failed. The following paragraphs describe the self-test feature.



Note: For details (help) on the function of each self-test, move the cursor to the test you want information about and press PF3 *or* ? .

Running the Self-Test

To use the self-test feature, do the following:

1. Make sure all device sockets are empty. From the More commands menu, type S to select the Self-test. The Self-test screen will then appear.
2. Select the test mode you want: move the cursor to the bottom of the screen to the "test mode" prompt. Select either "one pass" or "continuous" testing by using the spacebar to toggle between the two choices. "One pass" testing will run the specified test once; "continuous" testing will run the specified test until you halt the procedure by pressing Ctrl Z . There may be a long delay before the system RAM test responds to the Ctrl – Z to abort the operation.

CAUTION ***The System RAM test and User RAM test, if executed, will cause any data in user RAM to be lost.***

3. If you want to test all hardware, move the cursor to the "Perform All Tests" prompt and press ↵ . If you want to select a particular test, use the arrow keys to move the cursor to the desired test and press ↵ .

Interpreting Self-Test Results

Four conditions are used as status indicators on the self-test screen:

```
PASS (P)   UNTESTED (?)   FAIL (F)   NOT INSTALLED (-)
```

When testing begins, a question mark appears next to the areas that have not yet been tested. If a certain hardware item is not installed, a "-" symbol appears. For example, if you are testing Pin Driver boards on a UniSite that has ten boards installed (UniSite can hold 17), ten "?" and seven "-" symbols will appear. As each test completes, either "PASS" (P) or "FAIL" (F) messages will appear next to the system prompt, showing the results of the test performed.

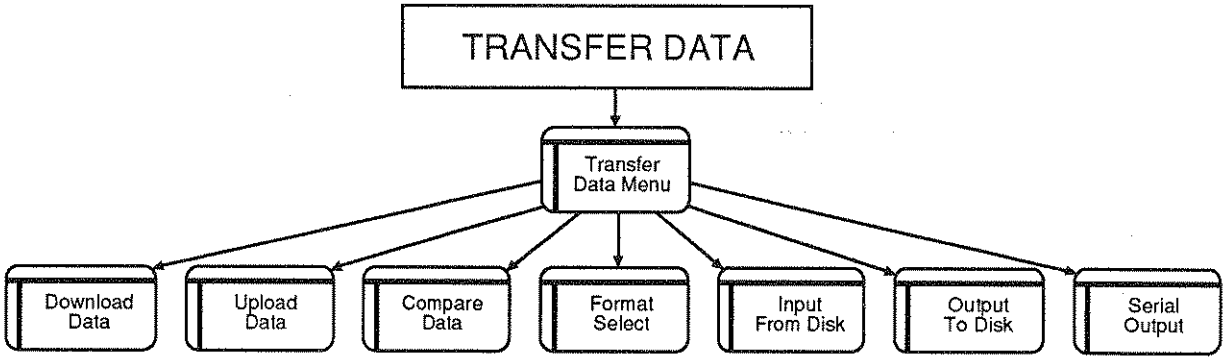
During testing, the message area of the self-test screen will indicate that testing is in progress. During the System RAM test, the Remote and the Terminal indicators will blink to indicate that testing is in progress. If, when the testing has completed, "?" symbols still appear next to some systems, it may be because some other test(s) need to pass before the indicated one may be tested. For example, the Waveform board test must pass before the Pin Control Unit test executes. All the installed UniSite hardware must pass self-test.

Transfer Data

Use this command to move data files back and forth between UniSite and the host computer.

The Transfer data command consists of the following seven screens: Download data, Upload data, Compare data, Format select, Input from disk, Output to disk, and Serial output.

The following illustration from the command tree shows the path to the screens that make up the Transfer data menu. Each of these screens are in this subsection.



Download Data

Use the Download data screen to specify downloading parameters and to execute the download operation. Downloading is an operation that moves a data file from a host computer to UniSite's RAM or disk.

To perform this operation specify the variables for each of the following parameters, enter a command line in the blank space under "Download host command". The information in the command line is a command that your host computer will recognize as an instruction to begin the download operation. Press [↵] to execute this command. The message "Data transfer complete" will appear in the message area of the screen when the operation is complete.

- **Source** — Specifies which port your host computer is connected to. Pressing the space alternates the variable between R (remote port) and T (terminal Port).
- **Destination** — Choose RAM or Disk to be the destination of the data that is being downloaded from the host computer.
- **Filename** — If you selected Disk as the destination of the incoming data you will create a file on that disk. To do that you need to give it a name. Enter that name into the highlighted area next to "Filename".
- **I/O Translation Format** — Select the data translation format your host computer is using. A list of formats that UniSite supports is available in the Format select screen in the Transfer Menu. If you know the number for your format, you can enter it from this screen. If you do not know the correct code number, go to the Format Select screen, find the format you want and enter the correct number from that screen. Entering the format number from the Format Select screen changes the Translation Format parameter on this screen. (If you are using the POF format, you must select the desired POF device before you perform a data transfer operation.)
- **I/O Addr Offset** — This field will only appear when a non-JEDEC format has been selected. Enter the beginning address of the host computer's data in this space. UniSite will subtract this address from addresses received to determine where, either in the user RAM or in the disk, the data will be loaded. A "FFFFFFFF" will set the first address received as the I/O offset for the rest of the download.
- **Memory Begin Address** — The Memory begin address defines the first address, in hex, to where the first byte of data is stored from the source port. If the destination is RAM, it is a beginning RAM address. If the destination is Disk, it is a beginning disk file address. The default address is 0.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block to be downloaded to the destination from the Source. The default User data size is 0, so that all of the data will be received. After the download is complete, a value equal to the number of bytes received will be set here. If a value less than the size of the data received is entered, only the number of bytes equal to that value are actually stored.

- **Download Host Command** — Enter the appropriate host command line here to download the data. This line may be up to 58 characters long. UniSite will generate a return character to terminate the line when transmitted to the host. Entering a blank command (by pressing first the spacebar then ↵) will suppress the transmission of anything prior to download.

Upload Data

Use the Upload Data screen to specify uploading parameters and to execute the upload operation. Uploading is an operation that moves a datafile from UniSite's RAM or disk to the host computer.

To perform this operation, specify the variables for each one of the following parameters, then enter a command line in the blank space under "Upload host command". The information in the command line is a command that your host computer will recognize as an instruction to begin the upload operation after a ↵ is received. Press ↵ to execute this command. The word "Done" will appear in the message area when the operation is complete.

- **Source** — Specifies where the data to be uploaded is located, RAM or Disk. Pressing the space bar toggles between the two choices.
- **Filename** — Enter the filename of the data to be transmitted if data source is disk.
- **Destination** — Specifies through which port the data will be sent, Remote (R) or Terminal (T). Press the space bar to select the port that is connected to the host computer.
- **I/O Translation Format** — The format specified here must be the same as is expected by the host computer that is to receive the data. A list of formats that UniSite supports is available on the Format Select screen in the Transfer menu. If you know the format number for your translation format, you can enter it from this screen. If you do not know the correct format number, go to the Format Select screen. Find the format you want and enter the correct number from that screen. Entering the format number from the Format Select screen changes the Translation Format parameter on this screen.
- **I/O Addr Offset** — This field only appears if a non-JEDEC format has been selected. This value will be added to the address of the data in memory (relative to the Memory begin address) and output as the I/O address. A value of "FFFFFFFF" will cause the I/O offset to be 0.
- **Memory Begin Address** — The Memory begin address defines the first address, in hex, from where the first byte of data is retrieved. If the source is RAM, it is a beginning RAM address. If the source is Disk, it is a beginning disk file address. The default address is 0.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block to be uploaded to the destination from the Source. Enter the value of the number of bytes to upload. If a zero is entered here, User data size will be set to the total number of hex bytes in the UniSite User RAM or the size of the disk file if disk is used as Source.

- **Upload Host Command** — Enter the appropriate host command line here to accept the uploaded data. This line may be up to 58 characters long. UniSite will generate a return character to terminate the line when transmitted to the host. Entering a blank command (by pressing the spacebar then ↵) will suppress the transmission of anything prior to upload. If a delay between the host command and the file transmission is required by the host, use the "upload wait" feature on the communication parameters screen.

Transmit Pacing

Transmit pacing provides a time delay between characters sent to the host by UniSite. This delay affects data that is uploaded from UniSite, as well as host commands sent by UniSite. If errors are encountered during upload operations to a host, the transmit pacing delay feature may be used to eliminate the errors. This will provide a character by character delay to prevent data overrun on the host. This type of condition may exist in spite of the use of hardware and/or software handshaking on the host and UniSite. This condition is most likely to occur on hosts which aren't able to accept incoming data fast enough at high baud rates.

Your host may not explicitly report any error, so one way to determine if errors are occurring during an upload process is to transfer data to the host using the upload function with an I/O format selected which utilizes checksums (such as Format 87). Note the checksum reported by UniSite when the transfer is complete. Then transfer the same data back to the UniSite while the UniSite is performing the compare data function, again noting the checksums. If the checksums don't match or if an error is encountered, a transmit pacing delay should be used.

Typical delay values are presented in the following table. The transmit pacing value is specified in tenths of milliseconds delay. For example, a value of 12 represents 1.2 milliseconds delay. The minimum delay possible (other than zero) is 4 (.4 milliseconds) and the maximum is 99 (9.9 milliseconds). The factory default is 0. The transmit pacing value required for reliable data transfers may vary somewhat from those presented in the table due to the particular characteristics of the host involved. This is primarily determined by the processor speed of the host and whether or not software other than the communication software is running at the same time on the host (in the latter case larger delay values may be required). Transmit pacing is selected on the More/Configure/Communications parameters screen.

Transmit Pacing Delay Values

	4800 and less	9600	19.2KBD
VTERM RUNNING ON			
IBM PC (4.77 MHZ)	0	4	15
IBM AT (6MHZ)	0	0	8
PROCOMM RUNNING ON			
PC	0	4	9
AT	0	0	6
TERM-100 RUNNING ON			
PC	0	0	6
AT	0	0	6

Compare Data

Use the Compare data screen to specify the compare parameters and to execute the operation. Compare data is an operation that compares the data that is in user memory with the datafile in the host computer. The current I/O format is used to translate the incoming data from the serial port. (Jedec format cannot be used with this command.) This operation is identical to a downloading operation, except data is compared rather than written to memory.

To perform this operation, specify the variables for each of the following parameters and then enter a command line in the blank space under "Download host command". The information in the command line is a command that your host computer will recognize as an instruction to begin the download operation. Press ↵ to execute this command. The message

```
Data transfer complete
```

will appear in the message area when the operation is complete.

If memory data does not correspond with the host's data, the screen will display the following message:

```
compare fail at AAAAAA:XX not YY
```

"AAAAAA" is the address, "XX" is the memory data and if the terminal is not on the same port as the port receiving the data from the host, "YY" is the host's data.

If the terminal is on the same port, then the following messge will be displayed:

```
Data verify error. Data sum = ssssssss
```

- **Source** — Specify which port is connected to the computer with the datafile that is to be used to compare with the memory data. Pressing the spacebar alternates the variable between R (remote port) and T (terminal port).
- **Data Location** — Select either RAM (R) or disk (D). This selection specifies where the data to be compared is located.
- **Filename** — Enter the name of the file you want compared (if you selected the data location to be the disk).

- **I/O Translation Format** — This parameter allows you to select the format of the data to be verified. A list of formats that UniSite supports is available from the Format Select screen in the Transfer menu. If you know the number for your format, you can enter it from this screen. If you do not know the correct format number, go to the Format Select screen, find the format you want, and enter the correct format number from that screen. Entering the format number from the Format Select screen changes the Translation Format parameter on this screen.
- **I/O Addr Offset** — Enter the beginning address of the downloaded data to be compared. FFFFFFFF causes UniSite to default to the first incoming address as the lowest address to be compared.
- **Memory Begin Address** — The memory begin address defines the first address, in hex, to where the first byte of data from the RAM or Disk is compared to data from the Source port. If the data location is RAM, it is a beginning RAM address. If the data location is Disk, it is a beginning disk file address. The default address is 0.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block to be downloaded and compared from the Source to the data location. Normally, a zero should be entered here so that all of the data will be compared. After the compare is complete, a value equal to the number of bytes compared will be set here. If a value less than the size of the data received is entered, only the number of bytes equal to that value are actually compared.
- **Enter Host Command** — Enter the appropriate host command line here to download the data. This line may be up to 58 characters long. UniSite will generate a return character to terminate the line when transmitted to the host. Entering a blank command (by pressing the spacebar, then ↵) will suppress the transmission of anything prior to download and compare.

Format Select

This command allows you to select the type of transmission protocol used when uploading/downloading data between UniSite and the host computer. Only the formats listed in the Translation format section of the manual are recognized by UniSite; if your host computer does not generate code into one of the listed formats, you will need to edit it to match one of the formats.

The Format Select screen displays a list of all UniSite supported formats to choose from. At the bottom of this screen is a format entry field. Enter the format number of the format that you want to use and press ↵ . Entering the format from this screen causes the same format to be entered in all of the other Transfer screens.

Input From Disk

Use this feature if you want to translate formatted data from a disk file into RAM or to another disk file, using one of Data I/O's supported translation formats. This operation is just like the Download data function (also on the Transfer data menu), except that the data is input from a disk file rather than through a port. The following parameters appear on the Input From Disk File With Translation screen:

- **Input Filename** — Specify the name of the disk file from which formatted data will be taken. The Filename parameter must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three- character file extension, with the two fields separated by a period. An example of a valid filename would be "B:27256.HEX".
- **Destination** — Select the destination for the translated data, either RAM (R) or another disk file (D).
- **Filename** — Specify the filename for the disk file into which data will be sent. The field is displayed only if D is selected as the destination.
- **I/O Translation Format** — Specify the translation format number for the data to be input. A complete listing of the formats is given in the Translation Formats section of this manual.
- **I/O Address Offset** — This field appears only if a non-JEDEC format has been selected. Enter the beginning address of the disk's data. UniSite will subtract this address from addresses received to determine where the data will be loaded. An "FFFFFFFF" will set the first address received equal to the I/O offset.
- **Memory Begin Address** — The Memory begin address defines the first address, in hex, to where the first byte of data is stored in user memory. If the Destination is RAM, it is a beginning RAM address. If the Destination is Disk, it is a beginning disk file address. The default address
  is 0.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block to be input, with translation, from the input file to the destination. The default User data size is 0 so that all of the data will be input. After the input is complete, a value equal to the number of bytes input will be stored here. If a value less than the size of data input is entered, the number of bytes equal to that value are actually stored.

When all parameters have been entered, press [↵] to begin the transfer.

Output To Disk

Use this feature if you want to encode binary data from a disk file or RAM to another formatted disk file, using one of Data I/O's supported data translation formats. This operation is just like the Upload Data function (also on the Transfer Data menu), except that the formatted data is sent to a disk file rather than through a port. The following parameters appear on the Output To Disk File With Translation screen:

- **Source** — Select the Source for the disk file data, either RAM (R) or another disk file (D).
- **Filename** — Specify the name of the disk file from which the data will be taken. The field is displayed only if **D** is selected as the Source.
- **Output Filename** — Type in the name of the disk file you want the formatted data sent to. The Filename parameter must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three- character file extension, with the two fields separated by a period. An example of a valid filename would be "B:27256.HEX".
- **I/O Translation Format** — Specify the translation format number for the data. A complete listing of the formats is given in the Translation Format section of this manual.
- **I/O Address Offset** — This field appears only if a non-JEDEC format has been selected. Enter the desired beginning address of the disk's data. UniSite will add this value to the address of the data in memory (relative to the Memory begin address) and output as the I/O address. A value of "FFFFFFFF" will cause the I/O address offset to be 0.
- **Memory Begin Address** — The Memory begin address defines the first address, in hex, from where the first byte of data is retrieved to write to the disk output file. If the Source is RAM, it is a beginning RAM address. If the Source is Disk, it is a beginning disk file address. The default address is 0.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block to be output, with translation, to the output file from the Source. Enter the value of the number of bytes to output. If a zero is entered here, User data size will be set to the total number of hex bytes in the UniSite User RAM or the size of the source disk file if disk is used as Source.

When all parameters are entered, press ↵ to begin the transfer.

Serial Output

This command allows you to send data from UniSite to a printer or other peripheral device. Use this command as a useful way to obtain a quick copy of programming or other device-related data. Serial output does not do any data translating. If a logic device is selected, the fuse data will be output by fuse number and the vectors will be output by vector number. If a memory device is selected, the data will be output by address in hex format.

Output Memory Data to Serial Port (Memory Device Selected)

- **Source** — Select the source for the data, either RAM (R) or disk file (D).
- **Destination** — Select the destination for the data, either Remote (R) or Terminal (T).
- **Filename** — If a disk is the source,type in the name of the disk file. The Filename parameter must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:21128A.DAT".
- **Number of Lines Between Form Feeds** — Specify the number of printed text lines you wish to have per page. The default is 0 (no form feed).
- **Memory Begin Address** — The Memory Begin Address defines the first address, in hex, from where the first byte of data is retrieved to send out the serial port. If the Source is RAM, it is a beginning RAM address. If the Source is Disk, it is a beginning disk file address. The default address is 0.
- **User Data Size** — The User data size defines the hexadecimal size, in bytes, of the data block to be output to the Destination from the Source. Enter the value of the number of bytes to output. If a zero is entered here, User data size will be set to the total number of hex bytes in the UniSite User RAM or the size of the source disk file if the disk is used as the source.

When all parameters have been entered, press ↵ to begin the transfer operation.

Output Logic Data to Serial Port (Logic Device Selected)

- **Source** — Select the source for the data, either RAM (R) or disk file (D).
- **Destination** — Select the destination for the data, either Remote (R) or Terminal (T).
- **Filename** — If a disk is the source, type in the name of the disk file. The Filename parameter must follow the MS-DOS convention: an optional drive (A: or B:), up to eight alphanumeric characters followed by an optional three-character file extension, with the two fields separated by a period. An example of a valid filename would be "B:16R8.DAT".
- **Number of Lines Between Form Feeds** — Specify the number of printed text lines you wish to have per page. The default is 0 (no form feed).
- **Starting Vector Number** — Type in the decimal number for the first vector to be output. (Default 1, first vector.)

- **Number of Vectors** — Type in the total decimal number of vectors you wish to output. (Default 0, no vectors.)

When all parameters are entered, press [↵] to begin the transfer.

Transparent Mode

Transparent mode can be entered from all of the UniSite screens with the following exceptions:

- Editor screens
- Under/over-blow screen
- Yield Tally screen
- Help screens
- CRC mode

Transparent mode allows the user to communicate with a host computer connected to the remote port. This mode causes the terminal connected to the terminal port of UniSite to act as if it were connected directly to the host computer. This mode is useful for establishing communication with the host (such as logging in, executing commands, etc.).

This mode is entered and exited by typing [Esc] [Ctrl] – [T] from the terminal. Transparent mode does not support binary data transfers (this can be done via the upload and download commands using one of the binary data formats).

In transparent mode all key strokes entered on the terminal will be passed on directly to the host with one exception. The [Esc] character is stripped out since it represents a special meaning to UniSite (it is part of the Exit Transparent Mode Command). To send an [Esc] character to the host, enter two consecutive [Esc] characters (the second one will be passed on to the host), or if [Esc] is followed by some character other than a [Ctrl] – [T] , the escape and the character will be sent on to the host.

Yield Tally

UniSite's Yield Tally function allows you to maintain programming information on devices that have been programmed. This information can be very useful in a manufacturing environment where device yield statistics must be kept. Yield statistics are maintained on the last 16 devices that have been programmed. If you attempt a yield tally on a 17th device, UniSite will drop the oldest device statistic. UniSite stores the manufacturer name and its part number or family/pinout codes as the device name in the yield tally record.

The yield data is stored on the algorithm disk, in a file called "YTALLY.YTL". If the file does not exist on the disk, enabling the Yield Tally option will create a blank copy of this file on the disk.

Note: You may upload the yield statistics while in CRC mode by using extended command "43]". The CRC extended command 46]" will clear the yield tally statistics. These commands and their formats are described in the Computer Remote Control section of this manual.

Space is allocated for the Yield Tally data files on the Algorithm disk for both single and dual drive systems. The Algorithm disk may be in either drive for a two drive system. When the Yield Tally function is invoked without the Algorithm disk, the error message:

```
Algorithm disk not found
```

will be displayed on the terminal or the CRC mode will fail with error code 9A.

Yield Total

The Yield total does not include those devices with error conditions that are not recorded in one of the four categories: illegal bit, mis-verify, device not programmable, structured test fail. Examples of these conditions are continuity check, electronic ID error, or overcurrent.

The Yield Tally screen provides statistics for the following categories:

- **Device Name** — Manufacturer's name and part number, family/pinout codes. The last sixteen device types' statistics are kept.
- **Total Count** — The number of individual devices (having the same name) that UniSite attempted to program.
- **Good Part** — The number of devices that were successfully programmed.
- **Illegal Bit** — The number of devices that failed because they did not pass non-blank test or illegal bit check.
- **Verify Fail** — The number of devices that failed because they did not verify.
- **Struct Fail** — The number of logic devices for this device name that failed the logic structured vector test.
- **Device Not Programmable** — The number of devices that could not be programmed because they contained bits that required more programming pulses than were specified.

In the case of the non-blank test, if you abort the operation without programming the device, the illegal bit count will be incremented by one. If you proceed with the programming operation, the illegal bit count remains unchanged while the yield tally records the result of the programming operation. To erase the entire set of statistics, press Ctrl – E . Press PF2 to go to the previous menu or PF1 to return to the Main Menu. The total number of programming errors is not recorded. This value may be derived by adding the values in the individual error columns.

4 Messages

Introduction

This section lists and describes the terminal status messages that appear on UniSite screens and UniSite System messages. Some messages require some action from the operator; instructions for those actions are included in the message's description. All of the messages are listed in alphabetical order. Error messages appear on the UniSite screen and their descriptions are available by pressing PF3 (help).

Note: The use of "PSM," (Package Specific Module) and "FSM," (Function Specific Module) in this section refers to the modules that are installed on UniSite's front panel. The PSM is the small socket module located on the left side of the top panel; the FSM is the optional, large module on the right.

Note: Because UniSite provides online help for most system error messages, these are not included in this section of the manual.

Terminal Status Messages

0 div err	UniSite has experienced a divide-by-zero error that it cannot recover from. This is a fatal error; turn UniSite off and reboot the system. If the error recurs, contact the Data I/O Service Center.
Addr err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.
Address out of range	The address you tried to select is beyond the selected device's range. Select an address that is within the limits of the device or select a different device. This message appears while you are in the memory editor, fuse editor, or using the under/overblow feature.
ASCII entry not allowed in 4-bit mode	This message appears in the memory editor when attempting to go into ASCII entry mode when a 4-bit device is selected. Re-select device or edit in hex mode only.
Beginning of file	This message appears when you are using the memory editor, vector editor, fuse editor, or using the under/overblow feature, and you press Ctrl – P (previous page) when the first block is already being displayed.
Begin address too large	The beginning address you selected in the memory editor was too large and is beyond the limits of the selected device. Change the begin address to one within the device's range.
Booting non-system disk. Insert system disk. Type ESC and CTRL W to reboot.	This message will appear if UniSite detects a disk other than the System disk installed in drive A during power up. Insert the System disk.
Bus err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact the Data I/O Service Center.
Bytes copied = nnnnnn	This message appears while the Copy File operation is in progress; "nnnnnn" refers to the number of bytes copied.
Cannot access system disk	This message indicates a non-system disk is installed. Insert the correct system disk.
Calculating sumcheck	This message appears when you are using the Device Check's Sumcheck screen, informing you that the RAM sumcheck is being calculated.

[Computer Remote Control: enter Control-Z to exit].	This message informs you that Unisite is now in remote control mode and all programmer commands are now read from the remote port. Typing CTRL - Z returns control to terminal mode.
Constant over-current fault	This message indicates that an over-current condition exists and UniSite is unable to clear the condition. The over-current could be caused by a hardware failure in UniSite. Reboot the system and if the condition persists, contact a Data I/O Service Center.
Constructing Job File Directory	The job files are now being read, in order to put together a job file directory. You can then select one of the files for playback.
Copying file1.ext to file2.ext. Bytes copied = xxxx	This message appears during a Copy operation if you are using the wildcard ("*") designation. "xxxx" in the display is the number of bytes copied into the destination file.
Copying sectors ssss - ssss+120 Reading source disk	This message appears while the Disk Copy command is proceeding. The information presented in this message displays the number of sectors copied in each pass. There are 1440 sectors on each disk. This message is accompanied by the message "Copying sectors ssss - ssss Writing destination disk" which appears while UniSite is writing data onto the destination disk.
Copying sectors ssss - ssss+120 Writing destination disk	This message appears during the Disk Copy routine, indicating that the data is being copied.
Could not initialize default system parameters from disk	When UniSite was booting up, the default and programming system parameters could not be loaded. Reboot UniSite with a different system disk, or call your nearest Data I/O Service Center for assistance.
Data transfer complete.	This message appears after a data transfer with an external source was successfully completed.
Data transfer complete. Data Sum = ssssssss	After a data transfer, this message appears. The data sum represents the calculated checksum for the data bytes transferred.
Data transfer complete. Data Sum = ssss. Xmit = ssss.	After a data transfer of a JEDEC file, this message appears. The data sum represents the calculated checksum for the data bytes in the fusemap section of the data transferred. The Xmit sum represents the calculated checksum for all the bytes transferred.
Data operation complete: data saved on disk	After a datafile is downloaded to disk, this message appears.
Destination file already exists. Hit return to continue, ^Z to abort.	The filename that you have designated as the destination for the data already exists, so existing data will be written over if you execute the operation. This is a precautionary message which occurs on any file operation which could overwrite an existing file.

Disk boot err	UniSite has experienced an error that it cannot recover from. Turn UniSite off and reboot the system. If the problem persists, use another copy of the System disk.
Disk data error	The read or write operation that was attempted could not be completed because there is a problem with the disk; try the operation again with a different disk.
Disk error, terminal type not saved!	If you try to save the terminal type as one of the power-up parameters and there is a write problem with the disk (the disk is either full or is defective), this message will appear.
Disk write-protected, terminal type not saved!	If you try to save the terminal type as one of the power-up parameters and the disk is write-protected, this message will appear. Move the write-protect slide so that the hole through the disk is blocked.
Done.	The operation is completed. Proceed to the next operation you want to perform.
Done. Bytes copied = nnnnnn	This message appears after the Copy File operation is complete. It displays the size of the file that was copied in hexadecimal bytes. Proceed to the next operation you want to perform.
End of file	When you are using the memory editor, vector editor, fuse editor, or the over/under blow feature, this message will appear if you press Ctrl – N (next page) when the last block of data is already being displayed.
Fatal system err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact the Data I/O Service Center.
FILE ERROR: Can't reach track 0.	If this message appears, a fatal disk error has occurred. The disk drive may be faulty. Contact a Data I/O Service Center for assistance.
FILE ERROR: Error in sector preamble.	This error appears when UniSite detected an error with the format of a disk. Use a different disk or reformat the existing disk and try the operation again.
FILE ERROR: No disk in drive	This message appears if UniSite is trying to access a disk file but the disk drive is empty. Insert the disk with the file to be used.
FILE ERROR: source file does not exist	This message appears during the Copy File operation, if the file that you want to copy is NOT on the disk installed in the disk drive. Insert the disk that has the source file into the disk drive and attempt the operation again.

FILE ERROR: Track not found.

This message appears if UniSite cannot find the disk track associated with the system file, or cannot find the data needed to support whatever action you just requested. If you try the operation again and the error message reappears, a new disk (or a new copy of whatever software or data the unit needs) must be used.

File not initialized! Enter 'C' to initialize, any other key to quit

This message appears within the fuse editor , vector editor or when the under/overblow feature is selected. The file that you have selected is not in a format that is compatible with the feature that you want to use. If you want to use the fuse editor, and the data file you have is not formatted for the device you have selected, typing [C] will reformat the data file to be compatible with the device.

Formatting and initializing user disk.

This message appears while a disk is being formatted.

Hit PF3 or ? to view device specific message

The selected device has specific information associated with it.

Hit return to continue, ^Z to abort.

This message appears after a Verify operation has failed. If you want to ignore the warning (not check out the errors) and proceed with the operation, press [↵] . If you want to investigate the errors, press [Ctrl] – [Z] and the Verify screen will reappear.

Hit return to switch user menu port, ^Z to abort.

This message is displayed whenever the parameter to change User Menu Port is toggled by the user. If the user wishes to cancel the port switch operation he should enter a [Ctrl] - [Z] at this time; otherwise entering a [↵] will cause the programmer to switch the port. The cable between the programmer and the PC (or terminal) should then be moved to the port specified by the parameter.

IOX init err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Illegal instr err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system.

Illegal Key Input: Type control-Z to abort parameter entry.

You pressed a key that is illegal for the field where the cursor is positioned. For example, if you type in a hex number for the "Data word width" field (only decimal numbers are allowed), this message will appear.

Illegal terminal type!

The terminal type number you entered was not one of the choices presented on the Terminal Type screen. Type in a valid terminal type number.

Insert blank device. Hit return.

This message appears during the Quick copy mode operation. Remove the newly programmed device or the master device from the device socket, place a blank device in the socket and press [↵] . UniSite will then begin programming the blank device with RAM data loaded from the master device.

Insert destination disk in drive A. Hit return to continue.

This message appears during the Duplicate disk or a Copy file operation, when a UniSite with one disk drive is being used. When this message appears, remove the source disk, insert the destination disk (the disk where you want the data to go to) and press [↵]. Make sure to use a formatted disk: if you insert an unformatted disk, UniSite will abort the operation and display "Sector not found". If this occurs, perform the Format disk operation and restart the Duplicate disk or Copy file operation.

Insert master device. Hit return to continue

This message appears during the Quick copy operation. Place the master device into the device socket, lock it into place, and press [↵]. UniSite will then start to load RAM with data from the master device.

Insert blank device. Hit return to continue or push START lever forward

This message appears during the Quick copy operation if you are using the SetSite module. Place the blank devices into the SetSite sockets, lock them into place and press [↵] or move the socket lever to the START position. UniSite will then start to program the parts with data from RAM.

Insert master device. Hit return to continue or push START lever forward

This message appears during the Quick copy operation if you are using the SetSite module. Place the master device into device socket number one, lock it into place, and press [↵] or move the socket lever to the START position. UniSite will then start to load RAM with data from the master device.

Insert source disk in drive A. Hit return to continue.

This message is a prompt that appears during the Duplicate disk operation if you are using a UniSite with a single disk drive. When this message appears, remove the destination disk from the disk drive, insert the source disk and press [↵].

Job file playback ended.

This message informs you that a job file's playback has ended and you may continue with the operation where the job file left off.

Job file save aborted. Keystrokes not recorded.

This message appears in the following situation: If you attempt to end job file recording, and either the system disk is not in the drive or UniSite has difficulty reading the disk, an error message will appear. If you press [Ctrl] - [Z] after seeing that message, the above message will appear.

Keystroke recording ended. Select job file for saving.

This message appears after you have pressed [Esc] [Ctrl] – [J] a second time to end recording keystrokes for a job file. Specify a job file number, by typing a number between 0 and 9. Then type in a job file description, such as "27128.DAT".

Keystroke recording for job file has begun.

After you press [Esc] [Ctrl] – [J] once, this message will appear. You are now in the job file record mode: every keystroke that you make will be recorded. Type [Esc] [Ctrl] – [J] a second time to end the session.

Loading data from file.	This message appears while data is being loaded into user RAM from a disk's data file.
Loading device algorithm	When you restore a set of system parameters that include a specific device, this message will appear while the programming algorithm is being loaded.
Loading device algorithm file into user RAM.	This message appears when the device programming algorithm is being loaded into user RAM at the first device selection operation after the "RAM device selection" switch is enabled.
Loading device menu data	For a single drive system, this message indicates that once UniSite has been booted with the system disk, and the algorithm disk installed, the device and manufacturer selection files are being loaded.
Loading from disk.	This message appears when UniSite is reading system information or routines from the disk.
Loading programming parameters	When you restore a set of system parameters from the Configuration file directory, this message will appear while the programming parameters are being loaded.
Loop count NNNN = Hit CTRL Z to abort this test	This message appears while a self-test is running in the continuous mode. The loop count NNNN is the number of times the selected test has been repeated.
Memory parity error at:XXXXXX	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the problem persists, record the location at which the error is occurring (represented above by "XXXXXX"), and call your nearest Data I/O Service Center.
No disk in drive A.	There is no disk in the disk drive. Insert the system disk into disk drive A and try the operation again.
Non-blank device. Hit return to continue, ^Z to abort.	This message appears after UniSite has performed a blank check on a device and has detected bits that are not in their erased or blank state, and are not illegal bits. If you press [↵], UniSite will proceed with the Programming operation and program over the existing data. If you press [Ctrl] – [Z], the Program screen will reappear and you can try the operation again with another device. The Blank Check option in the Programming Parameters screen must be enabled before this test can be performed.
OPERATION COMPLETE.	The operation you selected has been completed; you may now proceed with other operations.
OPERATION COMPLETE. Device = 00000000.	This message appears after a successful Compare Electronic ID operation. The "0's" are the device electronic ID.

OPERATION COMPLETE. Sumcheck = ssssssss

This message appears after the completion of a Program, Load or Verify operation. The "s's" represent the sumcheck of the data that was programmed into the device.

OPERATION COMPLETE. Sumcheck = ssssssss. Set Sumcheck = ssssssss

This message appears after the completion of a Set Program, Load, or Verify operation. "Sumcheck = ssssssss" is the sumcheck of data that was just programmed into the last set member. "Set Sumcheck = ssssssss" is the sumcheck of all the set members that have been programmed.

Options installed. Hit Return after changing your terminal settings.

This message appears in the Serial Port Configuration screen after the terminal serial port parameters have been changed and [↵] has been pressed. After this message appears, all output to the screen is suspended until a [↵] is pressed so that the user will have the opportunity to first configure his terminal to match the entered changes. Place the terminal in the setup mode (see your terminal's Instruction manual for setup procedure) and select the correct setting for the parameters that you changed in the Serial I/O screen.

Parameter Entered:

This message acknowledges that the parameter you entered was accepted.

Parameter Field Full. Hit return or arrows to enter, CTRL Z to abort.

This message appears when you have tried to enter too many characters into a parameter field. Press [↵], the [PF1] or [PF2] keys, or use the arrow keys to enter the parameter.

Power Down

UniSite has experienced a power down condition.

Pre-format check.

This message appears when you have selected the Format Disk operation, and means that UniSite is checking to see if the disk you want to format is a system disk.

Purging filename.ext

This message will appear if you are using the wildcard ("*") designation to purge more than one file at once: for example, typing "27*.DAT" to delete both the files *27512.DAT* and *27256.DAT*.

Reading user data file size

This message appears while UniSite is reading the data file size from disk.

Recording system state parameters.

This message appears after you select a file number for the set of system parameters that you want to save. This message remains until UniSite is finished recording the parameters.

Restoring system state variables.

This message appears while UniSite is reading the recorded system variables from the selected file.

RTE init err

UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact the Data I/O Service Center.

RTC err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact the Data I/O Service Center.
Saving data to file.	This message appears while data is being written to a file on disk.
Saving parameters	This message appears when UniSite is saving the selected variables onto the disk.
Saving job file.	This message appears when UniSite is saving a job file.
Search pattern not found	If you specified a data pattern for a file that does not contain that pattern, this message will appear. This message appears while UniSite is in the memory editor or in the under/overblow display.
Security fuse violation. Hit return to continue, ^Z to abort	This message appears when an attempt is made to program an EE device with the security fuse already blown. If you continue by pressing [↵], the program operation will be performed and previous data will be overwritten.
Single drive copy overwrites user RAM. Hit Return to continue, ^Z to abort.	If you try to perform a single drive disk copy, UniSite uses user RAM as a buffer. Therefore, anything already in user RAM will be overwritten on systems with one drive, or copying to the same drive. If you don't want the user RAM to change, type [Ctrl] – [Z] to abort. Otherwise a [↵] will proceed with the operation.
System error. Please contact Data I/O.	Contact your nearest Data I/O Service Center.
System parameters restored.	This message appears when you have restored a configuration file from the Restore System Parameters screen.
System parameters saved.	This message appears when you save a set of system parameters.
Task error	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact the Data I/O Service Center.
Testing	This message appears when a self-test is in progress.
TEST HALTED: Socket not empty, hit return to continue, ^Z to abort.	The self-test that you are attempting requires that the device socket does not contain any devices. Remove the socketed part and try the operation again, or type [Ctrl] – [Z] to abort the operation. Note: If you press [↵], UniSite will run the test and the socketed device could be damaged.
Transferring data.	This message appears while a data transfer operation is being performed.

[transparent mode]	This message appears on the screen when UniSite enters the transparent mode. To exit, type [Esc] [Ctrl] – [T] .
Trc init err	UniSite has experienced an error that it cannot recover from; turn UniSite off and reboot the system. If the error recurs, contact the nearest Data I/O Service Center.
User RAM sumcheck = ssssssss	This message contains the sumcheck for all of user RAM and is generated in the Sumcheck device check screen. This calculation is done regardless of whether or not user data is in RAM or on disk.
Vector out of range	The vector you tried to select does not exist for the device you have selected. Select a vector that is within the limits of the device or select a different device. This message may appear while you are using the vector editor.
Waiting for self-test completion.	This power-up message shows up only if you are changing the terminal selection before the power-up self-test has been completed.
WARNING Algorithm disk in drive. Hit return to continue, ^Z to abort.	This message will appear if you are attempting a file operation and have the Algorithm disk installed in the disk drive.
WARNING: system disk in drive. Hit return to continue, ^Z to abort.	This message appears during any file operation that displaces disk data. Any information currently on the disk will be erased and is not retrievable. Press [↵] if you want to go ahead with the operation; press [Ctrl] – [Z] , if you do not.

5 Computer Remote Control (CRC)

Introduction

UniSite can be controlled via a remote host computer using the Computer Remote Control (CRC) protocol described in this section. CRC commands have been designed to be incorporated into a remote computer software program (driver) which will allow an operator to control UniSite. The driver generates and sends commands to UniSite, which executes these commands and then returns a response character, and in some cases, also data. The driver then reacts to this character or data and uses it to generate messages and prompts for you. Standard CRC commands are supported by SetSite.

This section contains the following information:

- **System Setup** — Explains how to set up UniSite for remote control operation. Includes information on setting up the RS-232C port and how to enter/exit CRC mode.
- **CRC Commands** — Gives a complete listing of the available CRC commands. The comprehensive list is preceded by a command summary, which lists commands, descriptions and UniSite's response.
- **CRC Error Codes** — Lists the error codes that appear while UniSite is being operated in the CRC mode.

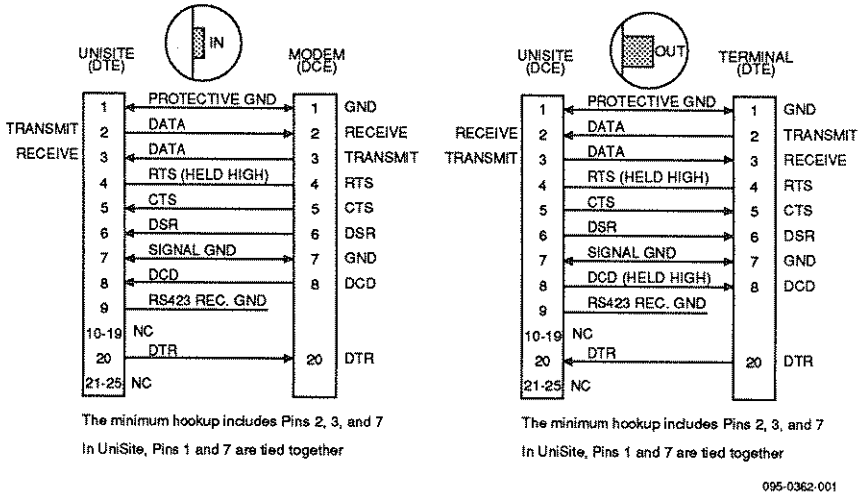
System Setup

UniSite communicates in CRC using 25-pin connectors that can be configured to be used with the RS-232C port configurations. The connections are shown in the following illustration.

Only the remote port supports remote control operation. The pin designations for the remote port are shown in the following illustration. This illustration is followed by a pin definitions table that explains the pin function for the two serial port configurations, including the handshaking lines.

To ensure correct operation of the remote port with the host computer, set the parameters for the serial remote port according to the host computer requirements.

Figure 5-1
Pin Designations for RS-232C Serial Port Connection



UniSite's Pin Functions for the 25-pin RS-232C Connector in DTE Mode

Pin No.	Signal	Description
1	Ground	Provides a safety ground connection.
2	Transmit Data	Carries the transmitted data.
3	Receive Data	Carries the received data.
4	Request to Send	This line is held high by UniSite.
5*	Clear to Send	A high on this line will enable UniSite to transmit data. (Used for hardware handshaking.) A low will inhibit data transmission from UniSite.
6*	Data Set Ready	This line is held high when the remote source is ready to send or receive data. A low will inhibit data transmission from UniSite.
7	Signal Ground	Provides a reference ground for all signals on the cable.
8*	Data Carrier Detect	This line is high when the modem detects a carrier. A low on this line inhibits UniSite from transmitting data.
9	RS-423	Receiver ground
10-19	No Connection	
20	Data Terminal Ready	This line is pulled high by UniSite to indicate it is ready to receive data. This line is pulled low to signal the remote computer to stop sending data. (Used for hardware handshaking.)
21-25	No Connection	

* *If these lines are not connected, UniSite will consider them high and will function normally.*

UniSite's Pin Functions for the 25-Pin RS-232C Connector in DCE mode

Pin No.	Signal	Description
1	Ground	Provides a safety ground connection.
2	Transmit Data	Carries the received data from DTE device to UniSite.
3	Receive Data	Carries the transmitted data from UniSite to DTE device.
4	Request to Send	This line is held high by UniSite.
5*	Clear to Send	A high on this line from UniSite means that it is ready to receive data (Used for hardware handshaking.)
6*	Data Set Ready	This line is high when UniSite is ready to transfer data.
7	Signal Ground	Provides a reference ground for all signals on the cable.
8*	Data Carrier Detect	This line is high by UniSite.
9	RS-423	Receiver ground
10-19	No Connection	
20	Data Terminal	A high on this line will enable UniSite to transmit data. (Used for hardware handshaking.) A low will inhibit data transmission from UniSite.
21-25	No Connection	

* *If these lines are not connected, UniSite will consider them high and will function normally.*

Entering CRC Mode

CRC mode can be entered in either of two ways: You can enter CRC by using the Remote Control menu, or you can set up UniSite to automatically go into CRC at power up.

To enter CRC mode using the Remote Control menu, do the following:

1. Enter the Main menu, by pressing [PF1] .
2. Type [M] to select the More commands menu.
3. Select Remote control from the More commands menu, by typing [R] .
4. UniSite is now in remote control mode. All keyboard input, except [Ctrl] - [Z] , will be ignored.

UniSite Interface Mode

The capability to use either the Terminal or Remote port as a normal terminal interface was added in version 2.8 of the UniSite software. The user may specify which port he desires to use via the User Menu Port parameter on the More commands/Configure system/Edit/Communication parameters screen. This parameter may also be saved as a power up parameter so that when UniSite is powered on it will use the port specified for terminal dialogue. UniSite has two basic operating modes: Terminal mode and CRC mode. Only one of these modes may be run at a time.

Terminal mode represents the mode UniSite is in when the user is controlling UniSite from a terminal (or PC running a terminal emulator program) using the menu screens to perform operations. CRC (Computer Remote Control) mode represents the mode UniSite is in when it only recognizes special commands sent from a computer to perform its operations (for more information about CRC mode refer to the Computer Remote Control section of the UniSite Operator's Manual). This mode does not provide the user menus which are present in terminal mode. Terminal mode operations may be run from either the Terminal or Remote port on UniSite. CRC operations may only be run on the Remote port.

UniSite's mode at power up is determined by the state of two system parameters (User Menu Port and Power Up CRC mode) and also by which port(s) are connected. The following table indicates UniSite's mode after power up as determined by these factors:

	A connected B connected	**A connected B not connected**	**A not connected B connected**
Power up CRC = off User Menu Port = A	Term on A	Term on A	CRC on B
Power up CRC = on User Menu Port = A	CRC on B	Term on A	CRC on B
Power up CRC = off User Menu Port = B	Term on B	Term on A	Term on B
Power up CRC = on User Menu Port = B	CRC on B	Term on A	CRC on B

Note: "A" represents the UniSite port labeled "Terminal". "B" represents the UniSite port labeled "Remote". "Term" represents Terminal mode and "CRC" represents Computer Remote Control mode.

If you wish to have UniSite power up in CRC, perform the following steps:

1. Enter the MAIN MENU, by pressing [PF1] .
2. Type [M] to select the More Commands menu.
3. Select the Configure System menu by typing [C] .
4. Select "Edit" from the Configure Systems menu, by typing [E] .
5. Select "Interface" from the Edit menu by typing [I] . UniSite's interface parameters will then be displayed on the screen.
6. When the cursor is next to the "power on CRC" option, type [Y] . CRC mode has now been selected. The following steps in this procedure save power-on CRC mode as a system parameter.
7. Press [PF2] two times to return to the Configure System Parameters menu.
8. Select "Save" from the Configure System Parameters menu by typing [S] . The screen will now display the Save System Parameters menu.
9. Type the number **1** and then press [↵] to select the "power up defaults" file as the one wheresystem parameters will be saved.
10. Press [↵] again so that the selection will be saved to the disk. Now, the next time you power up UniSite, it will enter CRC mode automatically.

Exiting CRC Mode

To exit CRC using the UniSite ASCII terminal, press [Ctrl] - [Z] . From the remote computer, send the "Z" command (followed by a [↵]).

If you exit remote mode using the "Z" command, UniSite's parameters will be set to what they were BEFORE you entered remote mode. If you use [Ctrl] - [Z] to exit remote mode, UniSite's parameters will NOT be changed.

Halting CRC Operations

To halt any command or any ongoing CRC operation, use the following commands from the remote port. Neither the **ESCAPE (ESC)** or **BREAK** require a carriage return to follow them. Each command is immediate and terminates any preceding command operation.

ASCII Command	Hex Code	Description
ESC	1B	Causes UniSite to unconditionally halt (abort) any operation except a binary transfer.
BREAK	none	Causes UniSite to unconditionally halt (abort) any operation in progress. This includes all data communications transfers. The data line must be held in the spacing condition for 110 ms to 700 ms.

Using PROMlink with UniSite

You may use Data I/O's PROMlink as a software driver for UniSite in CRC mode. The following subsection lists the UniSite CRC commands that are functional with PROMlink. In addition, many of UniSite's options are accessible by creating PROMlink User-Defined Functions to access them. Those functions are also listed below.

Note: You must have version 2.3 or later of PROMlink to use it with UniSite.

Program/Verify/Load Options

Data Word Width – Steps of 8 only (use User-Defined Function to specify 4)

(Logic) Terminal Mode – Not available (use UniSite's terminal mode)

Edit Functions

Split RAM – Not required (automatic with UniSite's Set Programming)

Shuffle RAM – Not required (automatic with UniSite's Set Programming)

(Logic) Terminal Mode – Not available (use UniSite's terminal mode)

File Transfer Functions

Binary File Transfers – Files less than or equal to 64K only (version 2.7 does not have the restriction).

Utilities

TERM-100.EXE – PROMlink Utilities includes Term-100, a general purpose VT-100 terminal emulator which may be used with UniSite's terminal mode.HiTerm is another terminal emulator program shipped with UniSite which provides all of the capabilities of Term-100 and also supports UniSite's high speed download feature. For this reason, HiTerm is the recommended program to use when controlling UniSite in terminal mode from a PC. For detailed information regarding HiTerm, refer to the UniSite PC Utilities Manual 983-0234.

Computer Remote Control Functions

Almost all of UniSite's CRC commands may be used by PROMlink. The following list shows those CRC commands that are not used by PROMlink's normal menu selections and that may be implemented by User-Defined Functions. (Refer to the PROMlink User Manual to find instructions for creating User-Defined Functions.)

CRC Program/Load/ Verify Commands

CRC Code	Command
nn22]	Data Word Width
nn07]	Next Set Member
hh2A]	Enable Programming Options
bit 0 (hex 01)	Illegal-Bit Check
bit 1 (hex 02)	Blank Check
bit 2 (hex 04)	Yield Tally
bit 3 (hex 08)	Erase EE Device
bit 4 (hex 10)	Odd/Even Byte Swap
bit 5 (hex 20)	JEDEC I/O Translate DIP/LCC
bit 6 (hex 40)	Continuity Check
hh2B]	Disable Programming Options <Same list as Enable>
hh2D]	Vector Test Options
nn2F]	View 8-Character Sumcheck
n27]	Program Security Fuse/Data
n29]	Reject Count Option
n23]	Number of Verify Passes
n26]	Logic Verification Options
n27]	Set/Clear Enable/Disable Security Fuse
n31	Set Data/Source Destination
39]	Delete All RAM Files
n03]	Silicon Verify Option
xx. . .xxxx30]	Set Data File Name
xx. . .xxxx38]	Load File From Disk

CRC RAM Commands

-	Invert RAM
\	Move Memory Block
n28]	Fill Fuse Map

CRC Device Status Commands

R	Return Status of Device*
nnS	View Sumcheck*
Y	Display Parity Errors
[	View Device Family/Pinout Code
43]	Upload Yield Tally

CRC File Transfer Functions

hhM	Enter Record Size
nn02]	Set Upload Wait Time
...x05]	Set Host Command

CRC System Management Functions

G	Configuration Inquiry
Z	Exit Remote Control
01]	Display System Configuration
n41]	Upload Self Test Results
FC]	Restore Entry CRC Default Parameters
FD]	Restore User-Defined CRC Parameters
FE]	Save User-Defined CRC Parameters

* *These commands are used internally by PROMlink, but must be implemented as User-Defined Functions to view the results directly.*

Using Remote ON/OFF to Connect Multiple UniSites

Two features on the Interface Parameters menu may be used to affect the manner in which UniSite responds to CRC commands while in CRC mode: the "Remote ON code" and the "Remote OFF code". Use these features if you want to use ASCII characters to enable/disable the remote port. Remote ON/OFF can be used, for example, to connect multiple UniSites to a single host computer.

When the Remote ON and Remote OFF codes are set to something other than zero, UniSite will ignore all data input after receiving the Remote OFF code until it receives the Remote ON code. After receiving the Remote ON code, commands and data are processed normally until another Remote OFF code is received.

The two codes are normally set to control characters (hex 01 - 1F) and only used when transfers contain non-binary data. The data itself should never be the same as the codes used for Remote ON/OFF.

CRC DEFAULT SETTINGS

When CRC mode is entered, certain defaults are set prior to accepting any commands. The default settings are outlined below:

Description	Setting
Upload/download port	Remote port
Data source/destination	RAM
Security fuse data (0 or 1)	0
Program security fuse	No
Reject option (commercial or single)	Commercial
Logic verification option (All,Fuse,Vector)	All
Number of verify passes (0,1 or 2)	2
Fill RAM before downloading	No
Illegal bit check option	No
Blank check option	No
Enable yield tally option	No
EE bulk erase option	No
Odd/even byte swap for 16 bit option	No
JEDEC I/O translate DIP/LCC option	Yes
Continuity check option	Yes
Compare electronic signature	Yes
Host command	Blank
I/O address offset	0

Description	Setting
I/O format	MOS technology (format 81)
Instrument control code (0,1, 2)	0
I/O timeout	30 seconds (if disabled in local mode, it remains disabled)
Upload wait	0 seconds
Number of nulls	255 (eliminates line feed after carriage return and nulls on output)
Serial set auto-increment mode	No
Programming mode	single device
Total set size	1
Upload EOF delimiter flag	Disabled
Download EOF delimiter flag	Disabled

If you exit remote mode using the Z command, UniSite's parameters will be set to what they were BEFORE you entered remote mode. If you use Ctrl - Z to exit remote mode, UniSite's parameters will NOT be changed.

CRC COMMANDS

CRC Command Summary

CRC commands are upper case ASCII characters which are summarized in the command summary table and described in more detail in the pages that follow. The command tables are broken up into standard and extended CRC commands.

When UniSite is sent one of the commands listed in the left column, followed by a carriage return, it executes the command and sends back one of three responses; an "F," a "?," or a ">." The response that should be sent is shown in the right-most column in the table. If an error occurs, an "F" will be sent. If "?" is sent, the previous command was not recognized. If the response is a ">," the previous command was successfully executed. The ">" is sometimes prededed by some status information.

All responses will be followed by a carriage return and possibly a line feed: the set nulls command (nnU) determines whether or not a line feed is sent after the carriage return. The commands "I", "O" and "C" will perform any data transfer prior to sending the response.

Summary of Standard CRC Commands

Command Entry	Command Description	Hex Code	UniSite Response
&	Insert parts mode	26	None
-	Invert RAM	2D	>
/	View device error status	2F	XXYY>
hhhhhh:	Select device begin address	3A	>
hhhhhh;	Select memory block size	3B	>
hhhhhh<	Select memory begin address	3C	>
nn=	Select I/O timeout	3D	>
fffppp@ or ffpp@	Select device type	40	>
cffA	Enter translation format	41	>
B	Blank check	42	>
C	Compare to port	43	>
D	Set odd parity	44	>
E	Set even parity	45	>
F	Error status inquiry	46	HHHHHHHH>
G	Configuration inquiry	47	RRDD>
H	No operation	48	>
I	Input from port	49	>
J	Set 1 stop bit	4A	>
K	Set 2 stop bits	4B	>
nnL	Load RAM from device	4C	>
hhM	Enter record size	4D	>
N	Set no parity	4E	>
O	Output to port	4F	>
nnP	Program device	50	>
R	Return status of device	52	AAAAA/BB/C>
nnS	View Sumcheck	53	HHHH>
nnT	Illegal-bit test	54	>
hhU	Set nulls	55	>
nnV	Verify device	56	>
hhhhhhhhW	Set I/O offset	57	>
X	Error code inquiry	58	HH....HH>
Y	Display parity errors	59	HHHH>
Z	Exit remote control	5A	none
[	View device family/ pinout code	5B	FFFPPP>
\	Move memory block	5C	>
hh^	Clear/fill RAM with data	5E	>

Summary of Extended CRC Commands

Command Entry	Command Description	UniSite Response
01]	Display system configuration	RRR/SSSS/AAAA/ MM/PPP/IIVV/ JJVV/KKVV>
nn02]	Set upload wait time	>
n03]	Set device ID verify option	HHHHHHHH> or >
nn04]	Set remote port baud rate	>
xxx...xxxx05]	Set host command	>
n06]	Select data bits	>
n07]	Set next set member	>
n08]	Select programming mode	>
nn22]	Set data word width	>
n23]	Select number of verify passes	>
n24]	Select security fuse programming option	>
n26]	Specify logic verify options	>
n27]	Set/clear, enable/disable sec. fuse	>
n28]	Fill fuse map	>
n29]	Set reject count option	>
hhh2A] or hh2A]	Enable programming options	>
hhh2B] or hh2B]	Disable programming options	>
nhh2C]	Select memory fill option	>
nhh2D]	Vector test options	>
nhh2F]	View 8-character sumcheck	>
xxx...xxxx30]	Set data file name	>
n31]	Set data source/destination	>
xxx...xxxx33]	Select device manufacturer	>
xxx...xxxx34]	Select device part number	>
xxx...xxxxx38]	Load file from disk	>
39]	Delete all RAM files	>
40]	Upload parts list	See text following
n41]	Upload self test results	AAA...AA>
43]	Upload yield tally	See text following
46]	Clear yield tally	>
DC]	Device check	>
DF]	View status of sockets	HH HH HH HH HH HH HH HH>
EB]	Input JEDEC data from host	>
EC]	Output JEDEC data to host	>
FC]	Restore CRC entry default parameters	>
FD]	Restore user-defined CRC parameters	>
FE]	Save user-defined CRC parameters	>

Standard CRC Commands

The Standard CRC Commands are described in this section. Note that the lower-case alpha characters preceding the commands are parameters that must be specified according to the options listed under the corresponding command description.

& — **Insert Parts Mode** — (SetSite command) causes UniSite to go into a "wait" state, allowing you time to insert the devices. It will remain in this state until you push the SetSite socket lever forward to the "start" position to begin a device operation, such as "B", "nnL" or "nnV." This command also clears the device statistics, although the yield tally data will remain unchanged. The "&" command may be halted by using the ESC key or pulling SetSite's socket lever to the OPEN (straight up) position.

/ — **View Device Error Status** — allows you to output a status sequence from the previous device operation, showing how many devices were successfully programmed. The data will be output in the form "XXYY," where "XX" is the number of device that did NOT successfully program and "YY" is the total number of devices you attempted to program.

— — **Invert RAM** — instructs UniSite to invert data in RAM within the address range defined by the beginning memory address and the memory block size. If the memory block size was previously set to 0, the user memory size determines the number of bytes to invert.

hhhhhh: — **Select Device Begin Address** — sets the first device address to be used. This device begin address is also used as the destination address in a RAM-RAM block move. Type a 1 to 6 digit hex address ("hhhhhh") preceding the ":" command to specify the specific address. A default address of 0 is set if no digits precede the command.

hhhhhh; — **Select Memory Block Size** — sets the number of bytes to be uploaded or programmed. Type a 1 to 6 digit hex address ("hhhhhh") preceding the ";" command to specify the specific block size. In UniSite, both the memory block size as well as the device block size are set by this command. A default block size of 0 is set (for device operations) if no digits precede the command. The default will be the user memory size during I/O operations, if no address is specified (minus any beginning address you may have set).

hhhhhh< — **Select Memory Begin Address** — sets the first RAM address from which or to which data is to be transferred. This address is also used as the begin RAM address where the programming data is located. Type a 1 to 6 digit hex address ("hhhhhh") preceding the "< "command to specify the specific address. A default address of 0 is used if no digits precede the command.

nn= — **Select I/O Timeout** — specifies how long UniSite will wait for data to be downloaded before it will return an I/O timeout error code (46). The command may be preceded with 2 decimal digits making the range of the timeout from 01 to 99 seconds. If the command is preceded either by 00 or no parameter, the timeout is disabled. The default timeout is 30 seconds.

fffppp@ or ffpp@	**Select Device Type** — selects the family and pinout codes for the device to be programmed. Either 3-digit hex family and pinout codes, "fffppp", or 2-digit hex family and pinout codes, "ffpp", must precede the command. (An alternate method of selecting the device type uses the commands 33] and 34].)
cffA	**Enter Translation Format** — selects the instrument control code "c" and the data translation format "ff" to be used for I/O data transfers through the remote port. From 1 to 3 digits must precede the command. If 1 or 2 digits precede the command, they define the data translation format and the instrument control code defaults to 0. If 3 digits precede the command, the first digit designates the instrument control code and the last two digits specify the format code. For example, if you type "**191A**," instrument control code 1 and data translation format 91 will be selected. The data translation formats and the instrument control codes are described at the end of this section.
B	**Blank Check** — instructs UniSite to search the device to insure that no bits are programmed.
C	**Compare To Port** — instructs UniSite to compare data in UniSite's RAM with data received through the remote port using the current data translation format. (JEDEC format cannot be used with this command. This command only works for memory formats.) The current memory begin address and I/O offset are used to calculate the RAM address where the data is located to compare against the incoming data.
D	**Set Odd Parity** — instructs UniSite to set odd parity on the remote port for output data and inspect incoming data for odd parity.
E	**Set Even Parity** — instructs UniSite to set even parity on the remote port for output data and inspect incoming data for even parity.
F	**Error Status Inquiry** — instructs UniSite to display a 32-bit number in the format HHHHHHHH where each H is a hex character. The 32-bit word defines the accumulated errors in the error status word since the last 'F' command. See the "error status word" description later in this subsection.
G	**Configuration Inquiry** — instructs UniSite to return the software configuration information. This includes 2 digits of ROM version followed by 2 digits of disk version. The configuration information is returned in the form "RRDD", where "RR" is the ROM version and 'DD' is the disk version. Additional configuration information can be obtained by using the extended command "01]."
H	**No Operation** — instructs UniSite to perform no operation, but just return the prompt character, ">" followed by the ↵ and line feed if specified.

I — **Input From Port** — instructs UniSite to accept formatted data from the remote port using the currently selected data translation format and load that data into RAM. For memory devices, the current memory begin address and I/O offset values are used to calculate the RAM address where the input data is loaded. For logic devices, all of the fuse map and structured vectors will be received and placed in RAM at the appropriate address. You must select the JEDEC format if a logic device is selected.

UniSite will send an XOFF to the host computer after the CRC I command is received. This allows UniSite time to get ready to receive data from the host computer. An XON will automatically be sent to the host computer to begin the data transfer. Even if your host system has hardware handshake or XON/XOFF, it is recommended that you provide a 20 millisecond delay between the CRC I command and the first byte of data.

If your system does not have hardware handshake or XON/XOFF capability, you must provide the delay to separate the CRC I command from the first byte of data sent. A delay of 1/2 second to 10 seconds is suggested, depending on whether you use the fill memory option and the size of your user memory.

J — **Set 1 Stop Bit** — sets one stop bit for serial data transfers through the remote port.

K — **Set 2 Stop Bits** — sets two stop bits for serial data transfers through the remote port.

L or nnL — **Load RAM From Device** — instructs UniSite to load data from the currently selected device to UniSite's RAM. For memory devices, the first device address copied from (device begin address), the first RAM address copied to (memory begin address), and the size of the block copied (memory block size) should all be specified prior to executing this command. In the case of logic devices, the entire device is loaded. For a SetSite operation (nn = 01- 08), use "nnL", where "nn" is the number of devices in the set you want to load.

hhM — **Enter Record Size** — sets the number of data bytes "hh" per record for serial output operations. The command must be preceded by a 2-digit hex code defining the record size.

N — **Set No Parity** — instructs UniSite not to check parity on incoming data and to output data without parity through the remote port.

O — **Output To Port** — instructs UniSite to output data using the current translation format to the remote port. For memory devices the current parameter settings for memory block size, memory begin address, and I/O address offset are used. The complete fuse map and structured vectors will be output for logic devices. The format must be JEDEC if a logic device is selected.

P or nnP — **Program Device** — instructs UniSite to program a device with data in RAM. For memory devices, the first address to program from (memory begin address), the number of bytes to program (memory block size) and the first device address to program (device block size) may be specified prior to executing this command. For logic devices the entire device is programmed. For a SetSite operation (nn = 01-08, use "nnP", where "nn" is the number of devices in the set you want to program.

R — **Return Status of Device** — Instructs UniSite to return the attributes of the device selected by the current family and pinout code. Data is output in the form "AAAAA/BB/C" where "AAAAA" is the device's word limit in hex, "BB" is the word size in decimal and "C" = 1 (VOL) or 0 (VOH). For logic devices, "AAAAA" indicates the number of fuses and "BB" is the number of device pins.

S or nnS — **View Sumcheck** — instructs UniSite to calculate the sumcheck of the RAM data. For memory devices, the sumcheck starts at the beginning of user RAM and continues for the word limit (device size) of the selected device. For logic devices, the sumcheck starts at the beginning of user RAM plus 8 bytes and continues for the device size divided by 8. In either case, the calculated sumcheck is returned as a 4-digit hex number, "HHHH". For a SetSite operation, use "nnS", where "nn" corresponds to data from device socket (nn = 01 - 08). The sumcheck is calculated from RAM.

T or nnT — **Illegal-bit Test** — instructs UniSite to test the selected device for illegal bits. An illegal bit is defined as a programmed bit in the device that does not exist in RAM. For a SetSite operation, use "nnT", where "nn" is the number of devices in the set, (nn = 01-08).

hhU — **Set Nulls** — sets the number of nulls after a carriage return on output data transfer operations. This command also enables/disables sending of a line feed after every carriage return sent out (for responses too). This command must be preceded by 1 or 2 hex digits that determine the number of nulls to be sent. If the null count is set to "FF", no line feeds or nulls will be sent after each carriage return. If no parameter precedes the command, the number of nulls defaults to zero and line feeds are enabled.

V or nnV — **Verify Device** — instructs UniSite to verify RAM data with the data from the programmed device. For memory devices, the memory begin address, device begin address and memory block size must be set prior to the execution of this command For logic devices, the entire device is verified. For a SetSite operation (nn = 01 - 08), use "nnV", where "nn" is the number of devices in the set you want to verify.

hhhhhhhhW — **Set I/O Offset** — sets the I/O offset address to be used in I/O operations. Up to eight hex digits may precede the command. If "FFFFFFFF" precedes the command, the default I/O offset value 0 is used on output and the first incoming address is used on input. If no parameter precedes the command, the I/O offset is set to 0. On input operations, the address where the data is placed is calculated by taking the incoming address, subtracting the I/O offset and adding the memory begin address. On output, the outgoing address is calculated by taking the address where the data is located, subtracting the memory begin address and adding the I/O offset.

X — **Error Code Inquiry** — instructs UniSite to output the last 20 error codes which occurred. The command also clears the error codes from memory. If no errors have occurred, UniSite will just return the normal response ">" followed by a carriage return. The 'X' command is normally sent as a result of the 'F' response being sent meaning the previous command failed. Each error code returned is a 2-digit hex character and all the error codes are defined in the CRC error message section.

Y — **Display Parity Errors** — instructs UniSite to display the number of parity errors encountered since power on, the last Y command, or since the last parity command (O,E, N). The number returned is a 4-digit hex number, "HHHH". The parity error counter is cleared after this command executes.

Z — **Exit Remote Control** — Exit remote control and return control to UniSite's terminal port interface.

[— **View Device Family/pinout Code** — instructs UniSite to output the family and pinout code currently in effect. The family and pinout codes are returned in the form FFFPPP where "FFF" is the 3-digit family code and "PPP" is the 3-digit pinout code.

**** — **Move Memory Block** — instructs UniSite to move data from one RAM location to another. The memory begin address, device begin address (memory destination address) and memory block size all should be set prior to execution of this command. The memory begin address is used for the source address. The device begin address is used for the destination address. The memory block size determines the number of bytes to move. If the memory block size is set to 0, then the block size will default to the size of user memory.

hh^ — **Clear/fill RAM With Data** — instructs UniSite to fill every address within the range defined by the memory begin address and memory block size with the hex data pattern "hh". The memory begin address and memory block size should be set prior to execution of this command. If you have set the memory block size to 0, all of user RAM will be filled with the data pattern. If you just send ^ without any preceding numbers, all of user RAM will be cleared (00) — regardless of how you have specified the block parameters.

Extended CRC Commands

The Extended CRC Commands are described in this section. Note that the lower- case alphabetic characters preceding the commands are variables that must be specified according to the options listed under the specific command description. For example, the "nn02]" indicates that you may precede the 02] command with two decimal digits.

01] **Display System Configuration** — instructs UniSite to display the system configuration information which includes the ROM and disk software version, the RAM size and the number of pin drivers. Data is presented in the form "RRR/SSSS/AAAA/MM/PPP/IIVV/JJVV/KKVV" where "RRR" defines the current ROM version, "SSSS" is the current System disk version, and "AAAA" is the Algorithm disk version. "MM" is a decimal number indicating the number of 64k- byte banks of RAM memory available, and PPP is a decimal number indicating the number of pin drivers available. "IIVV", "JJVV" and "KKVV" are 4-digit module configuration numbers that identify which module(s) are installed and what version they are: "IIVV" contains PSM data; "JJVV" contains FSM data; "KKVV" contains base data. If "II", "JJ" or "KK" are 00, it means no module is installed.

The following is a list of the configuration numbers which UniSite may output in response to receiving the 'Display System Configuration' CRC command (01]) depending on which modules/bases are installed.

PSMs (II)	FSMs (JJ)	Bases (KK) for use with PinSite
01 – Site 40	01 – ChipSite	01 – PLCC/LCC base
02 – Site 48	02 – SetSite	02 – PGA Base
	04 – PinSite	03 – SOIC Base
	05 – USM-340	

nn02] **Set Upload Wait Time** — sets the number of seconds that UniSite will wait before transferring data on an upload. The command must be preceded by two decimal digits, "nn", that specify between 0 and 99 seconds.

n03] **Select Electronic ID** — selects the option for the electronic ID as defined by the parameter (the "n") preceding the command: the command must be preceded by a 1 - digit decimal number defined as follows:

0 - disables electronic ID verify option

1 - enables electronic ID verify option

2 - display electronic ID

When the display electronic ID option is chosen, the current electronic ID is retrieved from RAM and returned as 8 hex digits in the form "HHHHHHHH". Leading zeros will be sent for those device not having an 8-digit ID (0000890D, for example). In gang/set mode, eight groups of 8 hex digits are returned (one for each socket), with each group separated by a space.

nn04]

Set Remote Port Baud Rate — sets the remote port baud rate. The command must be preceded by a 1 or 2-digit decimal number, "nn", in the range of 1-17. The baud rate will be set according to the following table selections.

Baud Selection	Rate	Baud Selection	Rate
1	50	10	1500
2	75	11	1800
3	110	12	2000
4	134.5	13	2400
5	150	14	4800
6	200	15	7200
7	300	16	9600
8	600	17	19.2K
9	1200		

xxx...xxxx05]

Set Host Command — sets the host command string to be used later for upload or download of data. The command string can be from 0 to 58 characters long. If there are no characters preceding the command, no host command will be sent. A ↵ is appended to the end of the string by UniSite.

n06]

Select Data Bits — selects the number of data bits used in data transfers on the remote port. The command must be preceded by a 1-digit decimal number defined below:

8 - selects 8 data bits
7 - selects 7 data bits

n07]

Set Next Set Member — determines data organization when doing set programming. For example, if you are programming 4-bit devices and have set the data word-width equal to 8, setting the "next set member" ("n") equal to 2 means that the upper 4 bits of each data byte (rather than the lower 4 bits) will be used to program the device.

n08]

Select Programming Mode — selects type of programming you want to do, either single or gang/set. The number "n" which precedes this command directs UniSite to single ("n" equal to 0) or gang/set ("n" equal to one) mode.

nn22]

Set Data Word Width — allows the operator to specify the width of a data word, "nn", in the target microprocessor system for the device being programmed. The command must be preceded by a 2-digit decimal number defining the data word width. The choices for this option range from 4 bits to 64 bits.

n23]

Select Number of Verify Passes — selects the number of verify passes and voltages used to verify the data programmed into a part during a program operation. The command must be preceded by a 1-digit number defined below:

0 - no verify passes.
1 - performs a single-pass verify with nominal Vcc.
2 - performs a two-pass verify, one at the maximum allowed Vcc, and one at the minimum allowed Vcc value.

n24] **Enable Security Fuse** — Enables/disables programming the security fuse(s). This command must be preceded by a 1-digit decimal number defining one of two allowable options below:

0 - disables programming the security fuse(s).
1 - enables programming the security fuse(s).

n26] **Specify Logic Verify Options** — selects the type of logic verification to perform on the selected device during any following verify operation. The command must be preceded by a 1-digit decimal number defining the option desired. The allowable options are defined below:

0 - performs the fuse verify test followed by a structured vector test.
1 - performs only the fuse verify test.
2 - performs the structured vector test.

n27] **Set/Clear Enable/Disable Security Fuse** — Enables/disables security fuse programming and sets the state of the security fuse. The command must be preceded by a 1-digit decimal number that is one of the allowable options defined below:

0 - disables programming and sets the security fuse state in RAM to 0.
1 - disables programming and sets the security fuse state in RAM to 1.
2 - enables programming and sets the security fuse state in RAM to 0.
3 - enables programming and sets the security fuse state in RAM to 1.

n28] **Fill Fuse Map** — specifies the fuse state with which to fill the fuse map. The command must be preceded by a 1-digit decimal number defining the state of the fuse:

0 - fills the fuse map in RAM with 0's.
1 - fills the fuse map in RAM with 1's.

n29] **Set Reject Count Option** — selects the maximum number of programming pulses required to program a device before UniSite rejects the device as unprogrammable. The command must be preceded by a 1-digit decimal number defining one of two allowable options below:

0 - selects the manufacturers specified number of programming pulses.
1 - selects a single programming pulse or military reject count

hhh2A] **Enable Programming Options** — enables one or more programming options. The command must be preceded by a 2 or 3-digit hex number, 'hh' or 'hhh', that enables the desired options as defined by the option bits below:

Bit 0 (hex 01) = enable illegal bit check
Bit 1 (hex 02) = enable blank check
Bit 2 (hex 04) = enable yield tally
Bit 3 (hex 08) = enable erase EE device
Bit 4 (hex 10) = enable odd/even byte swap
Bit 5 (hex 20) = enable JEDEC I/O translate DIP/LCC
Bit 6 (hex 40) = enable continuity check
Bit 8 (hex 100) = enable special data (optional)

hhh2B] **Disable Programming Options** — disables one or more programming options. The command must be preceded by a 2 or 3-digit hex number, 'hh' or 'hhh', that disables the desired options. The option bits are defined the same as command '2A' above.

hh2D] **Vector Test Options** — enables or disables the compensated vector test, serial vector test and high speed logic driver options.

Bit 0 = 0 for disable Compensated Vector Test
Bit 0 = 1 for enable Compensated Vector Test
Bit 1 = 0 for disable High Speed Logic Driver
Bit 1 = 1 for enable High Speed Logic Driver
Bit 2 = 0 for disable Serial Vector Test
Bit 2 = 1 for enable Serial Vector Test

nhh2C] **Select Memory Fill Option** — specifies what data the user memory will be filled with before downloading begins. The "hh" represents the hex value that user RAM will be filled with when "n" =2. The legal values of "n" are:

0 = None (memory is not changed)
1 = Default (unused locations are initialized to the unprogrammed state for the device type selected)
2 = User specified (fill unused memory locations with hex data specified by "hh")

nn2F] **View 8-Character Sumcheck** — instructs UniSite to calculate the 8-character sumcheck of the RAM data which is returned as an 8-digit hex number, "HHHHHHHH". Refer to the S or nnS command for further details.

xxx...xxxx30] **Set Data File Name** — this command instructs UniSite to use the file name for any subsequent Disk or RAM file operation.

n31] **Set Data Source/Destination** — This command specifies the source/destination for the data file. The allowable options are listed below.

0 = RAM
1 = Disk
2 = RAM file

xxx...xxxx33] **Select Device Manufacturer** — this command selects the device manufacturer for device operations. From 1 to 13 alphanumeric characters can precede the command and must match exactly as it appears on the UniSite MANUFACTURER LIST screen or as it is uploaded via the 40] command. The manufacturer selected will not take effect until the command 34] is issued to select the part number.

xxx...xxxx34] **Select Device Part Number** — selects the device part number for device operations. From 1 to 29 alphanumeric characters can precede the command and must match exactly as the part appears on the UniSite PARTS MENU for the selected Manufacturer or as it is uploaded via the 40] command. This command will select an algorithm based on the part number sent in this command and the Manufacturer sent in the 33] command.

xxx...xxxx38] **Load File From Disk** — allows you to load a disk file into RAM. The maximum length of the filename is 14 characters. The entire file is always loaded, and the user data size is updated to reflect the size of the file loaded into RAM by UniSite's disk. The default drive is A. To load a file from the B drive, precede the filename with a "B:". Command example, B:27128.DAT38].

39] **Delete All RAM Files** — this command should be used when clearing all RAM files from memory. When RAM files are created, they stay resident in memory until this command is sent to clear all of them from RAM. This should be done in order to keep UniSite from running out of RAM space for files.

40] or n40] **Upload Parts List** — the 40] command uploads from the disk a list of all the devices supported by that particular version of software. The data will be transferred as a string of characters in the format described.

Number of entries on manufacturer list screen2
<CR><LF> 2 (hex)

Next will be data for EACH device manufacturer, organized as follows:

Device manufacturer's name 1 to 32
Colon 1
Number of devices for this manufacturer3 (hex)

Next, the following will be repeated for each device that this manufacturer supports:

<CR><LF> 2 (hex)
Device's part number 1 to 32
Colon 1
Family code 4
Pinout code 4
Electronic ID 8
Module device support 2 (hex)
When the bit is set then
- Bit 7 the device is supported on SetSite
- Bit 6 (unused)
- Bit 5 the device is supported on PinSite
- Bit 4 the device is supported on ChipSite
- Bit 3 the device is supported on USM-340
- Bit 2 the device is supported on Site48
- Bit 1 the device is supported on Site40
- Bit 0 the device is not supported on HandlerLink

<CR><LF> next device for *this* manufacturer . . . etc

<CR><LF> next manufacturer . . . etc

Upload Current Part Information — if the 40] command is preceeded by a 1 (140]) UniSite will upload information about the currently selected part. If the part has been selected by fam/pincode, the silicon signature returned is the first one encountered from the silicon signature table. The current part information will be transferred as a string of characters in the format described below.

Device manufacturer's name	1 to 32
Colon	1
Device's part number	1 to 32
Colon	1
Family code	4
Pinout code	4
Electronic ID	8
Module device support	2 (hex)

When the bit is set then

- Bit 7 the device is supported on SetSite
- Bit 6 (unused)
- Bit 5 the device is supported on PinSite
- Bit 4 the device is supported on ChipSite
- Bit 3 the device is supported on USM-340
- Bit 2 the device is supported on Site48
- Bit 1 the device is supported on Site40
- Bit 0 the device is not supported on HandlerLink

Following are two examples.

1. If the part has been selected with fam/pincode 93/51 by doing 9351@, the 140] command will cause UniSite to return

Unknown:Unknown:009300510000070D86

2. If the Intel 27128A has been selected using manufacturer name/part number by using the commands INTEL33] and 27128A34], the 140] command will cause UniSite to return

Intel:27128A:009300510000898986

n41] **Upload Self Test Results** — uploads the results of self-test to the host computer. The command must be preceded by a 1-digit decimal number that determines whether or not the self-test routines will be performed prior to uploading the self-test results. The 1-digit option parameter is defined below:

0 - do not perform self-test.
1 - perform self-test (not available yet same as 0).

30 bytes of self-test results are uploaded to the host. The self-test results from each of the 30 UniSite boards or functions are returned. Each byte returned can be one of four ASCII codes indicating the self-test status:

ASCII '-' = hardware not installed
ASCII '?' = untested
ASCII 'F' = failed self test
ASCII 'P' = passed self test

The following list shows the 30 bytes of self-test data, returned when you specify the self-test command in CRC mode. The results of self-test are sent to the host in the order defined in the following table.

Byte Number	Board/Function Tested	Byte Number	Board/Function Tested
1	Spare	16	P/D board 7
2	EPROM	17	P/D board 8
3	System RAM	18	P/D board 9
4	User RAM	19	P/D board 10
5	Serial port A	20	P/D board 11
6	Serial port B	21	P/D board 12
7	Disk drive A	22	P/D board 13
8	Disk drive B	23	P/D board 14
9	Option board	24	P/D board 15
10	P/D board 1	25	P/D board 16
11	P/D board 2	26	P/D board 17
12	P/D board 3	27	Waveform gen-
13	P/D board 4		erator board
14	P/D board 5	28	PCU
15	P/D board 6	29	PSM board
		30	FSM board

43] **Upload Yield Tally** — uploads the device yield tally statistics. The statistics for up to sixteen different types of devices is returned. The format of the yield statistics returned is as follows:

Manufacturer's name or family/pinout	- 25 characters
Total parts attempted	- 5 characters
Space	- 1 character
Total parts passed	- 5 characters
Space	- 1 character
Total illegal bit/blank errors	- 5 characters
Space	- 1 character
Total verify errors	- 5 characters
Space	- 1 character
Total structured test errors	- 5 characters
Space	- 1 character
Total program failures	- 5 characters
Carriage return, line feed	- 2 characters

There is one line returned in the format above for every device entry in the yield tally statistics file.

46] **Clear Yield Tally** — clears the yield tally statistics.

DC] **Device Check** — Checks for device in socket. If the socket is empty, an "F" is returned. Error code "3B" will be returned after the "X" command is sent. If a device is in the socket, further device checks are done if the device supports insertion and socketing tests. For example, a device insertion error "2A" is returned if the device is mis-socketed. If a device is in the socket and no continuity errors occur, the normal prompt (<) is returned.

DF] **View Status Of Sockets** — (SetSite command) outputs the status of all eight sockets, from the previous device operation. Status is returned in groups of eight 2-digit hex numbers, separated by a space. Each of these groups represents data for a particular device. The very first two hex characters, for example, contain data for the device in socket one. This status is cleared after receiving the "&" command. Each bit contains different device status information:

Bit	Status If Set To One
7	Error was detected
6	Non-blank device error
5	Device testing or overcurrent error
4	Invalid electronic ID error
3	Illegal-bit error
2	Programming error
1	Verify error
0	Device is in the socket

EB] **Input JEDEC Data From Host** — instructs UniSite to accept JEDEC formatted data from the remote port. The I/O format is forced to '91.' This command is valid only for logic devices. All of the fuse map and structured vectors will be received and placed in RAM at the corresponding position.

EC] **Output Jedec Data To Host** — instructs UniSite to output JEDEC data to the remote port. This command is valid only for logic devices. The fuse and vector data in RAM must be valid for the logic device selected. The I/O format is forced to '91'. The complete fuse map and structured vectors will be output.

FC] **Restore CRC Entry Default Parameters** — sets the current system parameters to the original CRC default values as shipped from the factory.

FD] **Restore User-defined CRC Parameters** — sets the current system parameters to the values last saved by the save user-defined CRC parameters command. The user-defined CRC parameters would be the same as the CRC factory defaults if no one had saved any changed parameters using the save user-defined CRC parameters command.

FE] **Save User-defined CRC Parameters** — saves the current system parameters to a disk file which is used by the restore user-defined CRC parameters command to restore the current parameters to those saved in the file.

Error Status Word

After executing the CRC "F" command, a 32-bit error status will be sent to the computer (or terminal). The error status word format is shown in the following table.

The table shows that the eight-character word is broken into four two-character groups. The first two-character group defines receive errors, the second group defines programming errors, the third group defines I/O errors and the last group is unused. Each two-character group contains a maximum of eight bits, with each bit representing the presence of the defined error or error type. Multiple errors within a character do occur; therefore, if all four bits within the character are used and present, the transmitted character would be "F", while if there were no errors present for that character, a "0" would be transmitted.

Type of Error	No.	Bit Value	Description
Receive Errors	31	8	ANY ERROR. If the word contains any errors, the most significant bit (bit 31) will be high
	30	4	Not used
	29	2	Not used
	28	1	Not used
	27	8	Not used
	26	4	Serial-overrun error (42)
	25	2	Serial-framing error (41,43)
	24	1	Not used
Programming Errors	23	8	Any device-related error
	2	4	Not used
	21	2	Not used
	20	1	Not used
	19	8	Device not blank (20)
	18	4	Illegal bit (21)
	17	2	Nonverify (23, 24, 2B, 2C, A2)
	16	1	Incomplete programming (22, 2A, 30 or 31)
I/O Errors	15	8	I/O error (46)
	14	4	Not used
	13	2	Not used
	12	1	Compare error (52)
	11	8	Sumcheck error (82)
	10	4	Record-type error (94)
	9	2	Address error (27)
	8	1	I/O Format error (84, 90)
Unused	7	8	Not used
	6	4	Not used
	5	2	Not used
	4	1	Not used
	3	8	Not used
	2	4	Not used
	1	2	Not used
	0	1	Not used

Example: What errors are indicated in this error status word: **80888000** ?

8 — the word contains error information
0 — no receive errors
8 — device related error
8 — device is not blank (error 20)
8 — I/O error
0 — no errors
0 — no errors
0 — no errors

Note: 1. *The numbers in parentheses are UniSite error codes, defined in the error codes section.*
2. *An error can cause as many as 3 bits to be high: the bit which represents the error, the most significant bit of the 8-bit word in which the error bit occurs, and the bit 31.*
3. *After being read, the error-status word resets to zero.*

CRC ERROR CODES

Following is a list of hex error codes that appear while UniSite is being operated in the computer remote control mode. These error codes will be returned by UniSite to a host computer after UniSite receives the "X" command from the host. The host should normally send the "X" command after UniSite sent an "F" response to the host from a previous command. The list is in numerical order, according to the hex error code (left column).

1F **Cannot erase device error** —This error code appears after UniSite was not able to erase an EEPROM. The device may be defective; try another device.

20 **Non-blank device** —This error code appears after UniSite has performed a blank check on a device and has detected bits that are not in their erased or blank state, and are not illegal bits. This error is the result of either the 'B' (Blank Check) command or a 'P' (Program) command with the blank check option set previously by the extended command '2A' (Enable Programming Option).

21 **Illegal bit error** —This error code appears when UniSite has detected a device that has a bit programmed to the incorrect state. When this error code appears, try erasing the part (if possible) and then attempt to program the part again. If this error code continues to appear, it may be because the device is defective. Discard the part and try another device. The illegal-bit check error occurs as the result of either a 'T' (Illegal Bit Check) command or a 'P' (Program) command with the illegal bit option set previously by the extended command '2A' (Enable Programming Option).

22 **Device programming error** —This error code appears when UniSite detected a defective memory cell in a device during the programming operation. If this error code appears, try another device.

Note: The two following errors have the same error code. In order for either error to appear, you must have selected command x23] (SELECT VERIFY OPTION). If "1" was specified as the variable, use the first description. If "2" was specified, use the second description.

23 **Verify data error (Vcc Nominal)** —This error code appears when UniSite has performed a Verify and has found a memory cell that was not programmed correctly. The device was verified while being operated with its normal operating voltage applied. When this error code appears, try another device.

23 **Verify data error (Vcc low)** — This error code appears when UniSite has performed a Verify and has found a memory cell that was programmed incorrectly. The device was verified while being operated with its lowest operating voltage applied. When this error code appears, attempt to program the device again. If this error code reappears, try a different device.

24 **Verify data error (Vcc high)** —This error code appears when UniSite has performed a Verify and has found a memory cell that was programmed incorrectly. The device was verified while being operated with its high operating voltage applied. When this error code appears, attempt to program the device again. If this error code reappears, try a different device.

27 **End of user RAM exceeded** — There is not enough user RAM for the amount of data you want to Load into it or program from it. You may have the device block size set too large, or the beginning RAM address too high. The operation may still be performed, but only part of the device will be programmed.

28 **Fatal device-specific programming error** —Generic error code generated by the device-specific algorithm. No further commands hould be attempted until the error condition is corrected.

29 **Non-fatal device-specific programming error** — Generic error code generated by the device-specific algorithm. This error is non-fatal and is for information purposes only. In most cases, the operation was performed successfully. See "Device-Specific Error Messages" at the end of this section.

2A **Device Insertion error** When this error code appears, the problem may be one of the following: either the device socket is not in the locked position, the device is inserted backwards or is not bottom-justified in the socket, or the device pins are not making good contact. Check the device's continuity in the socket and then try to program the part again. If the same error code appears, try a different device.

Note: The two following errors have the same error code. In order for either error to appear, you must have previously selected command x23] - where x = 0, 1, or 2. If a 0 is chosen, there will be no error condition. (SELECT VERIFY OPTION). If "1" was specified as the variable, use the first description. If "2" was specified, use the second description.

2B **Structured test error (Vcc Nominal)** - This error code appears when UniSite has performed a functional test on a logic device and has detected a failure. If you had selected "1" as the number of Verify Passes, UniSite was attempting to verify the logic device at its normal operating voltage. When this error code appears, try another device.

2B **Structured test error (Vcc low)** – This error code appears when UniSite has performed a functional test on a logic device at the low voltage and has detected a failure. If you had selected "2" for the number of Verification passes, one pass is performed while the lowest specified operating voltage is applied to the device, and the second pass is performed while the highest specified operating voltage is applied to the device. When this error code appears, try another device.

2C **Structured test error (Vcc high)** – This error code appears when UniSite has performed a functional test of a logic device at the high voltage and detected a failure. If you had selected "2" for the number of Verification passes, one pass is performed while the lowest specified operating voltage is applied to the device, and the second pass is performed while the highest specified operating voltage is applied to the device. When this error code appears, try another device.

2D **FSM/PSM for device not installed**—The device you selected cannot be programmed in the PSM or FSM that is presently installed. If you select a device that is not supported by an installed PSM or FSM, no device operations can be performed. Install the correct module and try again.

2E **Programming Hardware hasn't passed self-test**—This error occurs when a programming operation is attempted and the self-test had previously failed for critical hardware. Return to local mode and check the self-test screen.

2F **Insufficient pin driver boards installed for the device selected.**— The device you are trying to load, program, verify or check requires more Pin Driver boards than are installed in your UniSite.

30	**Device algorithm not found**— This error code will occur if device selection is attempted using family/pinout codes, and the codes selected correspond to an algorithm which is not supported by UniSite. This error code will also occur when a device operation is attempted prior to having a device selected.
31	**Device over-current fault**— This error code appears when you attempt to program a socketed device whose programming current is higher than the device you selected on-screen. The device may be faulty; insert another device into the socket and try the operation again.
3B	**No device present.** This error code is returned after the executed command "DC]" is sent and no device is found to be in the socket.
40	**I/O initialization error**—An attempt to initialize the remote port with parameters has failed. Check connections and attempt the operation again.
41	**Serial-framing error** — The remote serial interface detected a start bit, but the stop bit was incorrectly positioned. Check the baud rate and stop bit setting for the remote port, or use hardware handshaking.
42	**Serial-overrun error** — The remote serial interface received characters that UniSite was unable to service. Check the baud rate and stop bit settings for the remote port, or use hardware handshaking.
43	**Serial framing/overrun error** — This is a combination of serial-framing error 0x41 and overrun error 0x42. Check the baud rate and stop bit settings for the remote port, or use hardware handshake.
46	**I/O timeout** — Too much time passed before UniSite received a data file during a download operation. The I/O timeout period may be changed via the Select I/O Timeout Command (=).
52	**Data verify error** — The data from the remote port did not match the data in RAM. Check the data and try the operation again.
75	**Security Fuse Violation** — If you tried to load, program or verify data from a device that has its security fuse programmed, this error code may appear. If this error code appears, use a master device whose security fuse is still intact.
77	**Security fuse programming error** — This error code will appear if UniSite cannot program the security fuse. If this error code appears, the device you are trying to program may be defective; try programming another device.
79	**Preload not supported by this device** — This error code appears when a preload vector in the programming data cannot be applied to the logic device.
81	**Serial-parity error** — The remote serial interface detected incoming data that had incorrect parity. Check the parity setting for the remote port.

82 **Checksum error** — The checksum of the data received (as the result of a download) did not match the checksum downloaded from the host computer. The host computer sends a transmission checksum, and possibly a fuse map checksum, as part of the data record. UniSite compares those checksums with the checksums it created on that same data. If the two checksums do not match, this error code will appear, indicating that some of the data transmitted by the host was not received by UniSite, Try the operation again, and if the problem continues, verify that the checksums generated from the host are correct. If the checksums are correct, consult your UniSite Service Manual or contact your nearest Data I/O Service Center.

84 **I/O format error** – There is a compatibility problem with the data translation format you are using. Check the format of the data. The Computer Remote Control section of the UniSite Operator's manual contains a description of all the data translation formats supported by UniSite. Or try sending a different translator format. If format 04 is selected, this error can indicate an illegal parameter error. Since this format is a word-oriented format, the following parameters must be set to even values; I/O offset, memory begin address, user data size and upload record size.

88 **Invalid number of parameters** — This error will be generated when a CRC command is preceded by an invalid number of parameters. Check the parameters preceding the command and re-issue the command.

89 **Illegal parameter value** — This error code will appear if an illegal parameter precedes a CRC command. Verify that the parameter is within the range specified for the command.

8B **Error restoring/saving CRC user-defined parameters or restoring CRC entry defaults.** — An error has occurred while attempting to restore or save CRC user-defined parameters (commands FD or FE) or restoring CRC entry defaults (command FC). Check to make sure the disk is not write-protected and that the valid system disk is in drive A.

8E **File error** — A disk file error has occurred during a command that accesses a disk file, such as load file from disk, yield tally operations (command 43]) or device selection. If you are doing a Load File from Disk operation, the file probably does not exist. Check the filename. If you are doing a yield tally operation or a device selection, the disk may be write-protected. Remove the write-protection and try the operation again. This error code also occurs when you are performing a SAVE CONFIGURATION operation and the Algorithm Save area is exceeded.

8F **NON-JEDEC data present in RAM or disk file or else a NON-logic device was selected with a JEDEC I/O format selected.** — If you are doing a device operation or a Load File From Disk operation, check your JEDEC data. If you are doing an upload operation, select the logic device for the JEDEC file to be uploaded or select a different I/O format for a memory device.

90	**Illegal I/O format** —You tried to select an I/O format that is not supported by UniSite or you attempted to select a non-JEDEC format when a logic device was selected. Select a valid format. See the Translation Formats section for a list of supported formats.
94	**Data record error**—The data that you attempted to transfer did not conform with the selected translation format; edit the data file so that it matches one of UniSite's supported translator formats. See the Translation Formats section for output samples of each translator.
97	**Block move error** —A block move within RAM has violated the RAM boundaries. Check the memory begin address and memory block size and try the operation again.
98	**End of device exceeded**—There is not enough room in the device to hold all the data you have specified. You may have the device beginning address set too high, the block size set too high, or you may need a larger device. Although the operation may still be performed, only part of the data will be programmed into the device.
99	**End of file exceeded**— This error code appears when the memory block size and memory begin address parameters you specified in the Programming screen are too large for the data file you intend to use for programming. When this error code appears, change the memory block size and memory begin address file size parameters so they are small enough to accommodate the data file. You can perform the operation without changing anything, but only part of the device will be programmed.
9A	**Algorithm diskette cannot be found**—This code will be returned if you are selecting a device and do not have UniSite's Algorithm diskette installed. Insert the Algorithm disk in drive A or B and send the device selection command again.
9B	**Incompatible system/algorithm disks** —The version number of the Algorithm disk does not match the version number of the System disk. Insert the correct version of the Algorithm disk and try the operation again.
9C	**Invalid command for this mode** —The command received is not valid in "single device" mode: it is a "set/gang" mode command. This error will also be returned if the set mode is not enabled or a non-gangable device is selected. Either select a different command, select "set/gang" mode, or select a different device.
9D	**I/O address beyond range of data format selected** — An I/O address exceeded the highest value allowed in the address field of the data format selected. Prior to performing an upload or output to disk operation the programmer calculates the highest I/O address that will be output based on the parameters supplied by the user and aborts the operation if the I/O address is too large for the data format selected. The formula for calculating the highest I/O address is:

Highest I/O address = I/O addr offset + User data size -1

To avoid this error condition either select a different data format (one which will support the I/O addresses for the transfer operation) or decrease the value of the I/O offset address and /or the User data size to achieve I/O addresses within the range of the data format selected. The I/O addr offest parameter is considered an unsigned value, also if it is set to the special default value of FFFFFFFF it is treated as a value of 0.

A1 — **No Electronic ID** — The device does not contain an electronic ID. Turn off the Electronic ID option or change devices.

A2 — **Electronic ID verify error** — The device you tried to program did not have the correct electronic ID. Insert the correct device in the socket, or select a different device.

B2 — **Partial device operation not allowed** — This error is returned when block limits other than the defaults are used for a device that only supports the defaults. In this case, the block size must be equal to or greater than the device size.

D1 — **RAM file buffer exceeded**—A data write was attempted beyond the end of a previously allocated RAM file.

D2 — **RAM file not found**— An operation such as device program operation was attempted using a RAM file but the RAM file could not be found in memory.

D3 — **RAM file create error**— An attempt was made to create a RAM file but the attempt was unsuccessful. Possible explanations are: an illegal file name was used or the file name already exists.

D4 — **RAM file space exhausted**— An attempt was made to create a RAM file but the attempt was unsuccessful. Possible explanations are: there was not enough RAM space remaining for RAM files or therewas not enough directory entries left for RAM files.

FE — **Undefined error**—An error occurred that the CRC program could not categorize. Document the method in which the error occurred and call Data I/O to report the problem.

FF — **Operation Aborted** - This code will be returned if the SetSite operation being performed was halted prematurely. For example, if you were programming devices and pulled the SetSite socket lever up to the OPEN ("stop") position.

6 *Translation Formats*

Introduction

Data translation formats are different ways of encoding the data in a data file. A data file contains the information to be programmed into a device. The data file could contain the fuse pattern and test vectors for a logic device or the data for a memory device.

Generally, the data, such as the fuse pattern for a logic device, is created on a development platform and is then stored is a particular data translation format. When you want to transfer the data file to UniSite, you will need to set up UniSite to handle the right translation format. During download, UniSite translates the formatted data and stores it in user memory as a binary image. You can use either remote control or UniSite's terminal. When using CRC, set the format code by using the "nnnA" command described in the previous section.

About This Chapter

This chapter describes all the translation formats that UniSite supports. This chapter does not cover how to select an individual translation format. For information on how to select a data translation format, see Sample Sessions in Section 2.

Below you will find a list, in numberical order, of all the translation formats supported by UniSite. Following the list is a description and, in most cases, an example of each translation format, presented in order by format number.

Format	Code	Format	Code
ASCII-BNPF	01 (05*)	MOS Technology	81
ASCII-BHLF	02 (06*)	Motorola Exorciser	82
ASCII-B10F	03 (07*)	Intel Intellec 8/MDS	83
Texas Instruments SDSMAC (320)	04	Signetics Absolute Object	85
5-level BNPF	08 (09*)	Tektronix Hexadecimal	86
Binary	10	Motorola Exormax	87
DEC Binary	11	Intel MCS-86 Hex Object	88
Spectrum	12 (13*)	Hewlett-Packard 64000 Absolute	89
POF	14	Texas Instruments SDSMAC	90
ASCII-Octal Space	30 (35**)	Jedec format (Full)	91
ASCII-Octal Percent	31 (36**)	Jedec format (Kernel)	92
ASCII-Octal Apostrophe	32	Tektronix Hexadecimal Extended	94
ASCII-Octal SMS	37	Motorola 32 bit (S3 record)	95
ASCII-Hex Space	50 (55**)	Hewlett-Packard UNIX Format	96
ASCII-Hex Percent	51 (56**)	Intel OMF 386	97
ASCII-Hex Apostrophe	52	Intel OMF 286	98
ASCII-Hex SMS	57	Intel Hex-32	99
ASCII-Hex Comma	53 (58**)		
RCA Cosmac	70		
Fairchild Fairbug	80		

* *This alternate code is used to transfer data without STX start code and EXT end code.*

** *This is alternate code is used to transfer data using SOH start code instead of usual STX.*

Instrument Control Codes

The instrument control code is a 1-digit number that signals or controls data transfers. Specifically, the instrument control code can be used to implement a form of remote control that provides peripherals with flow control beyond that provided by software handshaking. When using computer remote control, the instrument control code is sent immediately preceding the 2-digit format code. The three values of the instrument control code and associated functions are described below.

0 – Handshake Off

Input Function: Send "X-OFF" to stop the incoming transmission. Send "X-ON" to resume transmission.

Output Function: Data transmission will be halted upon receipt of an "X-OFF" character; transmission will resume upon receipt of an "X-ON"character.

1 – Handshake On

Input Function: Transmit an "X-ON" character when ready to receive data; transmit "X-OFF" if the receiver buffer is full; transmit an "X-ON if the receiver buffer is empty; transmit an "X-OFF" after all the data is received.

Output Function: Transmit a "PUNCH ON" character prior to data transmission. Data transmission will be halted upon receipt of an "X-OFF" character and will resume upon receipt of an "X-ON" character. A "PUNCH OFF" character is sent when the transmission is completed.

2 – X-ON/X-OFF	Input Function	Send "X-OFF" to stop the incoming transmission. Send "X-ON" to resume transmission.
	Output Function:	Transmit data only after receiving an "X-ON" character. Data transmission will be halted upon receipt of an "X-OFF" character; transmission will resume upon receipt of an "X-ON" character.

Note: "X-ON" character is a CTRL-Q, or 11 hex.
"X-OFF" character is a CTRL-S, or 13 hex.
"PUNCH-ON" character is a CTRL-R, or 12 hex.
"PUNCH-OFF" character is a CTRL-T, or 14 hex.

General Notes

Some information about data translation is listed below:

Aborting a Data Transfer

To abort a data transfer at any time, type Ctrl - Z from the terminal. In CRC mode, send Esc or Break.

Compatibility

When translating data, you may use any remote source that produces formats compatible with the descriptions listed in this section.

Hardware Handshaking

Hardware handshaking may be used if compatible with the host interface. Refer to the Computer Remote Control section of this manual for a description of the UniSite interface.

Leader/Trailer

During output of all formats except 89 (HP 64000), a 50-character leader precedes the formatted data and a 50-character trailer follows. This leader/trailer consists of null characters. If the null count parameter is set to FF hex, then the leader/trailer is not output. To set the null count while in terminal mode, go to the More commands/configure/edit/ communication parameters screen and set the number of nulls parameter. If in CRC mode use the CRC "U" command to set the null count.

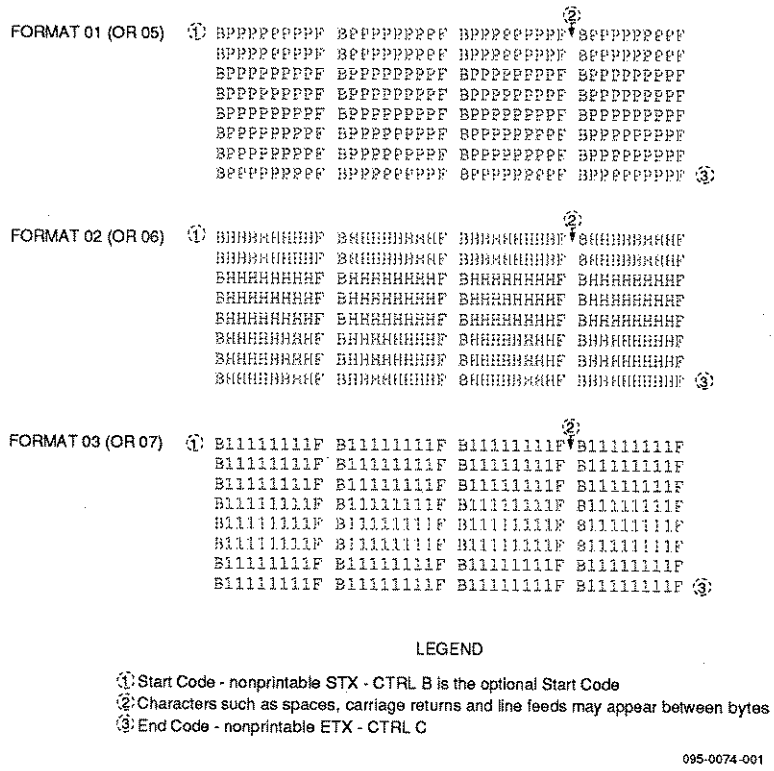
Note: Binary formats 10, 11, and 89 do not function properly unless you select NO parity, and 8-bit data.

ASCII Binary Format, Codes 01, 02 and 03 (or 05, 06 and 07)

In these formats, bytes are recorded in ASCII codes with binary digits represented by N's and P's, L's and H's, or 1's and 0's, respectively. See the figure. The ASCII Binary formats do not have addresses.

The figure shows sample data bytes coded in each of the three ASCII Binary formats. Incoming bytes are stored in RAM sequentially starting at the first RAM address. Bytes are sandwiched between "B" and "F" characters and are separated by spaces.

Figure 6-1
An Example of ASCII Binary Format



Data can also be expressed in 4-bit words. UniSite will generate the 4-bit format on upload if the data word width is 4 bits. Any other characters, such as carriage returns or line feeds, may be inserted between an "F" and the next "B".

The start code is a nonprintable STX, which is a CTRL-B (the same as a hex 02). The end code is a nonprintable ETX, which is a CTRL-C (the same as a hex 03).

Note: Data without a start or end code may be input to or output from UniSite by use of alternate data translation format codes. These are: ASCII-BNPF, 05; ASCII-BHLF, 06; ASCII-B10F, 07.

A single data byte can be aborted if UniSite receives an "E" character between "B" and "F" characters. Data will continue to be stored in sequential RAM addresses. Data is output in 4-byte lines with a space between bytes.

Texas Instruments SDSMAC Format (320), Code 04

Data files in the SDSMAC (320) format consist of a start-of-file record, data records, and an end-of-file record. See the figure. The format is used for Texas Instruments' 320 line of processors. It is very similar to format 90 with the only difference being that the address fields represent 16 bit data words rather than bytes.

Each record is composed of a series of small fields, each initiated by a tag character. UniSite recognizes and acknowledges the following tag characters:

0 or K - followed by a file header.

7 - followed by a checksum which UniSite acknowledges.

8 - followed by a checksum which UniSite ignores.

9 - followed by a load address which represents a word location.

B - followed by 4 data characters (16-bit word).

F - denotes the end of a data record.

* - followed by 2 data characters.

The start-of-file record begins with a tag character and a 12-character file header. The first four characters are the word count of the 16-bit data words; the remaining file header characters are the name of the file and may be any ASCII characters (in hex notation). Next come interspersed address fields and data fields (each with tag characters). The address fields represent 16 bit words. If any data fields appear before the first address field in the file, the first of those data fields is assigned to address 0000. Address fields may be expressed for any data word, but none are required.

The record ends with a checksum field initiated by the tag character 7 or 8, a 4-character checksum, and the tag character F. The checksum is the two's complement of the sum of the 8-bit ASCII values of the characters, beginning with the first tag character and ending with the checksum tag character (7 or 8).

Data records follow the same format as the start-of-file record but do not contain a file header. The end-of-file record consists of a colon (:) only. The output translator sends a [CTRL] – [S] after the colon.

During download or input from disk operations the destination address for the data will be calculated in the following manner:

Memory address =
(load address x 2) – I/O address offset + begin address

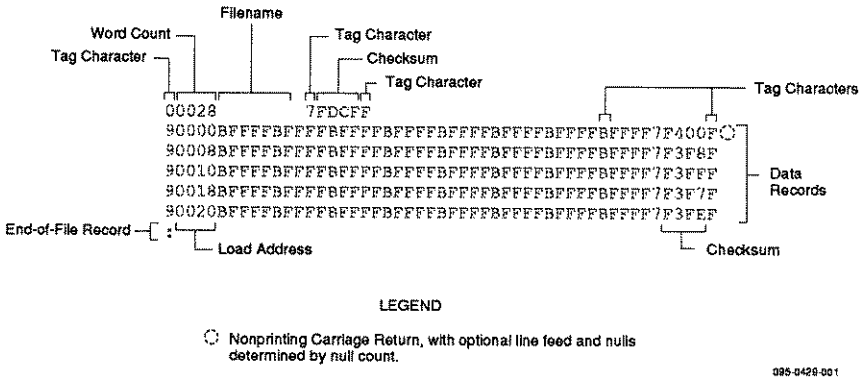
During upload or output to disk operations the load address sent with each data record is calculated in the following manner:

Load address = I/O address offset / 2

The Memory begin address, I/O address offset and User data size parameters represent bytes and must be even values for this format. The upload record size must also be even for this format (default is 16).

Note: If the data will be programmed into a 16-bit device to be used in a TMS320 processor based system, the odd/even byte swap switch must be enabled.

Figure 6-2
An Example of TI SDSMAC FormatS



The 5-Level BNPF Format, Codes 08 or 09

Except for the start and end codes, the same character set and specifications are used for the ASCII-BNPF and 5-level BNPF formats.

Data for input to UniSite is punched on 5-hole Telex paper tapes to be read by any paper tape reader that has an adjustable tape guide. The reader reads the tape as it would an 8-level tape, recording the 5 holes that are on the tape as 5 bits of data. The 3 most significant bits are recorded as if they were holes on an 8-level tape. Tape generated from a telex machine using this format can be input directly to a serial paper tape reader interfaced to UniSite. UniSite's software converts the resulting 8-bit codes into valid data for entry in RAM.

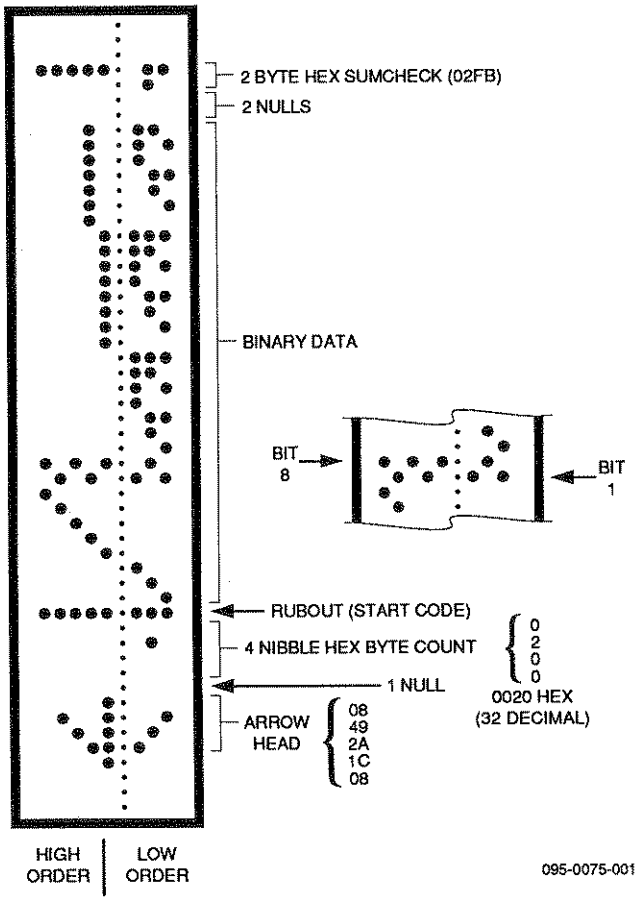
The start code for the format is a left parenthesis, ("Figs K" on a telex machine), and the end code is a right parenthesis, ("Figs L" on a telex machine). The 5-level BNPF format does not have addresses.

Note: Data without a start or end code may be input to or output from UniSite by use of the alternate data translation format code, 09. This format accepts an abort character (10 hex) to abort the transmission.

Binary Transfer, Code 10

Data transfer in the Binary format consists of a stream of 8-bit data words preceded by a byte count and followed by a sumcheck. The Binary format does not have addresses.

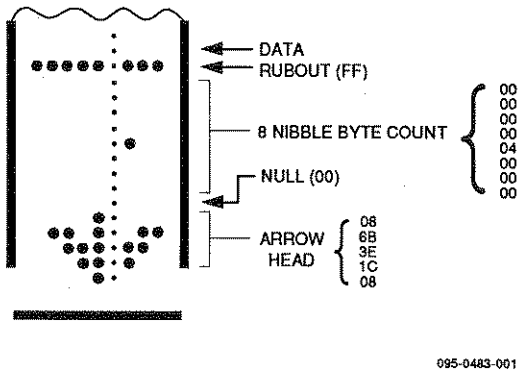
Figure 6-3
An Example of Binary Format



UniSite stores incoming binary data upon receipt of the start character. Data is stored in RAM starting at the first RAM address specified by the "Memory Begin Address" parameter and ending at the last incoming data byte.

A paper tape generated by a programmer will contain a 5-byte, arrow-shaped header followed by a null and a 4-nibble byte count. The start code, an 8-bit rubout, follows the byte count. The end of data is signaled by two nulls and a 2-byte sumcheck of the data field. Refer to the figure.

Figure 6-4
An Example of Binary Format



If the data output has a byte count GREATER than or equal to 64K, an alternate arrow-shaped header is used. This alternate header (shown below) is followed by an 8-nibble byte count, sandwiched between a null and a rubout. The byte count shown here is 40000H (256K decimal). If the byte count is LESS than 64K, the regular arrowhead is used instead. Data that is input using Binary format will accept either version of this format.

In addition, a third variation of this binary format is accepted on download. This variation does not have an arrowhead and is accepted only on input. The rubout begins the format and is immediately followed by the data. There is no byte count or sumcheck.

DEC Binary Format, Code 11

Data transmission in the DEC Binary format is a stream of 8-bit data words with no control characters except the start code. The start code is one null preceded by at least one rubout. A tape output from UniSite will contain 32 rubouts in the leader. The DEC Binary format does not have addresses.

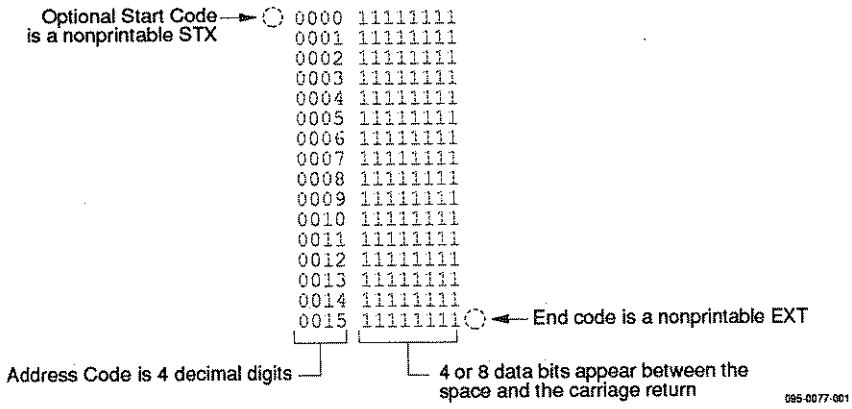
Spectrum Format, Codes 12 or 13

In this format, bytes are recorded in ASCII codes with binary digits represented by 1's and 0's. During output, each byte is preceded by a decimal address.

The figure shows sample data bytes coded in the Spectrum format. Bytes are sandwiched between the space and carriage return characters and are normally separated by line feeds. The start code is a nonprintable STX, CTRL-B (or hex 02), and the end code is a nonprintable ETX, CTRL-C (or hex 03).

Note: Data without a start or end code may be input to or output from UniSite by use of the alternate data translation format code, 13.

Figure 6-5
An Example of Spectrum Format



POF Format (Programmer Object File), Code 14

The Programmer Object File format (POF) provides a highly compact data format to enable translation of high bit count logic devices efficiently. This format currently applies to the Altera 5032 device.

The information contained in the file is grouped into "packets". Each packet contains a "tag", identifying what sort of data the package contains plus the data itself. This system of packeting information allows for future definitions as becomes required.

The POF file is composed of a header and a list of packets. The packets have variable lengths and structures, but the first six bytes of every packet always adheres to the following structure.

```
struct PACKET_HEAD
{
short tag;                    /*tag number - type of packet */
long length;                  /*number of bytes in rest of packet */
}
```

A POF file is read by the program examining each packet and if the tag value is recognized, then the packet is used. If a tag value is not recognized, the packet is ignored.

Any packet except the terminator packet may appear multiple times within a POF file. Packets do not need to occur in numerical tag sequence. The POF reader software is responsible for the interpretation and action taken as a result of any redundant data in the file including the detection of error conditions.

The POF format currently uses the following packet types.

Note: In the following packet type descriptions, one of the terms: Used, Skipped, or Read will appear after the tag and name.

Used: The information in this packet is used by UniSite.
Skipped: This information is not used by UniSite.
Read: This information is read by UniSite but has no direct application.

Creator_ID tag = 1 Used
This packet contains a version ID string from the program which created the POF file.

Device_Name tag = 2 Used
This packet contains the ASCII name of the target device to be programmed, for example, PM9129.

Comment_Text tag = 3 Read
This packet contains a text string which may consist of comments of documentation related to the POF file. This text may be displayed to the operator when the file is read. The string may include multiple lines of text, separated by appropriate new line characters.

Tag_Reserved tag = 4 Skipped

Security_Bit tag = 5 Used
This packet declares whether security mode should be enabled on the target device.

Logical_Address_and_Data tag = 6 Read
This packet defines a group of logical addresses in the target device and associates logical data with these addresses. The addresses comprise a linear region in the logical address space, bounded on the low end by the starting address, and extending upward by the address count specified in the packet.

Electrical_Address_and_Data tag = 7 Used
This packet defines a group of electrical addresses in the target device and associates data values with those addresses. The data field is ordered in column-row order, beginning with the data for the least column-row address, continuing with increasing row addresses until the first column is filled, then incrementing the column address, etc.

Terminator tag = 8 Used

This packet signals the end of the packet list in the POF file. This packet must be the N-th packet, where N is the packet count declared in the POF header. The CRC field is a 16-bit Cyclic Redundancy Check computed on all bytes in the file up to, but not including, the CRC value itself. If this CRC value is zero, the CRC check should be ignored.

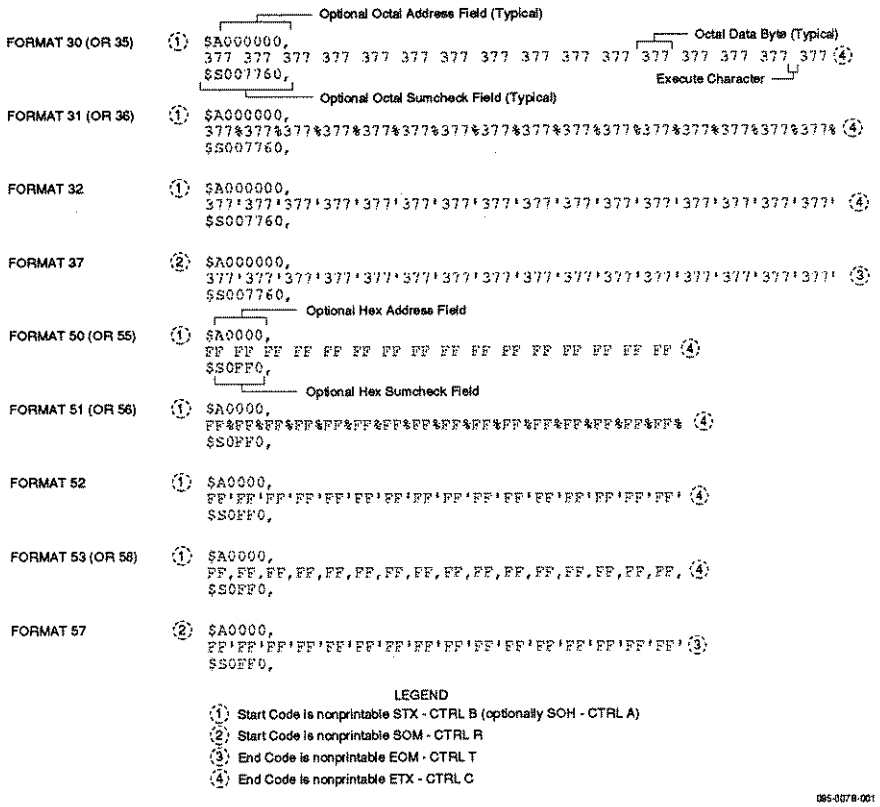
Symbol table tag = 9 Skipped

Test Vectors	tag = 10	Accepted but not used
	This packet allows the POF to contain test vectors for post programming testing purposes. Each vector is a character string and uses the 20 character codes for vector bits defined in JEDEC standard 3A, section 7.0.	
Electrical_ Address_and_ Constant_data	tag = 12	Skipped
Number of programmable elements	tag = 14	Read
	This packet defines the number of programmable elements in the target device.	

ASCII Octal and Hex Formats, Codes 30-37 and 50-58

Each of these formats has a start and end code, and similar address and checksum specifications. The figure illustrates 4 data bytes coded in each of the 9 ASCII Octal and Hexadecimal formats. Data in these formats is organized into sequential bytes separated by the execute character (space, percent, apostrophe, or comma). Characters immediately preceding the execute character are interpreted as data. ASCII Octal and Hex formats can express 8-bit data, by 3 octal, or 2 hexadecimal characters. Line feeds, carriage returns and other characters may be included in the data stream as long as a data byte directly precedes each execute character.

Figure 6-6
An Example of ASCII Octal and Hex Formats



Although each data byte has an address, most are implied. Data bytes are addressed sequentially unless an explicit address is included in the data stream. This address is preceded by a "$" and an "A", must contain 2 to 8 hex or 3 to 11 octal characters, and must be followed by a comma, except for the ASCII-Hex (Comma) format, which uses a period. UniSite skips to the new address to store the next data byte; succeeding bytes are again stored sequentially.

Each format has an end code, which terminates input operations. However, if a new start code follows within 16 characters of an end code, input will continue uninterrupted. If no characters come within 2 seconds, input operation is terminated.

After receiving the final end code following an input operation, the 2900 calculates a sumcheck of all incoming data. Optionally, a sumcheck can also be entered in the input data stream. UniSite compares this sumcheck with its own calculated sumcheck. If they match, UniSite will display the sumcheck; if not, a sumcheck error will be displayed.

Note: The sumcheck field consists of either 2-4 hex or 3-6 octal characters, sandwiched between "$" and "," characters. The sumcheck immediately follows an end code. The sumcheck is optional in the input mode but is always included in the output mode. The most significant digit of the sumcheck may be 0 or 1 when expressing 16 bits as 6 octal characters.

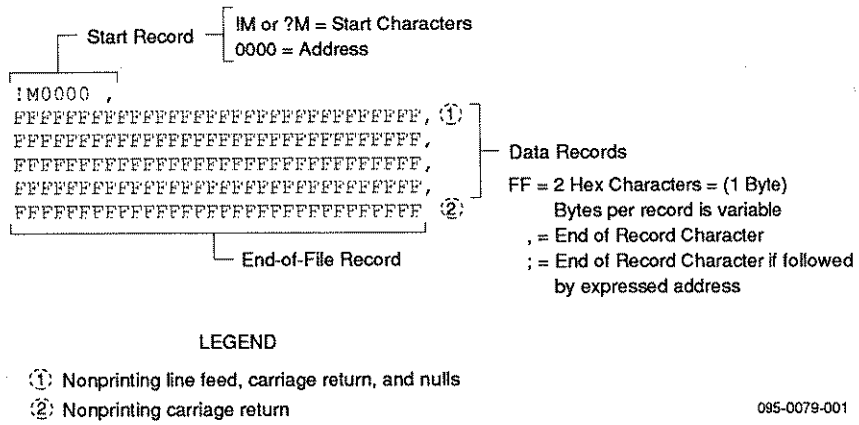
UniSite divides the output data into 8-line blocks. Data transmission is begun with the start code, a nonprintable STX character, or optionally, SOH.* Data blocks follow, each one prefaced by an address for the first data byte in the block. The end of transmission is signaled by the end code, a nonprintable ETX character. Directly following the end code is a sumcheck of the transferred data.

* *ASCII-Octal SMS and ASCII-Hex SMS use SOM (CTRL-R) as a start code and EOM (CTRL-T) as an end code.*

RCA Cosmac Format, Code 70

Data in this format begins with a start record consisting of the start character (!M or ?M), an address field, and a space. See the figure.

Figure 6-7
An Example of RCA Cosmac Format



The start character ?M is sent to UniSite by a development system, followed by the starting address, and a data stream which conforms to the data input format described in the ASCII-Hex and Octal figure. Transmission stops when the specified number of bytes have been transmitted.

Address specification is required for only the first data byte in the transfer. An address must have 1 to 4 hex characters and must be followed by a space. UniSite records the next hexadecimal character after the space as the start of the first data byte. (A carriage return must follow the space if the start code ?M is used.) Succeeding bytes are recorded sequentially.

Each data record is followed by a comma if the next record is not preceded by an address, or by a semicolon if it starts with an address. Records consist of data bytes expressed as 2 hexadecimal characters and followed by either a comma or semicolon, and a carriage return. Any characters received between a comma or semicolon and a carriage return will be ignored by UniSite.

The carriage return character is significant to this format because it can signal either the continuation or the end of data flow; if the carriage return is preceded by a comma or semicolon, more data must follow; the absence of a comma or semicolon before the carriage return indicates the end of transmission.

Output data records are followed by either a comma or a semicolon and a carriage return. The start-of-file records are expressed exactly as for input.

Fairchild Fairbug, Code 80

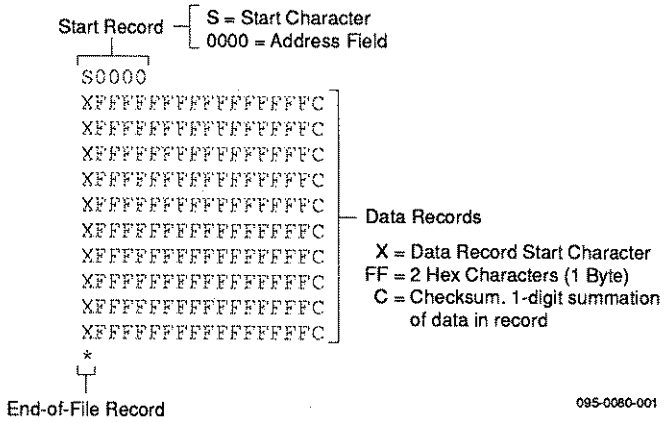
In the Fairbug format, input and output requirements are identical; both have 8-byte records and identical control characters. The figure shows a Fairbug data file. A file begins with a 5-character prefix and ends with a 1-character suffix. The start-of-file character is an "S", followed by the address of the first data byte. Each data byte is represented by 2 hexadecimal characters. UniSite will ignore all characters received prior to the first "S".

Note: Address specification is optional in this format; a record with no address directly follows the previous record.

Each data record begins with an "X", and always contains 8 data bytes. A 1-digit hexadecimal checksum follows the data in each data record. The checksum represents, in hexadecimal notation, the sum of the binary equivalents of the 16 digits in the record; the half carry from the fourth bit is ignored.

UniSite ignores any character (except for address characters and the "*" which terminates the data transfer) between a checksum and the start character of the next data record. This space can be used for comments.

Figure 6-8
An Example of Fairchild Fairbug



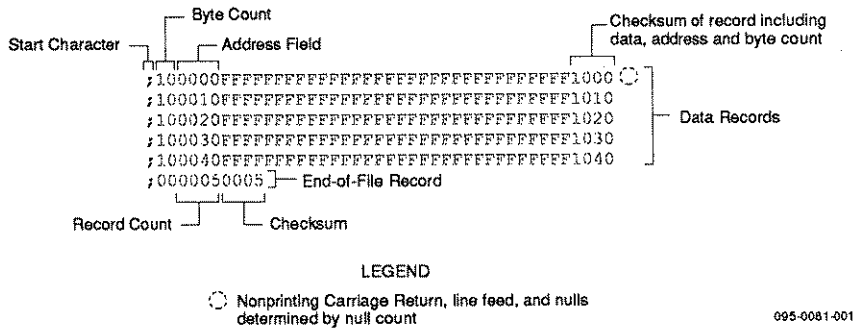
The last record consists of an asterisk only, which indicates the end of file.

MOS Technology Format, Code 81

The data in each record is sandwiched between a 7-character prefix and a 4-character suffix. The number of data bytes in each record must be indicated by the byte count in the prefix. The input file can be divided into records of various lengths.

The figure shows a series of valid data records. Each data record begins with a semicolon. UniSite will ignore all characters received prior to the first semicolon. All other characters in a valid record must be valid hexadecimal digits (0-9 and A-F). A 2-digit byte count follows the start character. The byte count, expressed in hexadecimal digits, must equal the number of data bytes in the record. The byte count is greater than zero in the data records, and equals zero (00) in the end-of-file record. The next 4 digits make up the address of the first data byte in the record. Data bytes follow, each represented by 2 hexadecimal digits. The end-of-file record consists of the semicolon start character, followed by a "00" byte count, the record count and a checksum.

Figure 6-9
An Example of MOS Technology Format

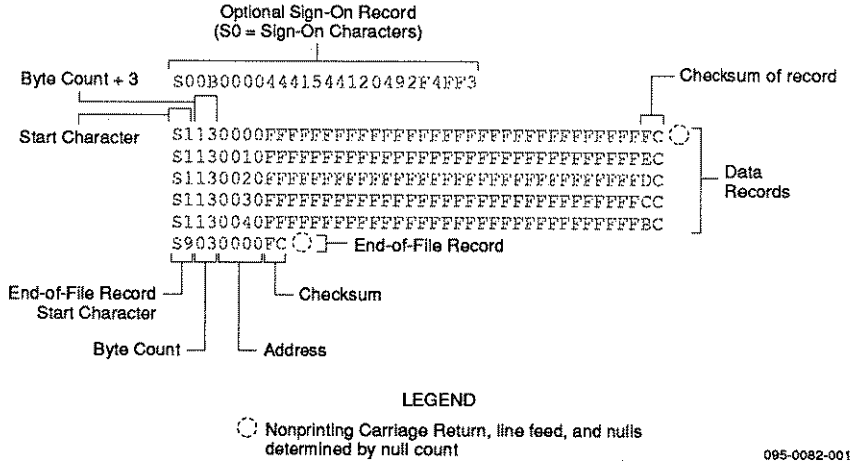


The checksum, which follows each data record, is a 2-byte binary summation of the preceding bytes in the record (including the address and byte count), in hexadecimal notation.

Motorola EXORciser Format, Code 82

Motorola EXORciser data files may begin with an optional sign-on record, which is initiated by the start characters "S0." Valid data records start with an 8-character prefix and end with a 2-character suffix. The figure shows a series of valid Motorola data records.

Figure 6-10
An Example of Motorola EXORciser Format



Each data record begins with the start characters "S1"; The third and fourth characters represent the byte count, which expresses the number of data, address and checksum bytes in the record. The address of the first data byte in the record is expressed by the last 4 characters of the prefix. Data bytes follow, each represented by 2 hexadecimal characters. The number of data bytes occurring must be three less than the byte count. The suffix is a 2-character checksum, which equals the one's complement of the binary summation of the byte count, address and data bytes.

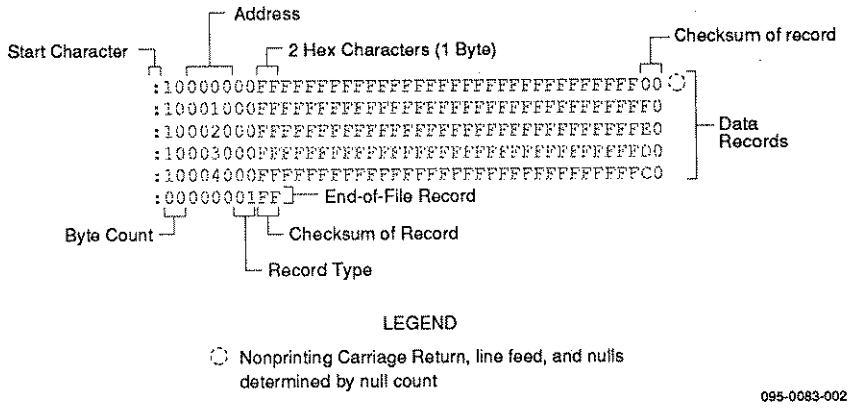
The end-of-file record consists of the start characters "S9", the byte count, the address (in hex) and a checksum. The maximum record length is 250 data bytes.

Intel Intellec 8/MDS Format, Code 83

Intel data records begin with a 9-character prefix and end with a 2-character suffix. The byte count must equal the number of data bytes in the record.

The figure simulates a series of valid data records. Each record begins with a colon, which is followed by a 2-character byte count. The 4 digits following the byte count give the address of the first data byte. Each data byte is represented by 2 hexadecimal digits; the number of data bytes in each record must equal the byte count. Following the data bytes of each record is the checksum, the two's complement (in binary) of the preceding bytes (including the byte count, address, record type and data bytes), expressed in hex.

Figure 6-11
An Example of Intel Intellec 8/MDS Format

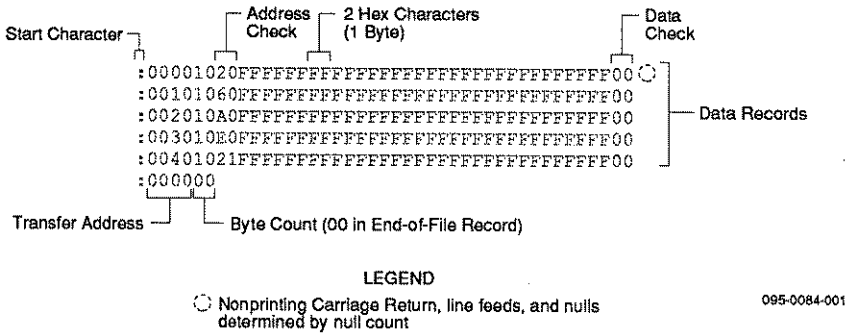


The end-of-file record consists of the "colon" start character, the byte count (equal to "00"), the address, the record type (equal to "01") and the checksum of the record.

Signetics Absolute Object Format, Code 85

The figure shows the specifications of Signetics format files. The data in each record is sandwiched between a 9-character prefix and a 2-character suffix.

Figure 6-12
An Example of Signetic Absolute Object Format



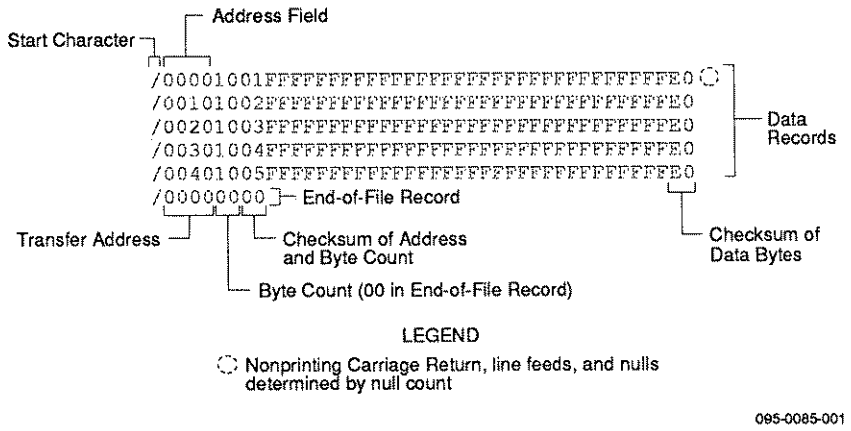
The start character is a colon. This is followed by the address, the byte count, and a 2-digit address check. The address check is calculated by exclusive ORing every byte with the previous one, then rotating left one bit. Data is represented by pairs of hexadecimal characters. The byte count must equal the number of data bytes in the record. The suffix is a 2-character data check, calculated using the same operations described for the address check.

The end-of-file record consists of the colon start character, the address and the byte count (equal to "00").

Tektronix Hexadecimal Format, Code 86

The figure illustrates a valid Tektronix data file. The data in each record is sandwiched between the start character (a slash) and a 2-character checksum. Following the start character, the next 4 characters of the prefix express the address of the first data byte. The address is followed by a byte count, which represents the number of data bytes in the record, and by a checksum of the address and byte count. Data bytes follow, represented by pairs of hexadecimal characters. Succeeding the data bytes is their checksum, an 8-bit sum, modulo 256, of the 4-bit hexadecimal values of the digits making up the data bytes. All records are followed by a carriage return.

Figure 6-13
An Example of Tektronix Hex Format



Data is output from UniSite starting at the first RAM address and continuing until the number of bytes in the specified block have been transmitted. UniSite divides output data into records prefaced by a start character and an address field for the first byte in the record.

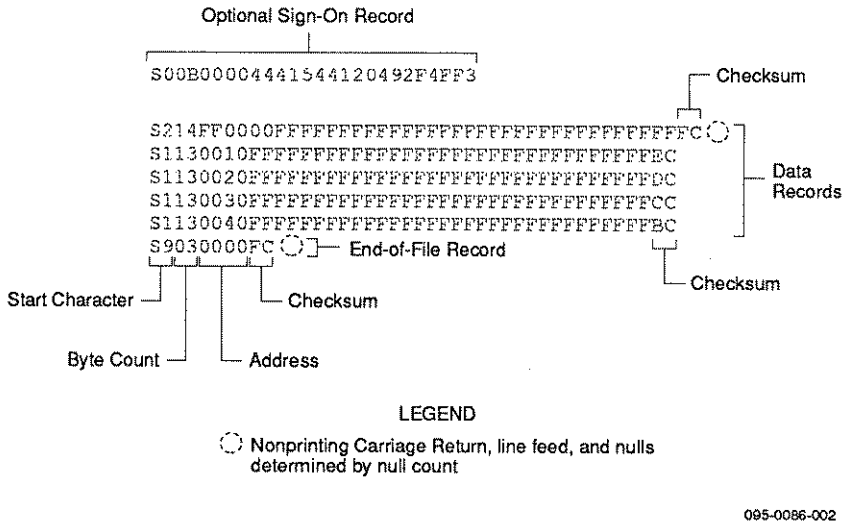
The end-of-file record consists of a start character (slash), followed by the transfer address, the byte count (equal to "00"), and the checksum of the transfer address and byte count.

An optional abort record contains 2 start characters (slashes), followed by an arbitrary string of ASCII characters. Any characters between a carriage return and a "/" are ignored.

Motorola EXORmacs Format, Code 87

Motorola data files may begin with an optional sign-on record, initiated by the start characters "S0." Data records start with an 8- or 10-character prefix and end with a 2-character suffix. The figure shows a series of Motorola EXORmacs data records.

Figure 6-14
An Example of Motorola Exormax Format



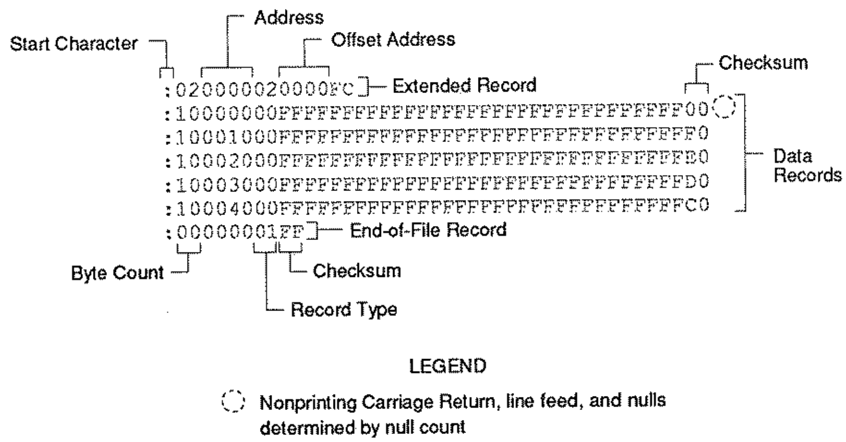
Each data record begins with the start characters "S1" or "S2"; "S1" if the following address field has 4 characters, S2 if it has 6 characters. The third and fourth characters represent the byte count, which expresses the number of data, address and checksum bytes in the record. The address of the first data byte in the record is expressed by the last 4 characters of the prefix (6 characters for addresses above hexadecimal FFFF). Data bytes follow, each represented by 2 hexadecimal characters. The number of data bytes occurring must be 3 or 4 less than the byte count. The suffix is a 2-character checksum, the one's complement (in binary) of the preceding bytes in the record, including the byte count, address and data bytes.

The end-of-file record begins with an "S9" start character. Following the start characters are the byte count, the address and a checksum. The maximum record length is 250 data bytes.

Intel MCS-86 Hexadecimal Object, Code 88

The Intel 16-bit Hexadecimal Object file record format has a 9-character (4-field) prefix that defines the start of record, byte count, load address, and record type and a 2-character checksum suffix. Figure 6-15 shows a sample record of this format.

Figure 6-15
An Example of Intel MCS-86 Hex Object



095-0087-002

The four record types are described below.

00 – Data Record

This begins with the colon start character, which is followed by the byte count (in hex notation), the address of the first data byte, and the record type (equal to "00"). Following these are the data bytes. The checksum follows the data bytes and is the two's complement (in binary) of the preceding bytes in the record, including the byte count, address, record type and data bytes.

01 – End Record

This end-of-file record also begins with the colon start character. This is followed by the byte count (equal to "00"), the address (equal to "0000"), the record type (equal to "01") and the checksum, "FF".

02 – Extended Segment Address Record

This is added to the offset to determine the absolute destination address. The address field for this record must contain ASCII zeros (Hex 30's). This record type defines bits 4 to 19 of the segment base address; it can appear randomly anywhere within the object file and affects the absolute memory address of subsequent data records in the file. The following example illustrates how the extended segment address is used to determine a byte address.

Problem:

Find the address for the first data byte for the following file.

```
: 02 0000 02 1230 BA
: 10 0045 00 55AA FF .....BC
```

Solution:

Step 1. Find the record address for the byte. The first data byte is 55. Its record address is 0045 from above.

Step 2. Find the offset address. The offset address is 1230 from above.

Step 3. Shift the offset address one place left, then add it to the record address, like this:

```
  1230      Offset address (upper 16 bits)
+ 0045      Record address (lower 16 bits)
  12345     20-bit address
```

The address for the first data byte is 12345.

Note: Always specify the address offset when using this format, even when the offset is zero.

During output translation, the firmware will force the record size to 16 (decimal) if the record size is specified greater than 16. There is no such limitation for record sizes specified less than 16.

03 – Start Record

This record type is not sent during output by Data I/O translator firmware.

Hewlett-Packard 64000 Absolute Format, Code 89

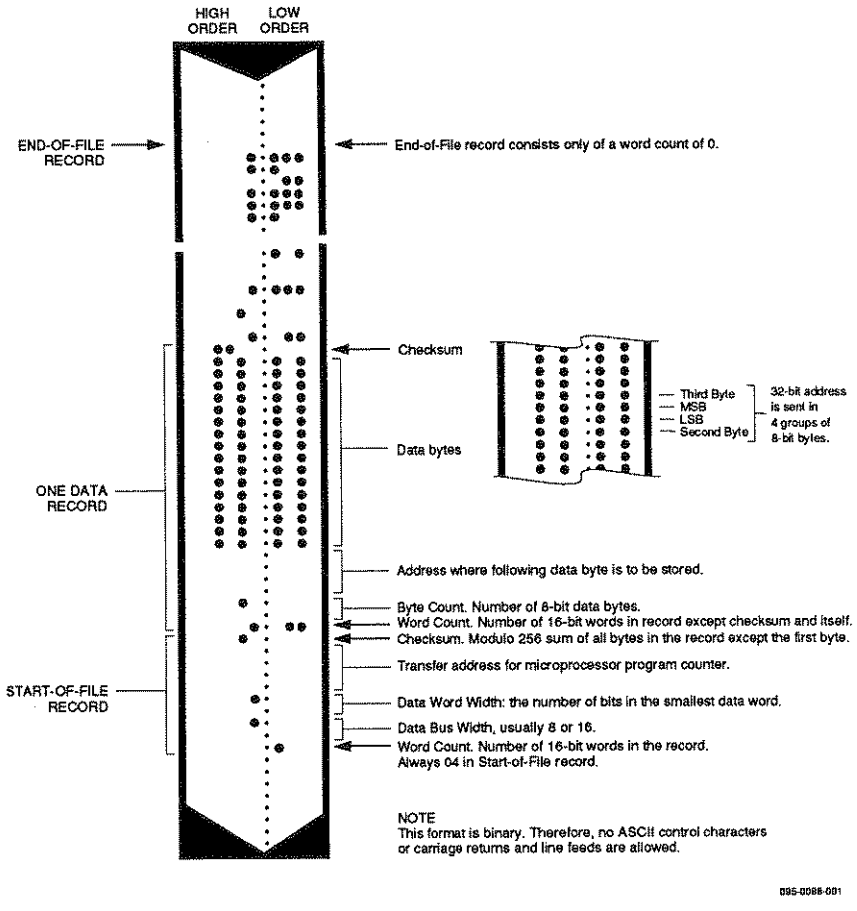
Hewlett-Packard Absolute is a binary format with control and data-checking characters. See the figure.

Data files begin with a start-of-file record including the data bus width, data width base, transfer address, and a checksum of the bytes in the record.

Data records follow the start-of-file record. Each begins with 2 byte counts: the first expresses the number of 16-bit words in the record not including the checksum and itself; the second expresses the number of 8-bit data bytes in the record. Next comes a 32-bit address, which specifies the storage location of the following data byte. Data bytes follow; after the last data byte is a checksum of every byte in the record except the first byte, which is the word count.

The end-of-file record consists only of a 1byte of word count, which is always zero. Leader and trailer nulls, normally 50 each, are suppressed in this translation format.

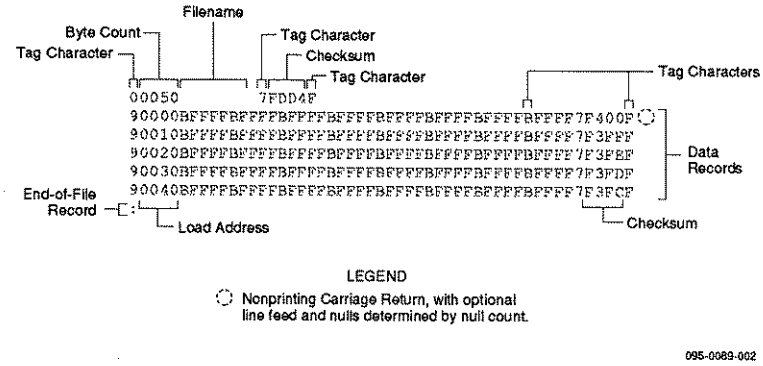
Figure 6-16
An Example of HP 64000 Absolute Format



Texas Instruments SDSMAC Format, Code 90

Data files in the SDSMAC format consist of a start-of-file record, data records, and an end-of-file record. See the figure.

Figure 6-17
An Example of the TI SDSMAC Format



Each record is composed of a series of small fields, each initiated by a tag character. UniSite recognizes and acknowledges the following tag characters:

0 or K - followed by a file header.

7 - followed by a checksum which UniSite acknowledges.

8 - followed by a checksum which UniSite ignores.

9 - followed by a load address.

B - followed by 4 data characters.

F - denotes the end of a data record.

* - followed by 2 data characters.

The start-of-file record begins with a tag character and a 12-character file header. The first four characters are the byte count of the data bytes; the remaining file header characters are the name of the file and may be any ASCII characters (in hex notation). Next come interspersed address fields and data fields (each with tag characters). If any data fields appear before the first address field in the file, the first of those data fields is assigned to address 0000. Address fields may be expressed for any data byte, but none are required.

The record ends with a checksum field initiated by the tag character 7 or 8, a 4-character checksum, and the tag character F. The checksum is the two's complement of the sum of the 8-bit ASCII values of the characters, beginning with the first tag character and ending with the checksum tag character (7 or 8).

Data records follow the same format as the start-of-file record but do not contain a file header. The end-of-file record consists of a colon (:) only. The output translator sends a CTRL-S after the colon.

JEDEC Format, Codes 91 and 92

Introduction

The JEDEC (Joint Electron Device Engineering Council) format is used to transfer fuse and test vector data between UniSite and a host computer. Code 91 is "full" format, and includes all the data fields (such as note and test fields) described on the following pages. Code 92 is the "Kernel", or shorter format. The JEDEC Kernel format includes only the minimum information needed for the programming: it does not, for example, include information fields or test vector fields. Prior to transferring a JEDEC file, the appropriate Logic device must be selected.

JEDEC's legal character set consists of all the printable ASCII characters, and four control characters. The four allowable control characters are STX, ETX CR (RETURN) and LF (line feed). Other control characters, such as ESC or BREAK, should not be used.

Note: This is Data I/O Corporation's implementation of JEDEC Standard 3A. For a copy of the strict standard, write:

Electronic Industries Association
Engineering Department
2001 Eye Street NW
Washington, D.C. 20006

BNF Rules and Standard Definitions

The Backus-Naur Form (BNF) is used in the description here to define the syntax of the JEDEC format. BNF is a shorthand notation that follows these rules:

":: =" denotes "is defined as."

Characters enclosed by single quotes are literals (required).

Angle brackets enclose identifiers.

Square brackets enclose optional items.

Braces { } enclose a repeated item. The item may appear zero or more times.

Vertical bars indicate a choice between items.

Repeat counts are given by a :n suffix. For example, a six digit number would be defined as

" <number> :: = <digit>:6 ."

For example, in words, the definition of a person's name reads:

The full name consists of an optional title followed by a first name, a middle name, and a last name. The person may not have a middle name or may have several middle names. The titles consist of: Mr., Mrs., Ms., Miss, and Dr.

The BNF definition for a person's name is:

<full name> :: = [<title>] <f. name> {<m.name>} <l. name>

<title> :: = 'Mr.' | 'Mrs.' | 'Ms.' | 'Miss' | 'Dr.'

The following standard definitions are used throughout the rest of this document:

<digit> :: = '0' | '1' | '2' | '3' | '4' | '5' | '6' | '7' | '8' | '9'

<hex-digit> :: = <digit> | 'A' | 'B' | 'C' | 'D' | 'E' | 'F'

<binary-digit> :: = '0' | '1'

<number> :: = <digit> {<digit>}

<del> :: = <space> | <carriage return>

<delimiter> :: = <del> {<del>}

<printable character> :: = <ASCII 20 hex ... 7E hex>

<control character> :: = <ASCII 00 hex ... 1F hex> | <ASCII 7F hex>

<STX> :: = <ASCII 02 hex>

<ETX> :: = <ASCII 03 hex>

<carriage return> :: = <ASCII 0D hex>

<line feed> :: = <ASCII 0A hex>

<space> :: = <ASCII 20 hex> | ' '

<valid character> :: = <printable character> | <carriage return> | <line feed>

<field character> :: = <ASCII 20 hex ... 29 hex> | <ASCII 2B hex ... 7E hex> | <carriage return> |

<line feed>

The Design Specification Field

<design spec> ::= {<field character>}'*'

The first field sent in a JEDEC transmission is the design specification. Both the "full" and "kernel" JEDEC formats accept the design specification field. This field is mandatory and it does not have an identifier (such as an "*") signalling its beginning. The design specification field consists of general device information. It could, for example, consist of the following information: your name, your company's name, the date, the device name and manufacturer, design revision level, etc. This field is terminated by a "*" character. Examine the sample transmission shown on the next page of this description -- the first three lines of the file comprise the design specification field. The 2900 ignores the contents of this field for downloads and places "Data I/O" in this field for upload operations.

Note: You do not need to send any information in this field if you do not wish to; a blank field, consisting of the terminating asterisk, is a valid design specification field.

The Transmission Checksum Field

<xmit checksum> ::= <hex digit>:4

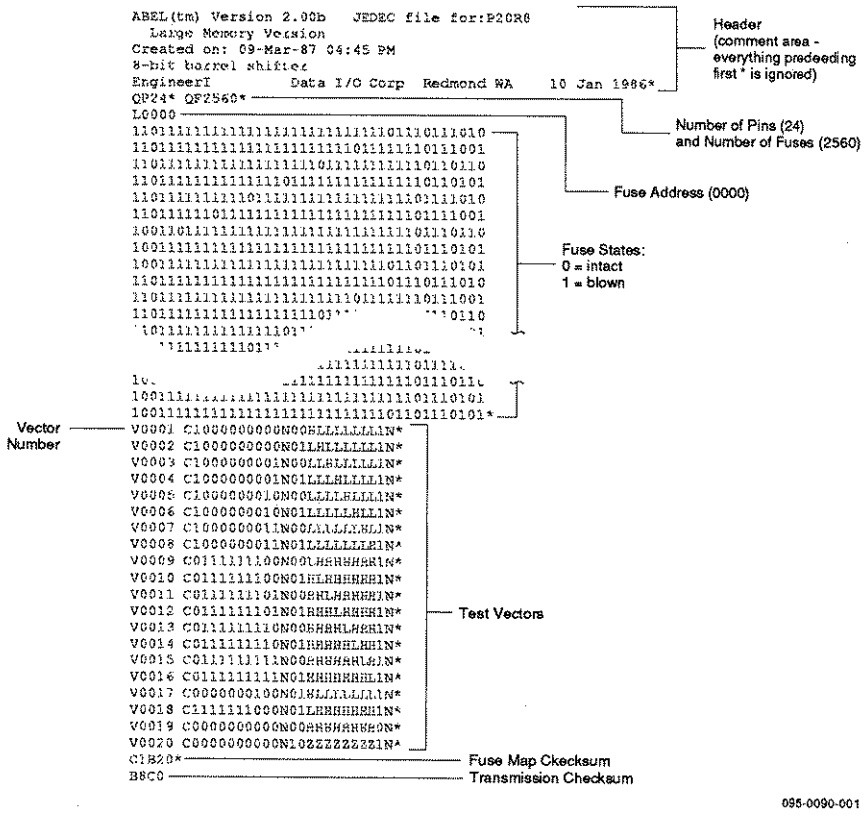
The transmission checksum is the last value sent in a JEDEC transmission. The "full" JEDEC formats requires the transmission checksum. The checksum is a 16-bit value, sent as a 4-digit hex number, and is the sum of all the ASCII characters transmitted between (and including) the STX and ETX. The parity bit is excluded in the calculation of the transmission checksum.

Some computer systems do not allow you to control what characters are sent, especially at the end of a line. You should set up the equipment so that it will accept a dummy value of "0000" as a valid checksum. This zero checksum is a way of disabling the transmission checksum, while still keeping within the JEDEC format rules.

JEDEC Full Format, Code 91

The "full" JEDEC format consists of a start-of-text character (STX), various fields, an end-of-text character (ETX) and a transmission checksum. A sample JEDEC transmission sent in the "full" format is shown below. Each of the valid fields is described on the following pages.

Figure 6-18
An Example of JEDEC Full Format



JEDEC Field Syntax

<field> ::= [<delimiter>]<field identifier>{<field character>}'*'

<field identifier>::= 'A' | 'C' | 'D' | 'F' | 'G' | 'K' | 'L' | 'N' | 'P' | 'Q' | 'R' | 'S' | 'T' | 'V' | 'X'

<reserved identifier>::= 'B' | 'E' | 'H' | 'I' | 'J' | 'M' | 'O' | 'U' | 'W' | 'Y' | 'Z'

Following the design specification field in a JEDEC transmission can be any number of information fields. Each of the JEDEC fields begins with a character that identifies what type of field it is. Fields are terminated by using a "*" character. Multiple character identifiers can be used to create sub-fields (i.e., "A1", "A$", or "AB3"). Although not required, you may use carriage returns (CR) and line feeds (LF) to improve readability of the data.

Field Identifiers

Field identifiers which are currently used in JEDEC transmissions are shown above on the "field identifiers" line. The "reserved identifier" line indicates characters not currently used (reserved for future use as field identifiers). JEDEC field identifiers are defined as follows:

A - Access time
B - *
C - Checksum field
D - Device type
E - *
F - Default fuse state field
G - Security fuse field
H - *
I - *
J - *
K - Fuse list field (hex format)
L - Fuse list field
M - *
N - Note field
O - *
P - Pin sequence
Q - Value field
R - Resulting vector field
S - Starting vector
T - Test cycles
U - *
V - Test vector field
W - *
X - default test condition
Y - *
Z - *

* *Reserved for future use*

Device Field (D)

Device selection by this field is not supported by the 2900. It has been replaced by the QF and QP fields and the manual selection of devices.

Fuse Information Fields (L, K, F, C)

<fuse information> :: = [<default state>] <fuse list> {<fuse list>} [<fuse checksum>]

<fuse list> :: = 'L' <number> <delimiter> {<binary-digit> [<delimiter>]} ' * '

<fuse list> :: = 'K' <number> <delimiter> {<hex-digit> [<delimiter>]} '*'

<default state> :: = 'F' <binary-digit> ' * '

<fuse checksum> :: = 'C' <hex-digit>:4 ' * '

Each fuse of a device is assigned a decimal number and has two possible states: zero, specifying a low-resistance link, or one, specifying a high resistance link. The state of each fuse in the device is given by three fields: the fuse list (L field or K field), the default state (F field), and the fuse checksum (C field).

Fuse states are explicitly defined by either the L field or the K field. The character L begins the L field and is followed by the decimal number of the first fuse for which this field defines a state. The first fuse number is followed by a list of binary values indicating the fuse states.

The information in the K field is the same as that of the L field except that the information is represented by hex characters instead of binary values. This allows more compact representation of the fusemap data. The character K begins the K field and is followed by the decimal number of the first fuse. The fuse data follows the fuse number and is represented by hex characters. Each bit of each hex character represents the state of one fuse, so each hex character represents four fuses. The most significant bit of the first hex character following the fuse number corresponds to the state of that fuse number. The next most significant

bit corresponds to the state of the next fuse number, etc. The least significant bit of the first hex character corresponds to the state of the fuse at the location specified by the fuse number plus three.

The K field supports download operations only. The K field is not part of the JEDEC standard, but is supported by Data I/O for fast data transfer. The L and K fields can be any length desired, and any number of L or K fields can be specified. If the state of a fuse is specified more than once, the last state specified replaces all previous ones for that fuse. The F field defines the states of fuses that are not explicitly defined in the L or K fields. If no F field is specified, all fuse states must be defined by L or K fields.

The C field, the fuse information checksum field, is used to detect transmitting and receiving errors. The field contains a 16-bit sum (i.e. modulus 65535) computed by adding 8-bit words containing the fuse states for the entire device. The 8-bit words are formed as shown in the following figure. Unused bits in the final 8-bit word are set to zero before the checksum is calculated.

Word 00	msb							lsb
Fuse No.	7	6	5	4	3	2	1	0
Word 01	msb							lsb
Fuse No.	7	6	5	4	3	2	1	0
Word 62	msb							lsb
Fuse No.	-	-	-	-	499	498	497	496

Following is an example of full specification of the L, C, and F fields:

F0*L0 01010101* L0008 01010111* L1000 0101*C019E*

Following is an alternate way of defining the same fuse states using the K field:

F0*K0 55* K0008 57* K1000 5* C019E*

Another example, where F and C are not specified:

L0200 01101010101010101011

01011101011010001001001010*

The Security Fuse Field (G)

<security fuse>::='G'<binary-digit>'*'

The JEDEC G field is used to enable the security fuse of some logic devices. To enable the fuse, send a "one" in the G field:

G1*

The Note Field (N)

<note>::='N'<field characters>'*'

The note field is used in JEDEC transmission to insert notes or comments. UniSite will "ignore" this field: it will not be interpreted as data. An example of a note field would be:

N Test Preload*

The Value Fields (QF, QP, and QV)

JEDEC value fields define values or limits for the data file: number of fuses, for example. The QF subfield defines the number of fuses in the device. All of the value fields must occur before any device programming or testing fields appear in the data file. Files with ONLY testing fields do not require the QF field and fields with ONLY programming data do not require the QP and QV fields.

The QF subfield tells UniSite how much memory reserve for fuse data, the number of fuses to set to the default condition and the number of fuses to include in the fuse checksum. The QP subfield defines the number of pins or test conditions in the test vector, and the QV subfield defines the maximum number of test vectors.

The P Field

The "P" field remaps the device pinout and is used with the "V" (test vector) field. An asterisk terminates the field. The syntax of the field is as follows:

<pin list>::='P'<pin number>:N'*'

<pin number>::=<delimiter><number>

The following example shows a "P" field, "V" field and the resulting application:

P 1 2 3 4 5 6 14 15 16 17 7 8 9 10 11 12 13 18 19 20 *

V0001 111000HLHHNNNNNNNNNNN*

V0002 100000HHHLNNNNNNNNNN*

The result of applying the above "P" and "V" fields:vector 1 will apply *111000* to pins 1 through 6, and *HLHH* to pins 14 through 17. Pins 7 through 13 and 18 through 20 will not be tested.

Test Field (V field)

<function test> :: = [<pin list>] <test vector> {<test vector>}

<pin number> :: = <delimiter> <number>

N :: = number of pins on device

<test vector> :: = 'V' <number> <delimiter> < test condition> :N ' * '

<test condition> :: = <digit> 'B' | 'C' | 'D' | 'F' | 'H' | 'K' | 'L' | 'N' | 'P' | 'U' | 'X' | 'Z'

<reserved condition> :: = 'A' | 'E' | 'G' | 'I' | 'J' | 'M' | 'O' | 'Q' | 'R' | 'S' | 'T' | 'V' | 'W' | 'Y' | 'Z'

Functional test information is specified by test vectors containing test conditions for each device pin. Each test vector contains n test conditions where n is the number of pins on the device. The following table lists the conditions that can be specified for device pins.

When using structured test vectors to check your logic design, do NOT use "101" or "010" transitions as tests for clock pins: use "C", "K", "U", or "D" instead.

Test Conditions

0 - Drive input low
1 - Drive input high
2-9 - Drive input to supervoltage #2-9
B - Buried register preload (not supported)
C - Drive input low, high, low
D - Drive input low, fast slew
F - Float input or output
H - Test output high
K - Drive input high, low, high
L - Verifies that the specified output pin is low
N - Power pins and outputs not tested
P - Preload registers
U - Drive input high, fast slew
X - Output not tested, input default level
Z - Test input or output for high impedance

Note: C, K, U, D are clocking functions that allow for setup time.

The C, K, U, and D driving signals are presented after the other inputs are stable. The L, H, and Z tests are performed after all inputs have stabilized, including C, K, U, and D.

Test vectors are numbered by following the V character with a number. The vectors are applied in numerical order to the device being tested. If the same numbered vector is specified more than one time, the data in the last vector replaces any data contained in previous vectors with that number.

The following example uses the V field to specify functional test information for a device:

```
V0001 C01010101NHLLLHHLHLN *
V0002 C01011111NHLLHLLLHLN *
V0003 C10010111NZZZZZZZZZN *
V0004 C01010100NFLHHLFFLLN *
```

JEDEC Kernel Mode, Code 92

<kernel>::=<STX><design spec><min. fuse information><ETX><xmit checksum>

<design spec>::={<field character>}*'

<min. fuse information>::=<fuse list>{<fuse list>}

You may use the JEDEC "kernel" format if you wish only to send the minimum data necessary to program the logic device--if you do not, for example, want to send any test vectors. If you specify format code 92, UniSite will ignore everything except the design specification field and the fuse information field. The following fields will be ignored if format 92 is specified: C, F, G, Q, V, and X. Also, the security fuse will be set to zero and the transmission checksum will be ignored.

An example of a "kernel" JEDEC transmission is shown below:

Figure 6-19
An Example of JEDEC Kernel Mode Format

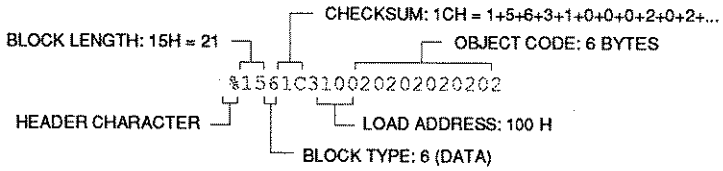
```
<STX>
Acme Logic Design  Jane Engineer   Feb. 29 1983
Widget Decode  756-AB-3456 Rev C  Device Mullard 12AX7*
L0000 1111111011 1111111111  1111000000 0000000000
      0000000000 0000000000  0000000000 0000000000
      0000000000 0000000101  1111111111 1111111111
      0000000000 0000000000  0000111101 1111111111
      1111111111 1111110111  1111111111 1111111111*
L0200 1110101111 1111110000  0000000000 0000000000
      1111111111 1111011011  1111111111 1111111110
      0111111111 1111111111  1111111110 1111111111
      1111111111 1111101111  1111111111 1111101111
      0000000000 0000000000  0000*
<EXT>0000
```

095-0091-001

Extended Tektronix Hexadecimal Format, Code 94

The Extended Tektronix Hexadecimal format has three types of records: data, symbol and termination records. The data record contains the object code. Information about a program section is contained in the symbol record (UniSite ignores symbol records) and the termination record signifies the end of a module. The data record (see sample below) contains a header field, a load address and the object code. The header field contains the information listed below.

Figure 6-20
An Example of Tektronix Extended Format



095-0092-001

Item	No. of ASCII Characters	Description
%	1	Signifies that the record is the Extended Tek Hex format.
Block length	2	Number of characters in the record, minus the %.
Block type	1	6 = data record 3 = symbol record (ignored by UniSite) 8 = termination record
Checksum	2	A 2-digit hex sum, modulo 256, of all the values in the record except the % and the checksum.

Character Values for Checksum Computation

Characters	Values (decimal)
0 . . 9	0 . . 9
A . . Z	10 . . 35
$	36
%	37
. *(period)*	38
_ *(underline)*	39
a . . z	40 . . 65

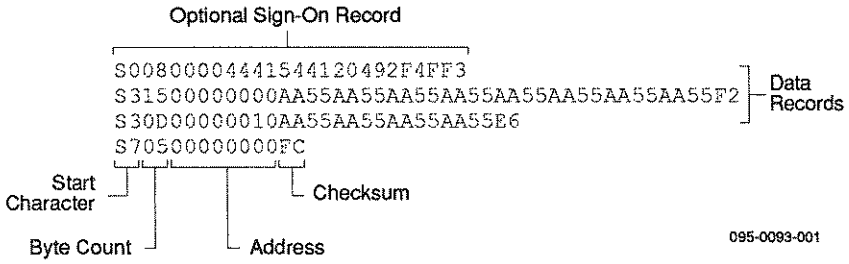
The number of fields in the file will vary, depending on whether a data or a termination block is sent. Both data and termination blocks have a 6-character header and a 2-to-17 character address.

The load address determines where the object code will be located. This is a variable length number that may contain up to 17 characters. The first number determines the address length, with a zero signifying a length of 16. The remaining characters of the data record contain the object code, 2 characters per byte.

When you are copying data to the port or to RAM, make sure to set the high-order address if the low-order is not at the default value.

Motorola 32-Bit Format, Code 95

The Motorola 32-bit format closely resembles the Motorola EXORmacs format, the main difference being the addition of the "S3" and "S7" start characters. The "S3" character is used to begin a record containing a 4-byte address. The "S7" character is a termination record for a block of "S3" records. The address field for an "S7" record may optionally contain the 4-byte instruction address that identifies where control is to be passed and is ignored by UniSite. A sample transmission is shown below.



Motorola data files may begin with an optional sign-on record, initiated by the start characters "S0." Data records start with an 8- or 10-character prefix and end with a 2-character suffix.

Each data record begins with the start characters "S1", "S2" or "S3". "S1" if the following address field has 4 characters, S2 if it has 6 characters, S3 if it has 8 characters. The third and fourth characters represent the byte count, which expresses the number of data, address and checksum bytes in the record. The address of the first data byte in the record is expressed by the last 4 characters of the prefix (6 characters for addresses above hexadecimal FFFF and 8 characters for addresses above hexadecimal FFFFFF). Data bytes follow, each represented by 2 hexadecimal characters. The number of data bytes occurring must be 3, 4 or 5 less than the byte count. The suffix is a 2-character checksum, the one's complement (in binary) of the preceding bytes in the record, including the byte count, address and data bytes.

The end-of-file record begins with an "S9" start character. Following the start characters are the byte count, the address and a checksum. The maximum record length is 250 data bytes.

Hewlett-Packard UNIX Format, Code 96

This format divides the data file into data records; each with a maximum size of 250 bytes not including header information. An I.D. header is added to the beginning of the first record. Each subsequent record has its own header section. The section at the beginning of the file contains the following elements: the header "8004", filename, byte count for the processor information record, and the processor information record.

The header "8004" identifies the type of file being transferred. The first byte of this header (80) indicates that this file is binary and the 04 indicates the type of file (absolute).

The I.D. header is followed by a sixteen byte file name (not used by UniSite).

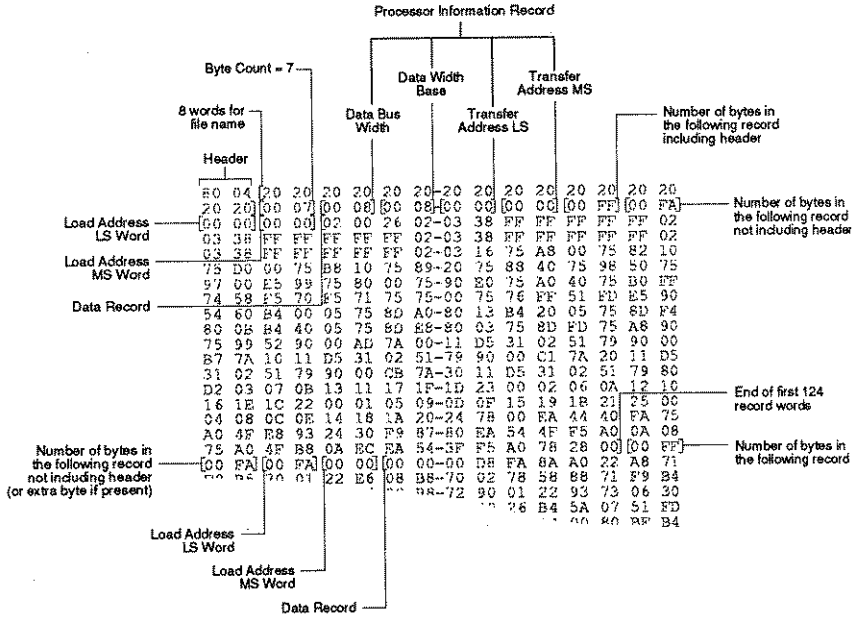
The byte count which appears next indicates the size (minus one) of the processor information record that follows. The processor information record is divided into the following data words: Data Bus Width, Data Width Base, Transfer Address LS (least significant), and Transfer Address MS (most significant). The two transfer address words are not used by UniSite. The data width base will correspond to the data word width on UniSite. During upload, the data width base word will be set to the data word width and the data bus width word will be set to the device width. During download, the data word width parameter on UniSite will be set to the data width base in the downloaded data unless the data width base is less than the device width (in which case an I/O translation format error will be reported and the data word width will not be changed). The data records follow the processor information record.

The data records consist of a header (eight bytes) and the data bytes. The first two bytes of the header indicate the size of the data record including the header (minus one). If the number of data bytes in the data record (not including the header) is odd, one extra byte will be added to the data record to ensure that an even number of data bytes exist in the data record. The maximum value for this field is 00FF hex. The next two bytes indicate the number of actual data bytes in the record, not including the header bytes and the extra byte (if present). The maximum value for this field is 00FA hex. The four bytes that follow represent the destination address for the data in this record. The rest of the bytes in the record are the data bytes.

This format has no end of file identifier.

The record length during upload is not affected by the upload record size parameter in the Configure/Edit/Communication screen. It is automatically set to transfer records using the maximum size (250 bytes) except for the last record. The size of the last record will be set according to the remaining number of data bytes.

Figure 6-22
Hewlett-Packard 64000
Unix Format



This data translation format was generated by a "dump utility" for illustrative purposes. Actual data files are in binary code and are typically generated by the appropriate development software.

095-0474-001

Intel OMF386 Format, Code 97

This data translation format is considered, by Intel, to be proprietary information. Contact your local Intel representative or call (408) 987-8080 for information about the structure of this format.

Intel OMF286 Format, Code 98

The Intel OMF286 format is a dynamically allocatable file format.

This format has three basic parts; the file header, data file module, and a one byte checksum. The file header is hexadecimal number (A2) that identifies this file as an Intel OMF 286 format file. (See Figure 7-23)

The first 75 bytes of the data file module is the data file header. The header information is generated and used by the development system and is not used by the UniSite, although some characters must fill those bytes. The rest of the data file module consists of one partition.

The partition begins with a 20 byte table of contents. The table of contents specifies the locations of ABSTXT (absolute text), DEBTXT (de-bug text), the last location of this partition, and the location of the next partition. The OMF286 format consists of only one partition so this field will be zeros. The rest of the partition consists of sections. The actual data is located in the sections. The first 3 bytes in each section specifies the real address of the text; the next 2 bytes state the length of the text and the remainder of the section is the text (or data). Following the final section of the final partition is a one byte checksum representing the complement of the sum of all the bytes in the file including the header. The sum of the checksum byte and the calculated checksum for the file should equal zero. UniSite ignores this checksum.

Figure 6-23
A Sample of the Intel OMF286 Format

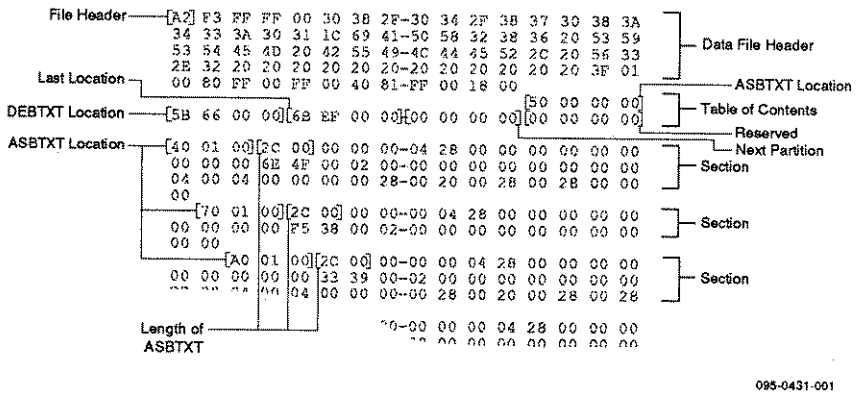
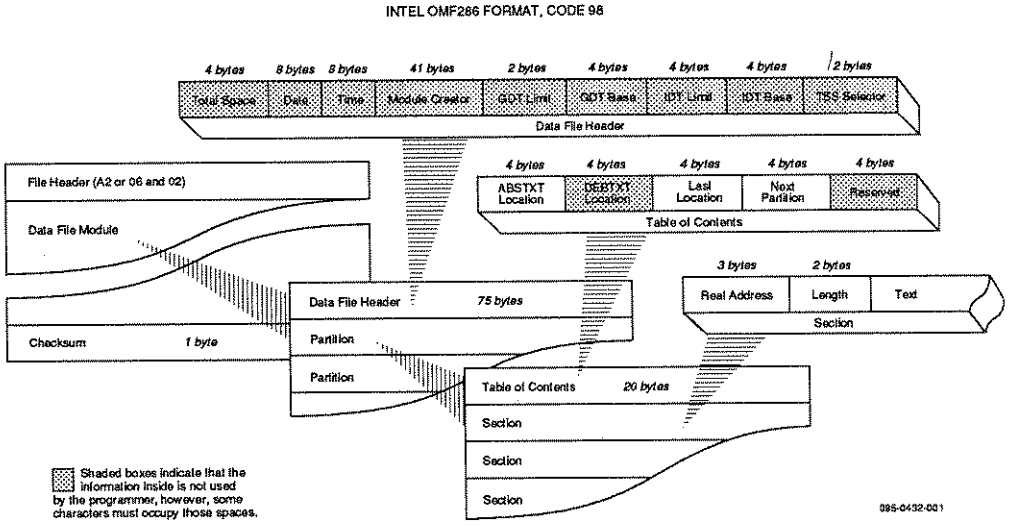


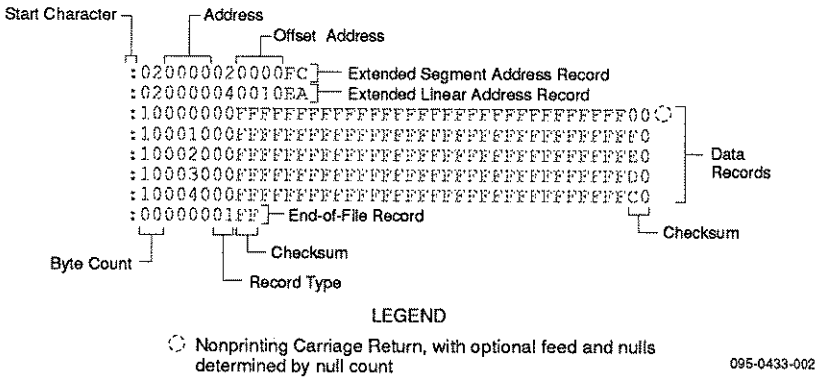
Figure 6-24
A Close Up of the Intel OMF286 Format



Intel Hex-32, Code 99

The Intel 32-bit Hexadecimal Object file record format has a 9-character (4-field) prefix that defines the start of record, byte count, load address, and record type and a 2-character checksum suffix. The figure illustrates the sample records of this format.

Figure 6-25
An Example of the Intel Hex-32 Format



The six record types are described below.

00 – Data Record

This record begins with the colon start character, which is followed by the byte count (in hex notation), the address of the first data byte, and the record type (equal to "00"). Following these are the data bytes. The checksum follows the data bytes and is the two's complement (in binary) of the preceding bytes in the record, including the byte count, address, record type and data bytes.

01 – End Record

This end-of-file record also begins with the colon start character and is followed by the byte count (equal to "00"), the address (equal to "0000"), the record type (equal to "01") and the checksum, "FF".

02 – Extended Segment Address Record

This is added to the offset to determine the absolute destination address. The address field for this record must contain ASCII zeros (Hex 30's). This record type defines bits 4 to 19 of the segment base address; it can appear randomly anywhere within the object file and affects the absolute memory address of subsequent data records in the file. The following example illustrates how the extended segment address is used to determine a byte address.

Problem

Find the address for the first data byte for the following file.

```
:02 0000 04 0010 EA
:02 0000 02 1230 BA
:10 0045 00 55AA FF ..... BC
```

Solution:

Step 1. Find the extended linear address offset for the data record (0010 in the example).

Step 2. Find the extended segment address offset for the data record (1230 in the example).

Step 3. Find the address offset for the data from the data record (0045 in the example).

Step 4. Calculate the absolute address for the first byte of the data record as follows:

```
   00100000    Linear address offset, shifted left 16 bits
+      12300    Segment address offset, shifted left 4 bits
+       0045    Address offset from data record
   00112345    32-bit address for first data byte
```

The address for the first data byte is 112345.

Note: Always specify the address offset when using this format, even when the offset is zero.

During output translation, the firmware will force the record size to 16 (decimal) if the record size is specified greater than 16. There is no such limitation for record sizes specified less than 16.

03 – Start Segment Address Record

This record, which specifies bits 4-19 of the execution start address for the object file, is not used by UniSite.

04 – Extended Linear Address Record

This record specifies bits 16-31 of the destination address for the data records that follow. It is added to the offset to determine the absolute destination address. and can appear randomly anywhere within the object file. The address field for this record must contain ASCII zeros (Hex 30's).

05 – Start Linear Address Record

This record, which specifies bits 16-31 of the execution start address for the object file, is not used by UniSite.

Highest I/O Addresses

The following table shows the highest I/O addresses accepted for each Data Translation Format.

Format #	Highest Address (Hex)
01-03	NA
04	1FFFF (FFFF words)
05-11	NA
12	270F (9999 decimal)
13	270F (9999 decimal)
14	NA
30-32	777777 (octal)
35-37	777777 (octal)
50-52	FFFF
55-58	FFFF
70	FFFF
80	FFFF
81	FFFF
82	FFFF
83	FFFF
85	FFFF
86	FFFF
87	FFFFFF
88	FFFFF
89	FFFFFFFF
90	FFFF
91, 92	NA
94	FFFFFFFF
95	FFFFFFFF
96	FFFFFFFF
97	FFFFFFFF
98	FFFFFF
99	FFFFFFFF

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UniSite™

Universal Programmer

Device List – Version 4.2

DATA I/O

Device List – Version 4.2

Following is a complete listing of the devices currently programmable with Version 4.2 of the UniSite Universal Programmer. The devices are organized by manufacturer, and are listed in numerical order. References in the Footnote column are explained following the list.

Data I/O Device Support Policy/Liability

1. Data I/O strives to achieve more device support approvals from semiconductor manufacturers than any other programmer manufacturer or software developer.
2. Every effort is made to program an adequate number of samples according to the manufacturer supplied specification, and verify waveforms as per that specification prior to release of support. Manufacturers' approvals are to be sought in parallel with this process.
3. Data I/O's objective is to seek and obtain approvals on all devices.
4. Data I/O has made every attempt to ensure that the device information (as provided by the device manufacturer) contained in our programmers, software and documentation is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages, whether direct, indirect, consequential or incidental, that result from use of documents provided with equipment or from the equipment or software which it accompanies, regardless of whether or not Data I/O has been advised of the possibility of such loss or damage.

Key To Device List Headings

An explanation of each of the column headings is given below.

Device Part Number: The number assigned by the device manufacturer.

Pins: The number of pins on the device package.

Device Type: The type of device, such as EPROM, EEPROM, PAL, etc.

Package Type: The type of package that the device is packaged in.

Footnote: Additional information about a device. Each footnote number corresponds to a numbered description at the end of the device list.

Product Version: The earliest version of UniSite software that will program the device to the manufacturer's latest specifications.

Module: The module required to program the device.

Base: The PinSite Base required to program the device.

MatchBook/PPI Adapter: The MatchBook or PPI adapter required to program the device.

Decoding Base and PPI Adapter names

The information in the Base and PPI Adapter fields is coded as follows:

Bases	*xx*BASE-*yyzz* (for example, 29BASE-0202)
PPI Adapters	PPI-*yyzz* (for example, PPI-0401)

Where *xx* is the programmer type:

29 - 2900
39 - 3900
PS - UniSite (with PinSite module)
AS - AutoSite

yy is the package type

01 - DIP
02 - PLCC, JLCC, CLCC, LCC
03 - SOIC, SOP, SO, PSOP
04 - PGA
05 - QFP, PQFP, CQFP, SQFP, CERQFP, TQFP
06 - Shrink DIP
07 - TSOP
08 - Memory Cards
5*p* - device specific "tuned" adapters where *p* is the package type
99 - PPI Base

zz is the revision level (01, 02, 03, etc.) or the Adapter sequence number

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
AMI Semiconductor								
153	153	20	DIP		2.6	Site 48/40		
173	173	24	DIP	33	2.5	Site 48/40		
18CV8	18CV8	20	DIP		4.2	Site 48/40		
18CV8	18CV8-PLCC	20	PLCC		4.2	ChipSite		
18CV8	18CV8-PLCC	20	PLCC		4.2	PinSite	0201	
20CG10	20CG10	24	DIP	33	2.5	Site 48/40		
20CG10	20CG10-PLCC	28	PLCC		3.5	ChipSite		
20CG10	20CG10-PLCC	28	PLCC		3.5	PinSite	0201	
22CV10	22CV10	24	DIP		2.5	Site 48/40		
22CV10	22CV10-FN	28	PLCC		2.7	ChipSite		
22CV10	22CV10-FN	28	PLCC		3.0	PinSite	0201	
22CV10Z	22CV10Z	24	DIP		2.6	Site 48/40		
22CV10Z	22CV10Z-FN	28	PLCC		2.7	ChipSite		
22CV10Z	22CV10Z-FN	28	PLCC		3.0	PinSite	0201	
253	253	20	DIP		2.5	Site 48/40		
273	273	24	DIP		2.5	Site 48/40		
7024	7024	24	DIP		4.0	Site 48/40		
AT&T Microelectronics								
17128	17128	8	DIP	173,202	4.1	Site 48/40		
17128F	17128F	8	DIP	173,202	4.1	Site 48/40		
1736	1736	8	DIP	173,206	4.1	Site 48/40		
1736F	1736F	8	DIP	173,206	4.1	Site 48/40		
1765	1765	8	DIP	173,99	4.1	Site 48/40		
1765F	1765F	8	DIP	173,99	4.1	Site 48/40		
Actel								
A1010-PG84	1010-PG84	85	PGA	39,216	4.2	PinSite	0402	
A1010-PL44	1010-44GANG	44	PLCC	39	4.2	USM-340-002		
A1010-PL68	1010-PL68	68	PLCC	39,216	4.2	PinSite	0201	
A1010-PL68	1010-PL68	68	PLCC	39	4.2	USM-340-001		
A1010A-PG84	1010A-PG84	85	PGA	39,216	4.2	PinSite	0402	
A1010A-PL44	1010A-44GANG	44	PLCC	39,216	4.2	PinSite	0201	
A1010A-PL44	1010A-44GANG	44	PLCC	39	4.2	USM-340-002		
A1010A-PL68	1010A-PL68	68	PLCC	39,216	4.2	PinSite	0201	
A1010A-PL68	1010A-PL68	68	PLCC	39	3.1	USM-340-001		
A1010A-PQ100	1010A-PQ100	100	QFP	39,216	4.2	PinSite	9901	0522
A1010B-PG84	1010B-PG84	85	PGA	39,216	4.2	PinSite	0402	
A1010B-PL44	1010B-44GANG	44	PLCC	39,216	4.2	PinSite	0201	
A1010B-PL44	1010B-44GANG	44	PLCC	39	4.2	USM-340-002		
A1010B-PL68	1010B-68GANG	68	PLCC	39,216	4.2	PinSite	0201	
A1010B-PL68	1010B-68GANG	68	PLCC	39	4.2	USM-340-001		
A1010B-PQ100	1010B-PQ100	100	QFP	39,216	4.2	PinSite	9901	0522
A1020-PL68	1020-PL68	68	PLCC	39,216	4.2	PinSite	0201	
A1020-PL68	1020-PL68	68	PLCC	39	4.2	USM-340-001		
A1020A-CQ84	1020A-CQ84	84	QFPCAR	39,216	4.2	PinSite	9901	0525
A1020A-JQ44	1020A-JQ44	44	JLCC	39,216	4.2	PinSite	0201	
A1020A-JQ68	1020A-JQ68	68	JLCC	39,216	4.2	PinSite	0201	
A1020A-JQ84	1020A-JQ84	84	JLCC	39,216	4.2	PinSite	0201	
A1020A-PG84	1020A-PG84	85	PGA	39,216	4.2	PinSite	0402	
A1020A-PL44	1020A-44GANG	44	PLCC	39,216	4.2	PinSite	0201	
A1020A-PL44	1020A-44GANG	44	PLCC	39	4.2	USM-340-002		
A1020A-PL68	1020A-PL68	68	PLCC	39,216	4.2	PinSite	0201	
A1020A-PL68	1020A-PL68	68	PLCC	39	3.1	USM-340-001		
A1020A-PL84	1020A-PL84	84	PLCC	39,216	4.2	PinSite	0201	
A1020A-PL84	1020A-PL84	84	PLCC	39	3.9	USM-340-002		
A1020B-CQ84	1020B-CQ84	84	QFPCAR	39,216	4.2	PinSite	9901	0525

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Actel (continued)								
A1020B-PG84	1020B-PG84	85	PGA	39,216	4.2	PinSite	0402	
A1020B-PL44	1020B-PL44	44	PLCC	39,216	4.2	PinSite	0201	
A1020B-PL44	1020B-PL44	44	PLCC	39	4.2	USM-340-002		
A1020B-PL68	1020B-68GANG	68	PLCC	39,216	4.2	PinSite	0201	
A1020B-PL68	1020B-68GANG	68	PLCC	39	4.2	USM-340-001		
A1020B-PL84	1020B-84GANG	84	PLCC	39,216	4.2	PinSite	0201	
A1020B-PL84	1020B-84GANG	84	PLCC	39	4.2	USM-340-002		
A1020B-PQ100	1020B-PQ100	100	QFP	39,216	4.2	PinSite	9901	0522
A1225-PG100	1225-PG100	100	PGA	39,192,216	4.2	PinSite	9901	0402
A1225-PL84	1225-PL84	84	PLCC	39,192,216	4.2	PinSite	0201	
A1225-PQ100	1225-PQ100	100	QFP	39,192,216	4.2	PinSite	9901	0522
A1225A-PG100	1225A-PG100	100	PGA	39,192,216	4.2	PinSite	9901	0402
A1225A-PL84	1225A-PL84	84	PLCC	39,192,216	4.2	PinSite	0201	
A1225A-PQ100	1225A-PQ100	100	QFP	39,192,216	4.2	PinSite	9901	0522
A1240-PG132	1240-PG132	132	PGA	39,192,216	4.2	PinSite	9901	0402
A1240-PL84	1240-PL84	84	PLCC	39,192,216	4.2	PinSite	0201	
A1240-PQ144	1240-PQ144	144	QFP	39,192,216	4.2	PinSite	9901	0523
A1240A-PG132	1240A-PG132	132	PGA	39,192,216	4.2	PinSite	9901	0402
A1240A-PL84	1240A-PL84	84	PLCC	39,192,216	4.2	PinSite	0201	
A1240A-PQ144	1240A-PQ144	144	QFP	39,192,216	4.2	PinSite	9901	0523
A1280-PG176	1280-PG176	176	PGA	39,192,216	4.2	PinSite	9901	0402
A1280-PQ160	1280-PQ160	160	QFP	39,192,216	4.2	PinSite	9901	0524
A1280A-PG176	1280A-PG176	176	PGA	39,192,216	4.2	PinSite	9901	0402
A1280A-PQ160	1280A-PQ160	160	QFP	39,192,216	4.2	PinSite	9901	0524
Advanced Micro Devices/MMI								
10020EG8	10020EG8	24	DIP	40	3.6	Site 48/40		
10020EG8	10020EG8-FN	28	PLCC	28	3.6	ChipSite		
10020EG8	10020EG8-FN	28	PLCC	28	3.6	PinSite	0201	
10020EV8	10020EV8	24	DIP	40	3.6	Site 48/40		
10020EV8	10020EV8-FN	28	PLCC	28	3.6	ChipSite		
10020EV8	10020EV8-FN	28	PLCC	28	3.6	PinSite	0201	
10H20EG8	10H20EG8	24	DIP	40	3.6	Site 48/40		
10H20EG8	10H20EG8-FN	28	PLCC	28	3.6	ChipSite		
10H20EG8	10H20EG8-FN	28	PLCC	28	3.6	PinSite	0201	
10H20EV8	10H20EV8	24	DIP	40	3.6	Site 48/40		
10H20EV8	10H20EV8-FN	28	PLCC	28	3.6	ChipSite		
10H20EV8	10H20EV8-FN	28	PLCC	28	3.6	PinSite	0201	
10H20G8	10H20G8	24	DIP		3.6	Site 48/40		
10H20P8	10H20P8	24	DIP		3.6	Site 48/40		
10H8/-2	10H8/-2	20	DIP		3.6	Site 48/40		
10H8/-2	10H8-NL	20	PLCC		3.6	ChipSite		
10H8/-2	10H8-NL	20	PLCC		3.6	PinSite	0201	
10H8/-2	10H8-SOIC	20	SO		3.6	ChipSite		
10H8/-2	10H8-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
10L8/-2	10L8/-2	20	DIP		3.6	Site 48/40		
10L8/-2	10L8-NL	20	PLCC		3.6	ChipSite		
10L8/-2	10L8-NL	20	PLCC		3.6	PinSite	0201	
10L8/-2	10L8-SOIC	20	SO		3.6	ChipSite		
10L8/-2	10L8-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
10P4	10P4	18	DIP		2.2	Site 48/40		
10P8	10P8	24	DIP		2.2	Site 48/40		
10R8	10R8	24	DIP	1	2.2	Site 48/40		
11P4	11P4	18	DIP		2.2	Site 48/40		
11P8	11P8	24	DIP		2.2	Site 48/40		
11RA8	11RA8	24	DIP	1	2.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
11RS8	11RS8	24	DIP	1	2.2	Site 48/40		
12H6/-2	12H6/-2	20	DIP		3.6	Site 48/40		
12H6/-2	12H6-NL	20	PLCC		3.6	ChipSite		
12H6/-2	12H6-NL	20	PLCC		3.6	PinSite	0201	
12H6/-2	12H6-SOIC	20	SO		3.6	ChipSite		
12H6/-2	12H6-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
12L10	12L10	24	DIP		3.6	Site 48/40		
12L10	12L10-SOIC	24	SO		3.6	ChipSite		
12L10	12L10-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
12L10-ML	12L10/A-ML	28	LCC	44	3.6	ChipSite		
12L10-ML	12L10/A-ML	28	LCC	44	3.6	PinSite	0202	
12L10-NL	12L10-NL	28	PLCC		3.6	ChipSite		
12L10-NL	12L10-NL	28	PLCC		3.6	PinSite	0201	
12L6/-2	12L6/-2	20	DIP		3.6	Site 48/40		
12L6/-2	12L6-NL	20	PLCC		3.6	ChipSite		
12L6/-2	12L6-NL	20	PLCC		3.6	PinSite	0201	
12L6/-2	12L6-SOIC	20	SO		3.6	ChipSite		
12L6/-2	12L6-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
12P4	12P4	20	DIP		2.2	Site 48/40		
12P8	12P8	24	DIP		2.2	Site 48/40		
14H4/-2	14H4/-2	20	DIP		3.6	Site 48/40		
14H4/-2	14H4-NL	20	PLCC		3.6	ChipSite		
14H4/-2	14H4-NL	20	PLCC		3.6	PinSite	0201	
14H4/-2	14H4-SOIC	20	SO		3.6	ChipSite		
14H4/-2	14H4-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
14L4/-2	14L4/-2	20	DIP		3.6	Site 48/40		
14L4/-2	14L4-NL	20	PLCC		3.6	ChipSite		
14L4/-2	14L4-NL	20	PLCC		3.6	PinSite	0201	
14L4/-2	14L4-SOIC	20	SO		3.6	ChipSite		
14L4/-2	14L4-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
14L8	14L8	24	DIP		3.6	Site 48/40		
14L8	14L8-SOIC	24	SO		3.6	ChipSite		
14L8	14L8-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
14L8-NL	14L8-NL	28	PLCC		3.6	ChipSite		
14L8-NL	14L8-NL	28	PLCC		3.6	PinSite	0201	
16A4	16A4	20	DIP		3.6	Site 48/40		
16A4	16A4-NL	20	PLCC		3.6	ChipSite		
16A4	16A4-NL	20	PLCC		3.6	PinSite	0201	
16A4	16A4-SOIC	20	SO		3.6	ChipSite		
16A4	16A4-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16C1/-2	16C1/-2	20	DIP		3.6	Site 48/40		
16C1/-2	16C1-NL	20	PLCC		3.6	ChipSite		
16C1/-2	16C1-NL	20	PLCC		3.6	PinSite	0201	
16C1/-2	16C1-SOIC	20	SO		3.6	ChipSite		
16C1/-2	16C1-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16H2/-2	16H2/-2	20	DIP		3.6	Site 48/40		
16H2/-2	16H2-NL	20	PLCC		3.6	ChipSite		
16H2/-2	16H2-NL	20	PLCC		3.6	PinSite	0201	
16H2/-2	16H2-SOIC	20	SO		3.6	ChipSite		
16H2/-2	16H2-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16H8	16H8	20	DIP		2.1	Site 48/40		
16HD8	16HD8	20	DIP		2.1	Site 48/40		
16L2/-2	16L2/-2	20	DIP		3.6	Site 48/40		
16L2/-2	16L2-NL	20	PLCC		3.6	ChipSite		
16L2/-2	16L2-NL	20	PLCC		3.6	PinSite	0201	
16L2/-2	16L2-SOIC	20	SO		3.6	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
16L2/-2	16L2-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16L6	16L6-SOIC	20	SO		3.6	ChipSite		
16L6	16L6-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16L6	16L6	24	DIP		3.6	Site 48/40		
16L6-NL	16L6-NL	28	PLCC		3.6	ChipSite		
16L6-NL	16L6-NL	28	PLCC		3.6	PinSite	0201	
16L8	16L8/A-PLCC	20	PLCC		1.6	ChipSite		
16L8	16L8/A-PLCC	20	PLCC		3.0	PinSite	0201	
16L8-4	16L8-4-PLCC	28	PLCC		3.9	PinSite	0201	
16L8-5	16L8-5	20	DIP	28	3.9	Site 48/40		
16L8-5	16L8-5-PLCC	20	PLCC	28	3.9	ChipSite		
16L8-5	16L8-5-PLCC	20	PLCC	28	4.2	PinSite	9901/0201	5202
16L8-7	16L8-7	20	DIP		3.9	Site 48/40		
16L8-7	16L8-7PLCC	20	PLCC		3.9	ChipSite		
16L8-7	16L8-7PLCC	20	PLCC		3.9	PinSite	0201	
16L8/A/A-2/A-4	16L8/A/A2/A4	20	DIP		3.6	Site 48/40		
16L8/A/A-2/A-4	16L8/A/2/4NL	20	PLCC		3.6	ChipSite		
16L8/A/A-2/A-4	16L8/A/2/4NL	20	PLCC		3.6	PinSite	0201	
16L8/A/A-2/A-4	16L8/A/2/4SO	20	SO		3.6	ChipSite		
16L8/A/A-2/A-4	16L8/A/2/4SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16L8/A/B	16L8/A/B	20	DIP		2.1	Site 48/40		
16L8/A/B	16L8/A/B-LCC	20	LCC	44	2.5	ChipSite		
16L8/A/B	16L8/A/B-LCC	20	LCC	44	3.0	PinSite	0202	
16L8A	16L8/A-PLCC	20	PLCC		1.6	ChipSite		
16L8A	16L8/A-PLCC	20	PLCC		3.0	PinSite	0201	
16L8B	16L8B/D	20	DIP		3.6	Site 48/40		
16L8B	16L8B/D-NL	20	PLCC		3.6	ChipSite		
16L8B	16L8B/D-NL	20	PLCC		3.6	PinSite	0201	
16L8B	16L8B-PLCC	20	PLCC		1.6	ChipSite		
16L8B	16L8B-PLCC	20	PLCC		3.0	PinSite	0201	
16L8B	16L8B/D-SO	20	SO		3.6	ChipSite		
16L8B	16L8B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16L8B-2/B-4	16L8B2/B4	20	DIP		3.6	Site 48/40		
16L8B-2/B-4	16L8B2/B4-NL	20	PLCC		3.6	ChipSite		
16L8B-2/B-4	16L8B2/B4-NL	20	PLCC		3.6	PinSite	0201	
16L8B-2/B-4	16L8B2/B4-SO	20	SO		3.6	ChipSite		
16L8B-2/B-4	16L8B2/B4-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16L8D	16L8B/D	20	DIP		3.6	Site 48/40		
16L8D	16L8B/D-NL	20	PLCC		3.6	ChipSite		
16L8D	16L8B/D-NL	20	PLCC		3.6	PinSite	0201	
16L8D	16L8B/D-SO	20	SO		3.6	ChipSite		
16L8D	16L8B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16L8D/2	16L8D/2	20	DIP	28	3.9	Site 48/40		
16L8D/2	16L8D/2-PLCC	20	PLCC	28	3.9	ChipSite		
16L8D/2	16L8D/2-PLCC	20	PLCC	28	3.9	PinSite	0201	
16L8H-10	16L8H-10	20	DIP		3.9	Site 48/40		
16L8H-10	16L8H-10PLCC	20	PLCC		3.9	ChipSite		
16L8H-10	16L8H-10PLCC	20	PLCC		3.9	PinSite	0201	
16L8H-15	16L8H-15	20	DIP		3.6	Site 48/40		
16L8H-15	16L8H-15PLCC	20	PLCC		3.6	ChipSite		
16L8H-15	16L8H-15PLCC	20	PLCC		3.6	PinSite	0201	
16LD8	16LD8	20	DIP		2.1	Site 48/40		
16P8A	16P8A	20	DIP		3.6	Site 48/40		
16P8A	16P8A-SOIC	20	SO		3.6	ChipSite		
16P8A	16P8A-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R4	16R4/A-PLCC	20	PLCC		2.1	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
16R4	16R4/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R4-4	16R4-4-PLCC	28	PLCC	28	3.9	PinSite	0201	
16R4-5	16R4-5	20	DIP	28	3.9	Site 48/40		
16R4-5	16R4-5-PLCC	20	PLCC	28	3.9	ChipSite		
16R4-5	16R4-5-PLCC	20	PLCC	28	3.9	PinSite	0201	
16R4-7	16R4-7	20	DIP		3.9	Site 48/40		
16R4-7	16R4-7-PLCC	20	PLCC		3.9	ChipSite		
16R4-7	16R4-7-PLCC	20	PLCC		3.9	PinSite	0201	
16R4/A/A-2/A-4	16R4/A/A2/A4	20	DIP		3.6	Site 48/40		
16R4/A/A-2/A-4	16R4/A/2/4NL	20	PLCC		3.6	ChipSite		
16R4/A/A-2/A-4	16R4/A/2/4NL	20	PLCC		3.6	PinSite	0201	
16R4/A/A-2/A-4	16R4/A/2/4SO	20	SO		3.6	ChipSite		
16R4/A/A-2/A-4	16R4/A/2/4SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R4/A/B	16R4/A/B	20	DIP		2.1	Site 48/40		
16R4/A/B	16R4/A/B-LCC	20	LCC	44	2.5	ChipSite		
16R4/A/B	16R4/A/B-LCC	20	LCC	44	3.0	PinSite	0202	
16R4A	16R4/A-PLCC	20	PLCC		2.1	ChipSite		
16R4A	16R4/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R4B	16R4B/D	20	DIP		3.6	Site 48/40		
16R4B	16R4B/D-NL	20	PLCC		3.6	ChipSite		
16R4B	16R4B/D-NL	20	PLCC		3.6	PinSite	0201	
16R4B	16R4B-PLCC	20	PLCC		2.1	ChipSite		
16R4B	16R4B-PLCC	20	PLCC		3.0	PinSite	0201	
16R4B	16R4B/D-SO	20	SO		3.6	ChipSite		
16R4B	16R4B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R4B-2/B-4	16R4B2/B4	20	DIP		3.6	Site 48/40		
16R4B-2/B-4	16R4B2/B4-NL	20	PLCC		3.6	ChipSite		
16R4B-2/B-4	16R4B2/B4-NL	20	PLCC		3.6	PinSite	0201	
16R4B-2/B-4	16R4B2/B4-SO	20	SO		3.6	ChipSite		
16R4B-2/B-4	16R4B2/B4-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R4D	16R4B/D	20	DIP		3.6	Site 48/40		
16R4D	16R4B/D-NL	20	PLCC		3.6	ChipSite		
16R4D	16R4B/D-NL	20	PLCC		3.6	PinSite	0201	
16R4D	16R4B/D-SO	20	SO		3.6	ChipSite		
16R4D	16R4B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R4D/2	16R4D/2	20	DIP	28	3.9	Site 48/40		
16R4D/2	16R4D/2-PLCC	20	PLCC	28	3.9	ChipSite		
16R4D/2	16R4D/2-PLCC	20	PLCC	28	3.9	PinSite	0201	
16R4H-10	16R4H-10	20	DIP		3.9	Site 48/40		
16R4H-10	16R4H-10PLCC	20	PLCC		3.9	ChipSite		
16R4H-10	16R4H-10PLCC	20	PLCC		3.9	PinSite	0201	
16R4H-15	16R4H-15	20	DIP		3.6	Site 48/40		
16R4H-15	16R4H-15PLCC	20	PLCC		3.6	ChipSite		
16R4H-15	16R4H-15PLCC	20	PLCC		3.6	PinSite	0201	
16R6	16R6/A-PLCC	20	PLCC		2.1	ChipSite		
16R6	16R6/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R6-4	16R6-4-PLCC	28	PLCC	28	3.9	PinSite	0201	
16R6-5	16R6-5	20	DIP	28	3.9	Site 48/40		
16R6-5	16R6-5-PLCC	20	PLCC	28	3.9	ChipSite		
16R6-5	16R6-5-PLCC	20	PLCC	28	3.9	PinSite	0201	
16R6-7	16R6-7	20	DIP		3.9	Site 48/40		
16R6-7	16R6-7-PLCC	20	PLCC		3.9	ChipSite		
16R6-7	16R6-7-PLCC	20	PLCC		3.9	PinSite	0201	
16R6/A/A-2/A-4	16R6/A/A2/A4	20	DIP		3.6	Site 48/40		
16R6/A/A-2/A-4	16R6/A/2/4NL	20	PLCC		3.6	ChipSite		
16R6/A/A-2/A-4	16R6/A/2/4NL	20	PLCC		3.6	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
16R6/A/A-2/A-4	16R6/A/2/4SO	20	SO		3.6	ChipSite		
16R6/A/A-2/A-4	16R6/A/2/4SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R6/A/B	16R6/A/B	20	DIP		2.1	Site 48/40		
16R6/A/B	16R6/A/B-LCC	20	LCC	44	2.5	ChipSite		
16R6/A/B	16R6/A/B-LCC	20	LCC	44	3.0	PinSite	0202	
16R6A	16R6/A-PLCC	20	PLCC		2.1	ChipSite		
16R6A	16R6/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R6B	16R6B/D	20	DIP		3.6	Site 48/40		
16R6B	16R6B/D-NL	20	PLCC		3.6	ChipSite		
16R6B	16R6B/D-NL	20	PLCC		3.6	PinSite	0201	
16R6B	16R6B-PLCC	20	PLCC		2.1	ChipSite		
16R6B	16R6B-PLCC	20	PLCC		3.0	PinSite	0201	
16R6B	16R6B/D-SO	20	SO		3.6	ChipSite		
16R6B	16R6B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R6B-2/B-4	16R6B2/B4	20	DIP		3.6	Site 48/40		
16R6B-2/B-4	16R6B2/B4-NL	20	PLCC		3.6	ChipSite		
16R6B-2/B-4	16R6B2/B4-NL	20	PLCC		3.6	PinSite	0201	
16R6B-2/B-4	16R6B2/B4-SO	20	SO		3.6	ChipSite		
16R6B-2/B-4	16R6B2/B4-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R6D	16R6B/D	20	DIP		3.6	Site 48/40		
16R6D	16R6B/D-NL	20	PLCC		3.6	ChipSite		
16R6D	16R6B/D-NL	20	PLCC		3.6	PinSite	0201	
16R6D	16R6B/D-SO	20	SO		3.6	ChipSite		
16R6D	16R6B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R6D/2	16R6D/2	20	DIP	28	3.9	Site 48/40		
16R6D/2	16R6D/2-PLCC	20	PLCC	28	3.9	ChipSite		
16R6D/2	16R6D/2-PLCC	20	PLCC	28	3.9	PinSite	0201	
16R6H-10	16R6H-10	20	DIP		3.9	Site 48/40		
16R6H-10	16R6H-10PLCC	20	PLCC		3.9	ChipSite		
16R6H-10	16R6H-10PLCC	20	PLCC		3.9	PinSite	0201	
16R6H-15	16R6H-15	20	DIP		3.6	Site 48/40		
16R6H-15	16R6H-15PLCC	20	PLCC		3.6	ChipSite		
16R6H-15	16R6H-15PLCC	20	PLCC		3.6	PinSite	0201	
16R8	16R8/A-PLCC	20	PLCC		2.1	ChipSite		
16R8	16R8/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R8-4	16R8-4-PLCC	28	PLCC	28	4.2	PinSite	9901/0201	5203
16R8-5	16R8-5	20	DIP	28	3.9	Site 48/40		
16R8-5	16R8-5-PLCC	20	PLCC	28	3.9	ChipSite		
16R8-5	16R8-5-PLCC	20	PLCC	28	3.9	PinSite	0201	
16R8-7	16R8-7	20	DIP		3.9	Site 48/40		
16R8-7	16R8-7-PLCC	20	PLCC		3.9	ChipSite		
16R8-7	16R8-7-PLCC	20	PLCC		3.9	PinSite	0201	
16R8/A/A-2/A-4	16R8/A/A2/A4	20	DIP		3.6	Site 48/40		
16R8/A/A-2/A-4	16R8/A/2/4NL	20	PLCC		3.6	ChipSite		
16R8/A/A-2/A-4	16R8/A/2/4NL	20	PLCC		3.6	PinSite	0201	
16R8/A/A-2/A-4	16R8/A/2/4SO	20	SO		3.6	ChipSite		
16R8/A/A-2/A-4	16R8/A/2/4SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R8/A/B	16R8/A/B	20	DIP		2.1	Site 48/40		
16R8/A/B	16R8/A/B-LCC	20	LCC	44	2.5	ChipSite		
16R8/A/B	16R8/A/B-LCC	20	LCC	44	3.0	PinSite	0202	
16R8A	16R8/A-PLCC	20	PLCC		2.1	ChipSite		
16R8A	16R8/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R8B	16R8B/D	20	DIP		3.6	Site 48/40		
16R8B	16R8B/D-NL	20	PLCC		3.6	ChipSite		
16R8B	16R8B/D-NL	20	PLCC		3.6	PinSite	0201	
16R8B	16R8B-PLCC	20	PLCC		2.1	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
16R8B	16R8B-PLCC	20	PLCC		3.0	PinSite	0201	
16R8B	16R8B/D-SO	20	SO		3.6	ChipSite		
16R8B	16R8B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R8B-2/B-4	16R8B2/B4	20	DIP		3.6	Site 48/40		
16R8B-2/B-4	16R8B2/B4-NL	20	PLCC		3.6	ChipSite		
16R8B-2/B-4	16R8B2/B4-NL	20	PLCC		3.6	PinSite	0201	
16R8B-2/B-4	16R8B2/B4-SO	20	SO		3.6	ChipSite		
16R8B-2/B-4	16R8B2/B4-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R8D	16R8B/D	20	DIP		3.6	Site 48/40		
16R8D	16R8B/D-NL	20	PLCC		3.6	ChipSite		
16R8D	16R8B/D-NL	20	PLCC		3.6	PinSite	0201	
16R8D	16R8B/D-SO	20	SO		3.6	ChipSite		
16R8D	16R8B/D-SO	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16R8D/2	16R8D/2	20	DIP	28	3.9	Site 48/40		
16R8D/2	16R8D/2-PLCC	20	PLCC	28	3.9	ChipSite		
16R8D/2	16R8D/2-PLCC	20	PLCC	28	3.9	PinSite	0201	
16R8H-10	16R8H-10	20	DIP		3.9	Site 48/40		
16R8H-10	16R8H-10PLCC	20	PLCC		3.9	ChipSite		
16R8H-10	16R8H-10PLCC	20	PLCC		3.9	PinSite	0201	
16R8H-15	16R8H-15	20	DIP		3.6	Site 48/40		
16R8H-15	16R8H-15PLCC	20	PLCC		3.6	ChipSite		
16R8H-15	16R8H-15PLCC	20	PLCC		3.6	PinSite	0201	
16RA8	16RA8	20	DIP		3.6	Site 48/40		
16RA8	16RA8-PLCC	20	PLCC		3.6	ChipSite		
16RA8	16RA8-PLCC	20	PLCC		3.6	PinSite	0201	
16RA8	16RA8-SOIC	20	SO		3.6	ChipSite		
16RA8	16RA8-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16RP4A	16RP4A	20	DIP		3.6	Site 48/40		
16RP4A	16RP4A-NL	20	PLCC		3.6	ChipSite		
16RP4A	16RP4A-NL	20	PLCC		3.6	PinSite	0201	
16RP4A	16RP4A-SOIC	20	SO		3.6	ChipSite		
16RP4A	16RP4A-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16RP6A	16RP6A	20	DIP		3.6	Site 48/40		
16RP6A	16RP6A-NL	20	PLCC		3.6	ChipSite		
16RP6A	16RP6A-NL	20	PLCC		3.6	PinSite	0201	
16RP6A	16RP6A-SOIC	20	SO		3.6	ChipSite		
16RP6A	16RP6A-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16RP8A	16RP8A	20	DIP		3.6	Site 48/40		
16RP8A	16RP8A-NL	20	PLCC		3.6	ChipSite		
16RP8A	16RP8A-NL	20	PLCC		3.6	PinSite	0201	
16RP8A	16RP8A-SOIC	20	SO		3.6	ChipSite		
16RP8A	16RP8A-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
16X4	16X4	20	DIP		3.6	Site 48/40		
16X4	16X4-NL	20	PLCC		3.6	ChipSite		
16X4	16X4-NL	20	PLCC		3.6	PinSite	0201	
16X4	16X4-SOIC	20	SO		3.6	ChipSite		
16X4	16X4-SOIC	20	SO		3.6	PinSite	0302/0301	.300 SOIC
1736	1736	8	DIP	46	2.6	Site 48/40		
1736	1736-PLCC	20	PLCC	46	2.8	ChipSite		
1736	1736-PLCC	20	PLCC	46	3.0	PinSite	0201	
1765	1765	8	DIP	46	2.8	Site 48/40		
1765	1765-PLCC	20	PLCC	46	2.8	ChipSite		
1765	1765-PLCC	20	PLCC	46	3.0	PinSite	0201	
18L4	18L4	24	DIP		3.6	Site 48/40		
18L4	18L4-SOIC	24	SO		3.6	ChipSite		
18L4	18L4-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
18L4-NL	18L4-NL	28	PLCC		3.6	ChipSite		
18L4-NL	18L4-NL	28	PLCC		3.6	PinSite	0201	
18P8	18P8	20	DIP		1.5	Site 48/40		
18P8	18P8-PLCC	20	PLCC		1.5	ChipSite		
18P8	18P8-PLCC	20	PLCC		3.0	PinSite	0201	
20C1	20C1	24	DIP		3.6	Site 48/40		
20C1-NL	20C1-NL	28	PLCC		3.6	ChipSite		
20C1-NL	20C1-NL	28	PLCC		3.6	PinSite	0201	
20L10	20L10	24	DIP		2.0	Site 48/40		
20L10	20L10-PLCC	28	PLCC		2.5	ChipSite		
20L10	20L10-PLCC	28	PLCC		3.0	PinSite	0201	
20L10-ML	20L10/A-ML	28	LCC	44	3.6	ChipSite		
20L10-ML	20L10/A-ML	28	LCC	44	3.6	PinSite	0202	
20L10/A	20L10/A	24	DIP		3.6	Site 48/40		
20L10/A	20L10/A-SOIC	24	SO		3.6	ChipSite		
20L10/A	20L10/A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20L10/A-FN	20L10/A-FN	28	PLCC		3.6	ChipSite		
20L10/A-FN	20L10/A-FN	28	PLCC		3.6	PinSite	0201	
20L10/A-NL	20L10/A-NL	28	PLCC		3.6	ChipSite		
20L10/A-NL	20L10/A-NL	28	PLCC		3.6	PinSite	0201	
20L2	20L2	24	DIP		3.6	Site 48/40		
20L2	20L2-SOIC	24	SO		3.6	ChipSite		
20L2	20L2-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20L2-NL	20L2-NL	28	PLCC		3.6	ChipSite		
20L2-NL	20L2-NL	28	PLCC		3.6	PinSite	0201	
20L8	20L8	24	DIP		2.0	Site 48/40		
20L8-10	20L8-10	24	DIP		3.6	Site 48/40		
20L8-10	20L8-10-PLCC	28	PLCC		3.6	ChipSite		
20L8-10	20L8-10-PLCC	28	PLCC		3.6	PinSite	0201	
20L8-10/2	20L8-10/2	24	DIP	28	3.9	Site 48/40		
20L8-10/2	20L8-10/2-PL	28	PLCC	28	3.9	ChipSite		
20L8-10/2	20L8-10/2-PL	28	PLCC	28	3.9	PinSite	0201	
20L8-5	20L8-5	24	DIP	28	3.9	Site 48/40		
20L8-5	20L8-5-PLCC	28	PLCC	28	3.9	ChipSite		
20L8-5	20L8-5-PLCC	28	PLCC	28	4.2	PinSite	9901/0201	5201
20L8-7	20L8-7	24	DIP		3.9	Site 48/40		
20L8-7	20L8-7-PLCC	28	PLCC		3.9	ChipSite		
20L8-7	20L8-7-PLCC	28	PLCC		3.9	PinSite	0201	
20L8A-ML	20L8A-ML	20	LCC		3.6	ChipSite		
20L8A-ML	20L8A-ML	20	LCC		3.6	PinSite	0202	
20L8A/A-2	20L8A-SOIC	24	SO		3.6	ChipSite		
20L8A/A-2	20L8A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20L8A/A-2/B/B-2	20L8A/A2/B	24	DIP		3.6	Site 48/40		
20L8A/A-2/B/FN	20L8A/A2-FN	28	PLCC		3.6	ChipSite		
20L8A/A-2/B/FN	20L8A/A2-FN	28	PLCC		3.6	PinSite	0201	
20L8A/A-2/B/NL	20L8A/A2-NL	28	PLCC		3.6	ChipSite		
20L8A/A-2/B/NL	20L8A/A2-NL	28	PLCC		3.6	PinSite	0201	
20L8B-2-FN	20L8B-2-FN	28	PLCC		3.6	ChipSite		
20L8B-2-FN	20L8B-2-FN	28	PLCC		3.6	PinSite	0201	
20L8B-2-NL	20L8B/D-NL	28	PLCC		3.6	ChipSite		
20L8B-2-NL	20L8B/D-NL	28	PLCC		3.6	PinSite	0201	
20L8B-ML	20L8B-ML	28	LCC	44	3.6	ChipSite		
20L8B-ML	20L8B-ML	28	LCC	44	3.6	PinSite	0202	
20L8B/B-2	20L8B/D-SOIC	24	SO		3.6	ChipSite		
20L8B/B-2	20L8B/D-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20R4	20R4	24	DIP		2.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
20R4-10	20R4-10	24	DIP		3.6	Site 48/40		
20R4-10	20R4-10-PLCC	28	PLCC		3.6	ChipSite		
20R4-10	20R4-10-PLCC	28	PLCC		3.6	PinSite	0201	
20R4-10/2	20R4-10/2	24	DIP	28	3.9	Site 48/40		
20R4-10/2	20R4-10/2-PL	28	PLCC	28	3.9	ChipSite		
20R4-10/2	20R4-10/2-PL	28	PLCC	28	3.9	PinSite	0201	
20R4-5	20R4-5	24	DIP	28	3.9	Site 48/40		
20R4-5	20R4-5-PLCC	28	PLCC	28	3.9	ChipSite		
20R4-5	20R4-5-PLCC	28	PLCC	28	3.9	PinSite	0201	
20R4-7	20R4-7	24	DIP		3.9	Site 48/40		
20R4-7	20R4-7-PLCC	28	PLCC		3.9	ChipSite		
20R4-7	20R4-7-PLCC	28	PLCC		3.9	PinSite	0201	
20R4A-ML	20R4A-ML	28	LCC		3.6	ChipSite		
20R4A-ML	20R4A-ML	28	LCC		3.6	PinSite	0202	
20R4A/A-2	20R4-SOIC	24	SO		3.6	ChipSite		
20R4A/A-2	20R4-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20R4A/A-2/B/B-2	20R4/A/A2/B	24	DIP		3.6	Site 48/40		
20R4A/A-2/B/FN	20R4/A/A2-FN	28	PLCC		3.6	ChipSite		
20R4A/A-2/B/FN	20R4/A/A2-FN	28	PLCC		3.6	PinSite	0201	
20R4A/A-2/B/NL	20R4/A/A2-NL	28	PLCC		3.6	ChipSite		
20R4A/A-2/B/NL	20R4/A/A2-NL	28	PLCC		3.6	PinSite	0201	
20R4B-2-FN	20R4B-2-FN	28	PLCC		3.6	ChipSite		
20R4B-2-FN	20R4B-2-FN	28	PLCC		3.6	PinSite	0201	
20R4B-2-NL	20R4B/D-NL	28	PLCC		3.6	ChipSite		
20R4B-2-NL	20R4B/D-NL	28	PLCC		3.6	PinSite	0201	
20R4B-ML	20R4B-ML	28	LCC	44	3.6	ChipSite		
20R4B-ML	20R4B-ML	28	LCC	44	3.6	PinSite	0202	
20R4B/B-2	20R4B/D-SOIC	24	SO		3.6	ChipSite		
20R4B/B-2	20R4B/D-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20R6	20R6	24	DIP		2.0	Site 48/40		
20R6-10	20R6-10	24	DIP		3.6	Site 48/40		
20R6-10	20R6-10-PLCC	28	PLCC		3.6	ChipSite		
20R6-10	20R6-10-PLCC	28	PLCC		3.6	PinSite	0201	
20R6-10/2	20R6-10/2	24	DIP	28	3.9	Site 48/40		
20R6-10/2	20R6-10/2-PL	28	PLCC	28	3.9	ChipSite		
20R6-10/2	20R6-10/2-PL	28	PLCC	28	3.9	PinSite	0201	
20R6-5	20R6-5	24	DIP	28	3.9	Site 48/40		
20R6-5	20R6-5-PLCC	28	PLCC	28	3.9	ChipSite		
20R6-5	20R6-5-PLCC	28	PLCC	28	4.2	PinSite	9901/0201	5201
20R6-7	20R6-7	24	DIP		3.9	Site 48/40		
20R6-7	20R6-7-PLCC	28	PLCC		3.9	ChipSite		
20R6-7	20R6-7-PLCC	28	PLCC		3.9	PinSite	0201	
20R6A-ML	20R6A-ML	20	LCC		3.6	ChipSite		
20R6A-ML	20R6A-ML	20	LCC		3.6	PinSite	0202	
20R6A/A-2	20R6-SOIC	24	SO		3.6	ChipSite		
20R6A/A-2	20R6-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20R6A/A-2/B/B-2	20R6/A/A2/B	24	DIP		3.6	Site 48/40		
20R6A/A-2/B/FN	20R6A/A2-FN	28	PLCC		3.6	ChipSite		
20R6A/A-2/B/FN	20R6A/A2-FN	28	PLCC		3.6	PinSite	0201	
20R6A/A-2/B/NL	20R6/A/A2-NL	28	PLCC		3.6	ChipSite		
20R6A/A-2/B/NL	20R6/A/A2-NL	28	PLCC		3.6	PinSite	0201	
20R6B-2-FN	20R6B-2-FN	28	PLCC		3.6	ChipSite		
20R6B-2-FN	20R6B-2-FN	28	PLCC		3.6	PinSite	0201	
20R6B-2-NL	20R6B/D-NL	28	PLCC		3.6	ChipSite		
20R6B-2-NL	20R6B/D-NL	28	PLCC		3.6	PinSite	0201	
20R6B-ML	20R6B-ML	28	LCC	44	3.6	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
20R6B-ML	20R6B-ML	28	LCC	44	3.6	PinSite	0202	
20R6B/B-2	20R6B/D-SOIC	24	SO		3.6	ChipSite		
20R6B/B-2	20R6B/D-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20R8	20R8	24	DIP		2.0	Site 48/40		
20R8-10	20R8-10	24	DIP		3.6	Site 48/40		
20R8-10	20R8-10-PLCC	28	PLCC		3.6	ChipSite		
20R8-10	20R8-10-PLCC	28	PLCC		3.6	PinSite	0201	
20R8-10/2	20R8-10/2	24	DIP	28	3.9	Site 48/40		
20R8-10/2	20R8-10/2-PL	28	PLCC	28	3.9	ChipSite		
20R8-10/2	20R8-10/2-PL	28	PLCC	28	3.9	PinSite	0201	
20R8-5	20R8-5	24	DIP	28	4.2	PinSite	9901	5102
20R8-5	20R8-5	24	DIP	28	3.9	Site 48/40		
20R8-5	20R8-5-PLCC	28	PLCC	28	3.9	ChipSite		
20R8-5	20R8-5-PLCC	28	PLCC	28	3.9	PinSite	0201	
20R8-7	20R8-7	24	DIP		3.9	Site 48/40		
20R8-7	20R8-7-PLCC	28	PLCC		3.9	ChipSite		
20R8-7	20R8-7-PLCC	28	PLCC		3.9	PinSite	0201	
20R8A-ML	20R8A-ML	28	LCC		3.6	ChipSite		
20R8A-ML	20R8A-ML	28	LCC		3.6	PinSite	0202	
20R8A/A-2	20R8-SOIC	24	SO		3.6	ChipSite		
20R8A/A-2	20R8-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20R8A/A-2/B/B-2	20R8/A/A2/B	24	DIP		3.6	Site 48/40		
20R8A/A-2/B/FN	20R8A/A2-FN	28	PLCC		3.6	ChipSite		
20R8A/A-2/B/FN	20R8A/A2-FN	28	PLCC		3.6	PinSite	0201	
20R8A/A-2/B/NL	20R8/A/A2-NL	28	PLCC		3.6	ChipSite		
20R8A/A-2/B/NL	20R8/A/A2-NL	28	PLCC		3.6	PinSite	0201	
20R8B-2-FN	20R8B-2-FN	28	PLCC		3.6	ChipSite		
20R8B-2-FN	20R8B-2-FN	28	PLCC		3.6	PinSite	0201	
20R8B-2-NL	20R8B/D-NL	28	PLCC		3.6	ChipSite		
20R8B-2-NL	20R8B/D-NL	28	PLCC		3.6	PinSite	0201	
20R8B-ML	20R8B-ML	28	LCC	44	3.6	ChipSite		
20R8B-ML	20R8B-ML	28	LCC	44	3.6	PinSite	0202	
20R8B/B-2	20R8B/D-SOIC	24	SO		3.6	ChipSite		
20R8B/B-2	20R8B/D-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20RA10	20RA10	24	DIP		3.6	Site 48/40		
20RA10	20RA10-SOIC	24	SO		3.6	ChipSite		
20RA10	20RA10-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20RA10-FN	20RA10-FN	28	PLCC		3.6	ChipSite		
20RA10-FN	20RA10-FN	28	PLCC		3.6	PinSite	0201	
20RA10-NL	20RA10-NL	28	PLCC		3.6	ChipSite		
20RA10-NL	20RA10-NL	28	PLCC		3.6	PinSite	0201	
20RP10	20RP10	24	DIP		2.0	Site 48/40		
20RP4	20RP4	24	DIP		2.0	Site 48/40		
20RP6	20RP6	24	DIP		2.0	Site 48/40		
20RP8	20RP8	24	DIP		2.0	Site 48/40		
20RS10	20RS10	24	DIP		3.6	Site 48/40		
20RS10	20RS10-SOIC	24	SO		3.6	ChipSite		
20RS10	20RS10-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20RS10-NL	20RS10-NL	28	PLCC		3.6	ChipSite		
20RS10-NL	20RS10-NL	28	PLCC		3.6	PinSite	0201	
20RS4	20RS4	24	DIP		3.6	Site 48/40		
20RS4	20RS4-SOIC	24	SO		3.6	ChipSite		
20RS4	20RS4-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20RS4-NL	20RS4-NL	28	PLCC		3.6	ChipSite		
20RS4-NL	20RS4-NL	28	PLCC		3.6	PinSite	0201	
20RS8	20RS8	24	DIP		3.6	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
20RS8	20RS8-SOIC	24	SO		3.6	ChipSite		
20RS8	20RS8-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20RS8-NL	20RS8-NL	28	PLCC		3.6	ChipSite		
20RS8-NL	20RS8-NL	28	PLCC		3.6	PinSite	0201	
20S10	20S10	24	DIP		3.6	Site 48/40		
20S10	20S10-SOIC	24	SO		3.6	ChipSite		
20S10	20S10-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20S10-NL	20S10-NL	28	PLCC		3.6	ChipSite		
20S10-NL	20S10-NL	28	PLCC		3.6	PinSite	0201	
20X10	20X10	24	DIP		3.6	Site 48/40		
20X10	20X10-SOIC	24	SO		3.6	ChipSite		
20X10	20X10-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20X10-ML	20X10-ML	28	LCC	44	3.6	ChipSite		
20X10-ML	20X10-ML	28	LCC	44	3.6	PinSite	0202	
20X10-NL	20X10-NL	28	PLCC		3.6	ChipSite		
20X10-NL	20X10-NL	28	PLCC		3.6	PinSite	0201	
20X10A	20X10A	24	DIP		3.6	Site 48/40		
20X10A	20X10A-SOIC	24	SO		3.6	ChipSite		
20X10A	20X10A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20X10A-FN	20X10A-FN	28	PLCC		3.6	ChipSite		
20X10A-FN	20X10A-FN	28	PLCC		3.6	PinSite	0201	
20X10A-NL	20X10A-NL	28	PLCC		3.6	ChipSite		
20X10A-NL	20X10A-NL	28	PLCC		3.6	PinSite	0201	
20X4	20X4	24	DIP		3.6	Site 48/40		
20X4	20X4-SOIC	24	SO		3.6	ChipSite		
20X4	20X4-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20X4-ML	20X4-ML	28	LCC	44	3.6	ChipSite		
20X4-ML	20X4-ML	28	LCC	44	3.6	PinSite	0202	
20X4-NL	20X4-NL	28	PLCC		3.6	ChipSite		
20X4-NL	20X4-NL	28	PLCC		3.6	PinSite	0201	
20X4A	20X4A	24	DIP		3.6	Site 48/40		
20X4A	20X4A-SOIC	24	SO		3.6	ChipSite		
20X4A	20X4A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20X4A-FN	20X4A-FN	28	PLCC		3.6	ChipSite		
20X4A-FN	20X4A-FN	28	PLCC		3.6	PinSite	0201	
20X4A-NL	20X4A-NL	28	PLCC		3.6	ChipSite		
20X4A-NL	20X4A-NL	28	PLCC		3.6	PinSite	0201	
20X8	20X8	24	DIP		3.6	Site 48/40		
20X8	20X8-SOIC	24	SO		3.6	ChipSite		
20X8	20X8-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20X8-ML	20X8-ML	28	LCC	44	3.6	ChipSite		
20X8-ML	20X8-ML	28	LCC	44	3.6	PinSite	0202	
20X8-NL	20X8-NL	28	PLCC		3.6	ChipSite		
20X8-NL	20X8-NL	28	PLCC		3.6	PinSite	0201	
20X8A	20X8A	24	DIP		3.6	Site 48/40		
20X8A	20X8A-SOIC	24	SO		3.6	ChipSite		
20X8A	20X8A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
20X8A-FN	20X8A-FN	28	PLCC		3.6	ChipSite		
20X8A-FN	20X8A-FN	28	PLCC		3.6	PinSite	0201	
20X8A-NL	20X8A-NL	28	PLCC		3.6	ChipSite		
20X8A-NL	20X8A-NL	28	PLCC		3.6	PinSite	0201	
20XRP10	20XRP10	24	DIP		2.0	Site 48/40		
20XRP4	20XRP4	24	DIP		2.0	Site 48/40		
20XRP6	20XRP6	24	DIP		2.0	Site 48/40		
20XRP8	20XRP8	24	DIP		2.0	Site 48/40		
22IP6	22IP6	24	DIP		3.6	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
22IP6	22IP6-PLCC	24	PLCC		3.6	PinSite	0201	
22P10	22P10	24	DIP		2.0	Site 48/40		
22P10	22P10-PLCC	28	PLCC		2.5	ChipSite		
22P10	22P10-PLCC	28	PLCC		3.0	PinSite	0201	
22RX8/A	22RX8A	24	DIP		3.6	Site 48/40		
22RX8/A	22RX8A-SOIC	24	SO		3.6	ChipSite		
22RX8/A	22RX8A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
22RX8/A-FN	22RX8A-FN	28	PLCC		3.6	ChipSite		
22RX8/A-FN	22RX8A-FN	28	PLCC		3.6	PinSite	0201	
22RX8/A-NL	22RX8A-NL	28	PLCC		3.6	ChipSite		
22RX8/A-NL	22RX8A-NL	28	PLCC		3.6	PinSite	0201	
22V10	22V10-15-LCC	28	LCC	44	2.5	ChipSite		
22V10	22V10-15-LCC	28	LCC	44	3.0	PinSite	0202	
22V10	22V10-15-PLCC	28	PLCC		2.0	ChipSite		
22V10	22V10-15-PLCC	28	PLCC		3.0	PinSite	0201	
22V10-10/-15	22V10-10	24	DIP		3.1	Site 48/40		
22V10-10/-15	22V10-10-PLCC	28	PLCC		3.1	ChipSite		
22V10-10/-15	22V10-10-PLCC	28	PLCC		4.2	PinSite	9901/0201	5201
22V10-7	22V10-7	24	DIP		4.2	Site 48/40		
22V10-7	22V10-7-PLCC	28	PLCC		4.2	ChipSite		
22V10-7	22V10-7-PLCC	28	PLCC		4.2	PinSite	0201	
22V10/A/B	22V10/A/B-15	24	DIP		2.0	Site 48/40		
22V10A	22V10/A-LCC	28	LCC	44	2.5	ChipSite		
22V10A	22V10/A-LCC	28	LCC	44	3.0	PinSite	0202	
22V10A	22V10/A-PLCC	28	PLCC		2.0	ChipSite		
22V10A	22V10/A-PLCC	28	PLCC		3.0	PinSite	0201	
22V10B	22V10/B-LCC	28	LCC	44	2.5	ChipSite		
22V10B	22V10/B-LCC	28	LCC	44	3.0	PinSite	0202	
22V10B	22V10/B-PLCC	28	PLCC		2.0	ChipSite		
22V10B	22V10/B-PLCC	28	PLCC		3.0	PinSite	0201	
22XP10	22XP10	24	DIP		2.0	Site 48/40		
23S8	23S8	20	DIP		2.2	Site 48/40		
2708	2708	24	DIP		2.0	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		1.7	Site 48/40		
27128A	27128A	28	DIP		2.1	SetSite		
27128A	27128A	28	DIP		1.7	Site 48/40		
27128AP	27128APC	28	DIP		2.0	SetSite		
27128AP	27128APC	28	DIP		1.7	Site 48/40		
2716	2716	24	DIP		2.0	SetSite		
2716	2716	24	DIP		2.0	Site 48/40		
2716B	2716B	24	DIP		2.5	SetSite		
2716B	2716B	24	DIP		2.5	Site 48/40		
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
2732B	2732B	24	DIP		2.5	SetSite		
2732B	2732B	24	DIP		2.5	Site 48/40		
27512	27512	28	DIP		2.4	SetSite		
27512	27512	28	DIP		2.4	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		1.5	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
2764	2764-LCC	32	LCC	44	2.6	ChipSite		
2764	2764-LCC	32	LCC	44	3.0	PinSite	0202	
2764A	2764A	28	DIP		2.1	SetSite		
2764A	2764A	28	DIP		2.1	Site 48/40		
2764AP	2764APC	28	DIP		2.0	SetSite		
2764AP	2764APC	28	DIP		1.5	Site 48/40		
27C010	27C010	32	DIP		3.8	SetSite		
27C010	27C010	32	DIP		3.8	Site 48/40		
27C010	27C010-LCC	32	LCC	44	3.8	ChipSite		
27C010	27C010-LCC	32	LCC	44	3.8	PinSite	0202	
27C010	27C010-PLCC	32	PLCC		3.8	ChipSite		
27C010	27C010-PLCC	32	PLCC		3.8	PinSite	0201	
27C020	27C020	32	DIP		3.8	SetSite		
27C020	27C020	32	DIP		3.8	Site 48/40		
27C020	27C020-LCC	32	LCC	44	3.8	ChipSite		
27C020	27C020-LCC	32	LCC	44	3.8	PinSite	0202	
27C040	27C040	32	DIP		3.9	SetSite		
27C040	27C040	32	DIP		3.9	Site 48/40		
27C040	27C040-PLCC	32	PLCC		4.1	ChipSite		
27C040	27C040-PLCC	32	PLCC		4.1	PinSite	0201	
27C080	27C080	32	DIP		4.0	Site 48/40		
27C100	27C100	32	DIP		3.8	SetSite		
27C100	27C100	32	DIP		3.8	Site 48/40		
27C1024	27C1024	40	DIP		3.8	SetSite		
27C1024	27C1024	40	DIP		3.8	Site 48/40		
27C1024	27C1024-LCC	44	LCC	44	3.8	ChipSite		
27C1024	27C1024-LCC	44	LCC	44	3.8	PinSite	0202	
27C1024	27C1024-PLCC	44	PLCC		3.8	ChipSite		
27C1024	27C1024-PLCC	44	PLCC		3.8	PinSite	0201	
27C128	27C128	28	DIP		3.8	SetSite		
27C128	27C128	28	DIP		3.8	Site 48/40		
27C128	27C128-LCC	32	LCC	44	3.8	ChipSite		
27C128	27C128-LCC	32	LCC	44	3.8	PinSite	0202	
27C128	27C128-PLCC	32	PLCC		3.8	ChipSite		
27C128	27C128-PLCC	32	PLCC		3.8	PinSite	0201	
27C191	27C191	24	DIP		2.2	SetSite		
27C191	27C191	24	DIP		2.2	Site 48/40		
27C2048	27C2048	40	DIP		3.8	SetSite		
27C2048	27C2048	40	DIP		3.8	Site 48/40		
27C2048	27C2048-LCC	44	LCC		3.8	ChipSite		
27C2048	27C2048-LCC	44	LCC		3.8	PinSite	0202	
27C2048	27C2048-PLCC	44	PLCC		3.8	ChipSite		
27C2048	27C2048-PLCC	44	PLCC		3.8	PinSite	0201	
27C256	27C256	28	DIP		3.8	SetSite		
27C256	27C256	28	DIP		3.8	Site 48/40		
27C256	27C256-LCC	32	LCC	44	3.8	ChipSite		
27C256	27C256-LCC	32	LCC	44	3.8	PinSite	0202	
27C256	27C256-PLCC	32	PLCC		3.8	ChipSite		
27C256	27C256-PLCC	32	PLCC		3.8	PinSite	0201	
27C291	27C291	24	DIP		2.2	SetSite		
27C291	27C291	24	DIP		2.2	Site 48/40		
27C400	27C400	40	DIP		3.9	Site 48/40		
27C4096	27C4096	40	DIP		4.0	SetSite		
27C4096	27C4096	40	DIP		3.9	Site 48/40		
27C4096	27C4096-PLCC	44	PLCC		4.0	ChipSite		
27C4096	27C4096-PLCC	44	PLCC		4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
27C43	27C43	24	DIP		3.0	SetSite		
27C43	27C43	24	DIP		2.7	Site 48/40		
27C45	27C45	28	DIP	38	2.7	Site 48/40		
27C49	27C49	24	DIP		2.2	SetSite		
27C49	27C49	24	DIP		2.2	Site 48/40		
27C51	27C51	28	DIP		2.5	SetSite		
27C51	27C51	28	DIP		2.5	Site 48/40		
27C512	27C512	28	DIP		3.8	SetSite		
27C512	27C512	28	DIP		3.8	Site 48/40		
27C512	27C512-LCC	32	LCC	44	3.8	ChipSite		
27C512	27C512-LCC	32	LCC	44	3.8	PinSite	0202	
27C512	27C512-PLCC	32	PLCC		3.8	ChipSite		
27C512	27C512-PLCC	32	PLCC		3.8	PinSite	0201	
27C64	27C64	28	DIP		3.8	SetSite		
27C64	27C64	28	DIP		3.8	Site 48/40		
27C64	27C64-LCC	32	LCC	44	3.8	ChipSite		
27C64	27C64-LCC	32	LCC	44	3.8	PinSite	0202	
27C64	27C64-PLCC	32	PLCC		3.8	ChipSite		
27C64	27C64-PLCC	32	PLCC		3.8	PinSite	0201	
27C800	27C800	42	DIP		4.1	Site 48		
27H010	27H010	32	DIP		3.8	SetSite		
27H010	27H010	32	DIP		3.8	Site 48/40		
27H010	27H010-LCC	32	LCC	44	4.2	ChipSite		
27H010	27H010-LCC	32	LCC	44	4.2	PinSite	0202	
27H010	27H010-PLCC	32	PLCC		4.2	ChipSite		
27H010	27H010-PLCC	32	PLCC		4.2	PinSite	0201	
27H256	27H256	28	DIP		3.8	Site 48/40		
27H256	27H256-PLCC	32	PLCC		4.2	ChipSite		
27H256	27H256-PLCC	32	PLCC		4.2	PinSite	0201	
27LS18	27LS18	16	DIP		2.2	Site 48/40		
27LS184	27LS184	18	DIP		2.2	Site 48/40		
27LS185	27LS185	18	DIP		2.2	Site 48/40		
27LS19	27LS19	16	DIP		2.2	Site 48/40		
27LV020	27LV020	32	DIP		3.6	Site 48/40		
27LV020	27LV020-PLCC	32	PLCC		3.6	ChipSite		
27LV020	27LV020-PLCC	32	PLCC		3.6	PinSite	0201	
27LV512	27LV512	32	DIP		3.6	Site 48/40		
27LV512	27LV512-PLCC	32	PLCC		3.6	ChipSite		
27LV512	27LV512-PLCC	32	PLCC		3.6	PinSite	0201	
27PS181	27PS181	24	DIP		2.2	Site 48/40		
27PS184	27PS184	18	DIP		2.2	Site 48/40		
27PS185	27PS185	18	DIP		2.2	Site 48/40		
27PS191	27PS191	24	DIP		2.2	Site 48/40		
27PS281	27PS281	24	DIP		2.2	Site 48/40		
27PS291	27PS291	24	DIP		2.2	Site 48/40		
27PS41	27PS41	20	DIP		2.2	Site 48/40		
27S12	27S12	16	DIP		2.2	Site 48/40		
27S13	27S13	16	DIP		2.2	Site 48/40		
27S13	27S13-PLCC	20	PLCC		2.2	ChipSite		
27S13	27S13-PLCC	20	PLCC		3.0	PinSite	0201	
27S15	27S15	24	DIP		2.2	Site 48/40		
27S18	27S18	16	DIP		2.2	Site 48/40		
27S180	27S180	24	DIP		2.2	Site 48/40		
27S181	27S181	24	DIP		2.2	Site 48/40		
27S184	27S184	18	DIP		2.2	Site 48/40		
27S185	27S185	18	DIP		2.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
27S185	27S185-PLCC	28	PLCC		2.2	ChipSite		
27S185	27S185-PLCC	28	PLCC		3.0	PinSite	0201	
27S19	27S19	16	DIP		2.2	Site 48/40		
27S19	27S19-PLCC	20	PLCC		2.2	ChipSite		
27S19	27S19-PLCC	20	PLCC		3.0	PinSite	0201	
27S190	27S190	24	DIP		2.2	Site 48/40		
27S191	27S191	24	DIP		2.2	Site 48/40		
27S191	27S191-PLCC	28	PLCC		2.2	ChipSite		
27S191	27S191-PLCC	28	PLCC		3.0	PinSite	0201	
27S20	27S20	16	DIP		2.2	Site 48/40		
27S21	27S21	16	DIP		2.2	Site 48/40		
27S21	27S21-PLCC	20	PLCC		2.2	ChipSite		
27S21	27S21-PLCC	20	PLCC		3.0	PinSite	0201	
27S23/A	27S23/A	20	DIP		3.6	Site 48/40		
27S25	27S25	24	DIP		2.2	Site 48/40		
27S25	27S25-PLCC	28	PLCC		2.2	ChipSite		
27S25	27S25-PLCC	28	PLCC		3.0	PinSite	0201	
27S26	27S26	22	DIP		2.2	Site 48/40		
27S27	27S27	22	DIP		2.2	Site 48/40		
27S28	27S28	20	DIP		2.2	Site 48/40		
27S280	27S280	24	DIP		2.2	Site 48/40		
27S281	27S281	24	DIP		2.2	Site 48/40		
27S281	27S281-PLCC	28	PLCC		2.2	ChipSite		
27S281	27S281-PLCC	28	PLCC		3.0	PinSite	0201	
27S29	27S29	20	DIP		2.2	Site 48/40		
27S29	27S29-LCC	20	LCC	44	2.7	ChipSite		
27S29	27S29-LCC	20	LCC	44	3.0	PinSite	0202	
27S290	27S290	24	DIP		2.2	Site 48/40		
27S291	27S291	24	DIP		2.2	Site 48/40		
27S30	27S30	24	DIP		2.2	Site 48/40		
27S31	27S31	24	DIP		2.2	Site 48/40		
27S31	27S31-LCC	28	LCC	44	2.7	ChipSite		
27S31	27S31-LCC	28	LCC	44	3.0	PinSite	0202	
27S32	27S32	18	DIP		2.2	Site 48/40		
27S33	27S33	18	DIP		2.2	Site 48/40		
27S33	27S33-PLCC	20	PLCC		2.2	ChipSite		
27S33	27S33-PLCC	20	PLCC		3.0	PinSite	0201	
27S35	27S35	24	DIP	1	2.2	Site 48/40		
27S35	27S35-PLCC	28	PLCC	1	2.2	ChipSite		
27S35	27S35-PLCC	28	PLCC	1	3.0	PinSite	0201	
27S37	27S37	24	DIP	1	2.2	Site 48/40		
27S40	27S40	20	DIP		2.2	Site 48/40		
27S41	27S41	20	DIP		2.2	Site 48/40		
27S43	27S43	24	DIP		2.2	Site 48/40		
27S45	27S45	24	DIP	3	2.3	Site 48/40		
27S45	27S45-PLCC	28	PLCC	3	2.3	ChipSite		
27S45	27S45-PLCC	28	PLCC	3	3.0	PinSite	0201	
27S45A	27S45A-PLCC	28	PLCC	3	3.1	ChipSite		
27S45A	27S45A-PLCC	28	PLCC	3	3.1	PinSite	0201	
27S45A-L32	27S45A-L32	32	LCC	3,44	3.0	ChipSite		
27S45A-L32	27S45A-L32	32	LCC	3,44	3.0	PinSite	0202	
27S45SA	27S45SA	24	DIP	3,19	2.3	Site 48/40		
27S45SA	27S45SA-PLCC	28	PLCC	3,19	2.5	ChipSite		
27S45SA	27S45SA-PLCC	28	PLCC	3,19	3.0	PinSite	0201	
27S45SA-L28	27S45SA-L28	28	LCC	3,19,44	2.8	ChipSite		
27S45SA-L28	27S45SA-L28	28	LCC	3,19,44	3.0	PinSite	0202	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
27S45SA-L32	27S45SA-L32	32	LCC	3,19,44	3.0	ChipSite		
27S45SA-L32	27S45SA-L32	32	LCC	3,19,44	3.0	PinSite	0202	
27S47	27S47	24	DIP	3	2.3	Site 48/40		
27S49	27S49	24	DIP		2.4	Site 48/40		
27S49A	27S49A	24	DIP		3.1	Site 48/40		
27S49A/B-L28	27S49A-L28	28	LCC	44	3.3	ChipSite		
27S49A/B-L28	27S49A-L28	28	LCC	44	3.3	PinSite	0202	
27S49SA	27S49SA	24	DIP	19	2.3	Site 48/40		
27S51	27S51	28	DIP		2.2	Site 48/40		
27S65	27S65	24	DIP	1	2.1	Site 48/40		
27S65	27S65-PLCC	28	PLCC	1	2.1	ChipSite		
27S65	27S65-PLCC	28	PLCC	1	3.0	PinSite	0201	
27S75	27S75	24	DIP	1	1.7	Site 48/40		
27S85	27S85	24	DIP	1	2.1	Site 48/40		
27S85	27S85-PLCC	28	PLCC	1	2.1	ChipSite		
27S85	27S85-PLCC	28	PLCC	1	3.0	PinSite	0201	
2817A	2817A	28	DIP		2.5	SetSite		
2817A	2817A	28	DIP		2.5	Site 48/40		
2864A	2864A	28	DIP		2.8	SetSite		
2864A	2864A	28	DIP		2.0	Site 48/40		
2864AE	2864AE	28	DIP		2.8	SetSite		
2864AE	2864AE	28	DIP		2.8	Site 48/40		
2864B	2864B	28	DIP		2.8	SetSite		
2864B	2864B	28	DIP		2.0	Site 48/40		
2864B	2864B-LCC	28	LCC	44	2.0	ChipSite		
2864B	2864B-LCC	28	LCC	44	3.0	PinSite	0202	
2864BE	2864BE	28	DIP		2.2	SetSite		
2864BE	2864BE	28	DIP		2.2	Site 48/40		
28F010	28F010-P1	32	DIP		4.2	Site 48/40		
28F010	28F010P1-LCC	32	LCC	44	4.2	ChipSite		
28F010	28F010P1-LCC	32	LCC	44	4.2	PinSite	0202	
28F010	28F010P1PLCC	32	PLCC		4.2	ChipSite		
28F010	28F010P1PLCC	32	PLCC		4.2	PinSite	0201	
28F010EC	28F010-TSOPE	32	TSOP		4.2	PinSite	9901	0702
28F010FC	28F010-TSOPF	32	TSOP		4.2	PinSite	9901	0702
28F020	28F020	32	DIP		4.2	Site 48/40		
28F020	28F020-PLCC	32	PLCC		4.2	ChipSite		
28F020	28F020-PLCC	32	PLCC		4.2	PinSite	0201	
28F256	28F256	32	DIP		4.2	Site 48/40		
28F256	28F256-PLCC	32	PLCC		4.2	ChipSite		
28F256	28F256-PLCC	32	PLCC		4.2	PinSite	0201	
28F512	28F512-P1	32	DIP		4.2	Site 48/40		
28F512	28F512P1PLCC	32	PLCC		4.2	ChipSite		
28F512	28F512P1PLCC	32	PLCC		4.2	PinSite	0201	
28F512-P1	28F512P1-LCC	32	LCC	44	4.2	ChipSite		
28F512-P1	28F512P1-LCC	32	LCC	44	4.2	PinSite	0202	
2971	2971	24	DIP		1.5	Site 48/40		
29774	29774	22	DIP		2.2	Site 48/40		
29CPL141	29CPL141	28	DIP	28	2.4	Site 48/40		
29CPL142	29CPL142	28	DIP	28	2.6	Site 48/40		
29CPL144	29CPL144	28	DIP	28	2.4	Site 48/40		
29CPL151	29CPL151	28	DIP	28	2.4	Site 48/40		
29CPL151	29CPL151PLCC	28	PLCC	28	2.8	ChipSite		
29CPL151	29CPL151PLCC	28	PLCC	28	3.0	PinSite	0201	
29CPL152	29CPL152	28	DIP	28	2.6	Site 48/40		
29CPL154	29CPL154	28	DIP	28	2.4	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
29F010	29F010	32	DIP	177,173	4.1	Site 48/40		
29F010	29F010-PLCC	32	PLCC	173,177	4.1	ChipSite		
29F010	29F010-PLCC	32	PLCC	173,177	4.1	PinSite	0201	
29LPL141	29LPL141	28	DIP	28	2.2	Site 48/40		
29PL141	29PL141	28	DIP	28	1.5	Site 48/40		
29PL142	29PL142	28	DIP	28	2.2	Site 48/40		
30K12	30K12	28	DIP		2.6	Site 48/40		
30S16	30S16	28	DIP		2.6	Site 48/40		
30S16	30S16-PLCC	28	PLCC		3.2	ChipSite		
30S16	30S16-PLCC	28	PLCC		3.2	PinSite	0201	
32R16	32R16	40	DIP		3.6	Site 48/40		
32R16	32R16-NL	44	PLCC		3.6	ChipSite		
32R16	32R16-NL	44	PLCC		3.6	PinSite	0201	
32VX10/A	32VX10/A	24	DIP		3.6	Site 48/40		
32VX10/A	32VX10-SOIC	24	SO		3.6	ChipSite		
32VX10/A	32VX10-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
53/63S1681J	63S1681J	24	DIP		2.2	Site 48/40		
53/63S485	53S485-LCC	28	LCC	44	3.0	ChipSite		
53/63S485	53S485-LCC	28	LCC	44	3.0	PinSite	0202	
5300	5300	16	DIP		1.0	Site 48/40		
5301	5301	16	DIP		1.0	Site 48/40		
5305	5305	16	DIP		1.0	Site 48/40		
5306	5306	16	DIP		1.0	Site 48/40		
5308	5308	20	DIP		2.8	Site 48/40		
5309	5309	20	DIP		2.8	Site 48/40		
5330	5330	16	DIP		1.0	Site 48/40		
5331	5331	16	DIP		1.0	Site 48/40		
5335	5335	24	DIP		2.8	Site 48/40		
5336	5336	24	DIP		2.8	Site 48/40		
5340	5340	24	DIP		2.8	Site 48/40		
5341	5341	24	DIP		2.8	Site 48/40		
5348	5348	20	DIP		2.8	Site 48/40		
5349	5349	20	DIP		2.8	Site 48/40		
5352	5352	18	DIP		2.8	Site 48/40		
5353	5353	18	DIP		2.8	Site 48/40		
5380	5380	24	DIP		2.8	Site 48/40		
5381	5381	24	DIP		2.8	Site 48/40		
5388	5388	18	DIP		2.8	Site 48/40		
5389	5389	18	DIP		2.8	Site 48/40		
53D1641	53D1641	24	DIP		2.2	Site 48/40		
53DA1643	53DA1643	24	DIP	1	2.2	Site 48/40		
53DA441	53DA441	24	DIP	1	2.2	Site 48/40		
53DA442	53DA442	24	DIP	1	2.2	Site 48/40		
53DA841	53DA841	24	DIP	1	2.2	Site 48/40		
53LS140	53LS140	16	DIP		2.2	Site 48/40		
53LS141	53LS141	16	DIP		2.2	Site 48/40		
53LS240	53LS240	16	DIP		2.2	Site 48/40		
53LS241	53LS241	16	DIP		2.2	Site 48/40		
53RA1681	53RA1681	24	DIP	1	2.2	Site 48/40		
53RA1681	53RA1681-LCC	28	LCC	1,44	2.3	ChipSite		
53RA1681	53RA1681-LCC	28	LCC	1,44	3.0	PinSite	0202	
53RA481	53RA481	24	DIP		2.2	Site 48/40		
53RS1681	53RS1681	24	DIP	1	2.2	Site 48/40		
53RS881	53RS881	24	DIP	1	2.2	Site 48/40		
53S080	53S080	16	DIP		2.2	Site 48/40		
53S081	53S081	16	DIP		2.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
53S140	53S140	16	DIP		2.2	Site 48/40		
53S141	53S141	16	DIP		2.2	Site 48/40		
53S1641	53S1641	20	DIP		2.2	Site 48/40		
53S1681	53S1681	24	DIP		2.2	Site 48/40		
53S240	53S240	16	DIP		2.2	Site 48/40		
53S241	53S241	16	DIP		2.2	Site 48/40		
53S280	53S280	20	DIP		2.2	Site 48/40		
53S281	53S281	20	DIP		2.2	Site 48/40		
53S285	53S285	24	DIP		2.2	Site 48/40		
53S3281	53S3281	24	DIP		2.2	Site 48/40		
53S440	53S440	18	DIP		2.2	Site 48/40		
53S441	53S441	18	DIP		2.2	Site 48/40		
53S480	53S480	20	DIP		2.2	Site 48/40		
53S481	53S481	20	DIP		2.2	Site 48/40		
53S485	53S485	24	DIP		2.2	Site 48/40		
53S840	53S840	18	DIP		2.2	Site 48/40		
53S841	53S841	18	DIP		2.2	Site 48/40		
53S881	53S881	24	DIP		2.2	Site 48/40		
5P16	5P16	24	DIP		2.1	Site 48/40		
5P16	5P16-PLCC	28	PLCC		2.1	ChipSite		
5P16	5P16-PLCC	28	PLCC		3.0	PinSite	0201	
5P8/A	5P8A	16	DIP		2.2	Site 48/40		
6300	6300	16	DIP		1.0	Site 48/40		
6301	6301	16	DIP		1.0	Site 48/40		
6305	6305	16	DIP		1.0	Site 48/40		
6306	6306	16	DIP		1.0	Site 48/40		
6308	6308	20	DIP		2.8	Site 48/40		
6309	6309	20	DIP		2.8	Site 48/40		
6330	6330	16	DIP		1.0	Site 48/40		
6331	6331	16	DIP		1.0	Site 48/40		
6335	6335	24	DIP		2.8	Site 48/40		
6336	6336	24	DIP		2.8	Site 48/40		
6340	6340	24	DIP		2.8	Site 48/40		
6341	6341	24	DIP		2.8	Site 48/40		
6348	6348	20	DIP		2.8	Site 48/40		
6349	6349	20	DIP		2.8	Site 48/40		
6352	6352	18	DIP		2.8	Site 48/40		
6353	6353	18	DIP		2.8	Site 48/40		
6380	6380	24	DIP		2.8	Site 48/40		
6381	6381	24	DIP		2.8	Site 48/40		
6388	6388	18	DIP		2.8	Site 48/40		
6389	6389	18	DIP		2.8	Site 48/40		
63D1641	63D1641	24	DIP		2.2	Site 48/40		
63D1641	63D1641PLCC	28	PLCC		2.2	ChipSite		
63D1641	63D1641PLCC	28	PLCC		3.0	PinSite	0201	
63DA1643	63DA1643	24	DIP	1	2.2	Site 48/40		
63DA441	63DA441	24	DIP	1	2.2	Site 48/40		
63DA442	63DA442	24	DIP	1	2.2	Site 48/40		
63DA841	63DA841	24	DIP	1	2.2	Site 48/40		
63DA841	63DA841PLCC	28	PLCC	1	2.2	ChipSite		
63DA841	63DA841PLCC	28	PLCC	1	3.0	PinSite	0201	
63LS140	63LS140	16	DIP		2.2	Site 48/40		
63LS141	63LS141	16	DIP		2.2	Site 48/40		
63LS240	63LS240	16	DIP		2.2	Site 48/40		
63LS241	63LS241	16	DIP		2.2	Site 48/40		
63RA1681	63RA1681	24	DIP	1	2.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
63RA1681	63RA1681PLCC	28	PLCC	1	2.2	ChipSite		
63RA1681	63RA1681PLCC	28	PLCC	1	3.0	PinSite	0201	
63RA481	63RA481	24	DIP		2.2	Site 48/40		
63RA481	63RA481PLCC	28	PLCC		2.2	ChipSite		
63RA481	63RA481PLCC	28	PLCC		3.0	PinSite	0201	
63RS1681	63RS1681	24	DIP	1	2.2	Site 48/40		
63RS1681	63RS1681PLCC	28	PLCC	1	2.2	ChipSite		
63RS1681	63RS1681PLCC	28	PLCC	1	3.0	PinSite	0201	
63RS881	63RS881	24	DIP	1	2.2	Site 48/40		
63RS881	63RS881PLCC	28	PLCC	1	2.2	ChipSite		
63RS881	63RS881PLCC	28	PLCC	1	3.0	PinSite	0201	
63S080	63S080	16	DIP		2.2	Site 48/40		
63S080	63S080PLCC	20	PLCC		2.2	ChipSite		
63S080	63S080PLCC	20	PLCC		3.0	PinSite	0201	
63S081	63S081	16	DIP		2.2	Site 48/40		
63S081	63S081PLCC	20	PLCC		2.2	ChipSite		
63S081	63S081PLCC	20	PLCC		3.0	PinSite	0201	
63S140	63S140	16	DIP		2.2	Site 48/40		
63S140	63S140PLCC	20	PLCC		2.2	ChipSite		
63S140	63S140PLCC	20	PLCC		3.0	PinSite	0201	
63S141	63S141	16	DIP		2.2	Site 48/40		
63S141	63S141PLCC	20	PLCC		2.2	ChipSite		
63S141	63S141PLCC	20	PLCC		3.0	PinSite	0201	
63S1641	63S1641	20	DIP		2.2	Site 48/40		
63S1641	63S1641PLCC	20	PLCC		2.2	ChipSite		
63S1641	63S1641PLCC	20	PLCC		3.0	PinSite	0201	
63S1681	63S1681	24	DIP		2.2	Site 48/40		
63S1681	63S1681PLCC	28	PLCC		2.2	ChipSite		
63S1681	63S1681PLCC	28	PLCC		3.0	PinSite	0201	
63S240	63S240	16	DIP		2.2	Site 48/40		
63S240	63S240PLCC	20	PLCC		2.2	ChipSite		
63S240	63S240PLCC	20	PLCC		3.0	PinSite	0201	
63S241	63S241	16	DIP		2.2	Site 48/40		
63S241	63S241PLCC	20	PLCC		2.2	ChipSite		
63S241	63S241PLCC	20	PLCC		3.0	PinSite	0201	
63S280	63S280	20	DIP		2.2	Site 48/40		
63S280	63S280PLCC	20	PLCC		2.2	ChipSite		
63S280	63S280PLCC	20	PLCC		3.0	PinSite	0201	
63S281	63S281	20	DIP		2.2	Site 48/40		
63S281	63S281PLCC	20	PLCC		2.2	ChipSite		
63S281	63S281PLCC	20	PLCC		3.0	PinSite	0201	
63S285	63S285	24	DIP		2.2	Site 48/40		
63S3281	63S3281	24	DIP		2.2	Site 48/40		
63S3281	63S3281PLCC	28	PLCC		2.2	ChipSite		
63S3281	63S3281PLCC	28	PLCC		3.0	PinSite	0201	
63S440	63S440	18	DIP		2.2	Site 48/40		
63S440	63S440PLCC	20	PLCC		2.2	ChipSite		
63S440	63S440PLCC	20	PLCC		3.0	PinSite	0201	
63S441	63S441	18	DIP		2.2	Site 48/40		
63S441	63S441PLCC	20	PLCC		2.2	ChipSite		
63S441	63S441PLCC	20	PLCC		3.0	PinSite	0201	
63S480	63S480	20	DIP		2.2	Site 48/40		
63S480	63S480PLCC	20	PLCC		2.2	ChipSite		
63S480	63S480PLCC	20	PLCC		3.0	PinSite	0201	
63S481	63S481	20	DIP		2.2	Site 48/40		
63S481	63S481PLCC	20	PLCC		2.2	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
63S481	63S481PLCC	20	PLCC		3.0	PinSite	0201	
63S485	63S485	24	DIP		2.2	Site 48/40		
63S840	63S840	18	DIP		2.2	Site 48/40		
63S841	63S841	18	DIP		2.2	Site 48/40		
63S841	63S841PLCC	20	PLCC		2.2	ChipSite		
63S841	63S841PLCC	20	PLCC		3.0	PinSite	0201	
63S881	63S881	24	DIP		2.2	Site 48/40		
63S881	63S881PLCC	28	PLCC		2.2	ChipSite		
63S881	63S881PLCC	28	PLCC		3.0	PinSite	0201	
6L16A	6L16A	24	DIP		3.6	Site 48/40		
6L16A	6L16A-SOIC	24	SO		3.6	ChipSite		
6L16A	6L16A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
6L16A-NL	6L16A-NL	28	PLCC		3.6	ChipSite		
6L16A-NL	6L16A-NL	28	PLCC		3.6	PinSite	0201	
6P16	6P16	24	DIP		2.1	Site 48/40		
6P16	6P16-PLCC	28	PLCC		2.1	ChipSite		
6P16	6P16-PLCC	28	PLCC		3.0	PinSite	0201	
8751H	8751H	40	DIP	2	1.5	Site 48/40		
8751H	8751H-PLCC	44	LCC	2,44	2.1	ChipSite		
8751H	8751H-PLCC	44	LCC	2,44	3.0	PinSite	0202	
8753H	8753H/9761H	40	DIP	2	1.5	Site 48/40		
8753H	8753H-PLCC	44	PLCC	2,44	2.1	ChipSite		
8753H	8753H-PLCC	44	PLCC	2,44	3.0	PinSite	0201	
87C51	87C51	40	DIP	2	3.8	Site 48/40		
87C51	87C51-LCC	44	LCC	2,44	3.8	ChipSite		
87C51	87C51-LCC	44	LCC	2,44	3.8	PinSite	0202	
87C51	87C51-PLCC	44	PLCC	2	3.8	ChipSite		
87C51	87C51-PLCC	44	PLCC	2	3.8	PinSite	0201	
87C521	87C521	40	DIP	2	3.8	Site 48/40		
87C521	87C521-LCC	44	LCC	2,44	3.8	ChipSite		
87C521	87C521-LCC	44	LCC	2,44	3.8	PinSite	0202	
87C52T2	87C52T2	40	DIP	2	3.4	Site 48/40		
87C52T2	87C52T2-LCC	44	LCC	2,44	3.4	ChipSite		
87C52T2	87C52T2-LCC	44	LCC	2,44	3.4	PinSite	0202	
87C541	87C541	40	DIP		3.0	Site 48/40		
87C541	87C541-LCC	44	LCC	44	3.0	ChipSite		
87C541	87C541-LCC	44	LCC	44	3.0	PinSite	0202	
8L14A	8L14A	24	DIP		3.6	Site 48/40		
8L14A	8L14A-SOIC	24	SO		3.6	ChipSite		
8L14A	8L14A-SOIC	24	SO		3.6	PinSite	0302/0301	.300 SOIC
8L14A-NL	8L14A-NL	28	PLCC		3.6	ChipSite		
8L14A-NL	8L14A-NL	28	PLCC		3.6	PinSite	0201	
8P4	8P4	16	DIP		2.2	Site 48/40		
8P8	8P8	20	DIP		2.2	Site 48/40		
9708	9708	24	DIP		2.8	SetSite		
9708	9708	24	DIP		2.1	Site 48/40		
9732A	9732A	24	DIP		2.0	SetSite		
9732A	9732A	24	DIP		2.0	Site 48/40		
9864	9864	28	DIP		2.0	SetSite		
9864	9864	28	DIP		1.5	Site 48/40		
9P4	9P4	16	DIP		2.2	Site 48/40		
9P8	9P8	20	DIP		2.2	Site 48/40		
9R8	9R8	24	DIP		2.2	Site 48/40		
9R8	9R8-PLCC	28	PLCC		2.2	ChipSite		
9R8	9R8-PLCC	28	PLCC		3.0	PinSite	0201	
C16L8Q	C16L8Q	20	DIP		2.4	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
C16L8Q	C16L8Q-PLCC	20	PLCC		3.2	ChipSite		
C16L8Q	C16L8Q-PLCC	20	PLCC		3.2	PinSite	0201	
C16L8Z	C16L8Z	20	DIP		2.3	Site 48/40		
C16L8Z	C16L8Z-PLCC	20	PLCC		2.5	ChipSite		
C16L8Z	C16L8Z-PLCC	20	PLCC		3.0	PinSite	0201	
C16R4Q	C16R4Q	20	DIP		2.4	Site 48/40		
C16R4Q	C16R4Q-PLCC	20	PLCC		2.7	ChipSite		
C16R4Q	C16R4Q-PLCC	20	PLCC		3.0	PinSite	0201	
C16R4Z	C16R4Z	20	DIP		2.3	Site 48/40		
C16R4Z	C16R4Z-PLCC	20	PLCC		2.5	ChipSite		
C16R4Z	C16R4Z-PLCC	20	PLCC		3.0	PinSite	0201	
C16R6Q	C16R6Q	20	DIP		2.4	Site 48/40		
C16R6Q	C16R6Q-PLCC	20	PLCC		2.7	ChipSite		
C16R6Q	C16R6Q-PLCC	20	PLCC		3.0	PinSite	0201	
C16R6Z	C16R6Z	20	DIP		2.3	Site 48/40		
C16R6Z	C16R6Z-PLCC	20	PLCC		2.5	ChipSite		
C16R6Z	C16R6Z-PLCC	20	PLCC		3.0	PinSite	0201	
C16R8Q	C16R8Q	20	DIP		2.4	Site 48/40		
C16R8Q	C16R8Q-PLCC	20	PLCC		2.7	ChipSite		
C16R8Q	C16R8Q-PLCC	20	PLCC		3.0	PinSite	0201	
C16R8Z	C16R8Z	20	DIP		2.3	Site 48/40		
C16R8Z	C16R8Z-PLCC	20	PLCC		2.5	ChipSite		
C16R8Z	C16R8Z-PLCC	20	PLCC		3.0	PinSite	0201	
C18U8	C18U8	20	DIP		2.4	Site 48/40		
C18U8	C18U8-PLCC	20	PLCC		2.4	ChipSite		
C18U8	C18U8-PLCC	20	PLCC		3.0	PinSite	0201	
C20L8Z	C20L8Z	24	DIP		1.7	Site 48/40		
C20L8Z	C20L8Z-FN	28	PLCC		2.5	ChipSite		
C20L8Z	C20L8Z-FN	28	PLCC		3.0	PinSite	0201	
C20R4Z	C20R4Z	24	DIP		1.7	Site 48/40		
C20R4Z	C20R4Z-FN	28	PLCC		2.4	ChipSite		
C20R4Z	C20R4Z-FN	28	PLCC		3.0	PinSite	0201	
C20R6Z	C20R6Z	24	DIP		1.7	Site 48/40		
C20R6Z	C20R6Z-FN	28	PLCC		2.4	ChipSite		
C20R6Z	C20R6Z-FN	28	PLCC		3.0	PinSite	0201	
C20R8Z	C20R8Z	24	DIP		1.7	Site 48/40		
C20R8Z	C20R8Z-FN	28	PLCC		2.4	ChipSite		
C20R8Z	C20R8Z-FN	28	PLCC		3.0	PinSite	0201	
C22V10	C22V10	24	DIP		2.3	Site 48/40		
C22V10	C22V10-PLCC	28	PLCC		3.2	ChipSite		
C22V10	C22V10-PLCC	28	PLCC		3.2	PinSite	0201	
CE16V8H-10/4	CE16V8H/4-SO	20	SO	49	4.1	ChipSite		
CE16V8H-10/4	CE16V8H/4-SO	20	SO	49	4.1	PinSite	0302/0301	.300 SOIC
CE16V8H-15	CE16V8H	20	DIP	49	3.9	Site 48/40		
CE16V8H-15	CE16V8H-PLCC	20	PLCC	49	3.9	ChipSite		
CE16V8H-15	CE16V8H-PLCC	20	PLCC	49	3.9	PinSite	0201	
CE16V8H-15/4	CE16V8H/4	20	DIP	49	3.9	Site 48/40		
CE16V8H-15/4	CE16V8H/4-PL	20	PLCC	49	3.9	ChipSite		
CE16V8H-15/4	CE16V8H/4-PL	20	PLCC	49	3.9	PinSite	0201	
CE16V8H-15/4	CE16V8H/4-SO	20	SO	49	4.1	ChipSite		
CE16V8H-15/4	CE16V8H/4-SO	20	SO	49	4.1	PinSite	0302/0301	.300 SOIC
CE16V8H-25	CE16V8H	20	DIP	49	3.9	Site 48/40		
CE16V8H-25	CE16V8H-PLCC	20	PLCC	49	3.9	ChipSite		
CE16V8H-25	CE16V8H-PLCC	20	PLCC	49	3.9	PinSite	0201	
CE16V8H-25/4	CE16V8	20	DIP	49	3.9	Site 48/40		
CE16V8H-25/4	CE16V8-PLCC	20	PLCC	49	3.9	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
CE16V8H-25/4	CE16V8-PLCC	20	PLCC	49	3.9	PinSite	0201	
CE16V8H-25/4	CE16V8-SOIC	20	SO	49	3.9	ChipSite		
CE16V8H-25/4	CE16V8-SOIC	20	SO	49	3.9	PinSite	0302/0301	.300 SOIC
CE16V8H-7/5	CE16V8/5	20	DIP	49	3.9	Site 48/40		
CE16V8H-7/5	CE16V8/5-PLC	20	PLCC	49	3.9	ChipSite		
CE16V8H-7/5	CE16V8/5-PLC	20	PLCC	49	4.2	PinSite	9901/0201	5202
CE16V8HD-15	CE16V8HD	24	DIP		3.9	Site 48/40		
CE16V8HD-15	CE16V8HD-PLC	28	PLCC		4.2	ChipSite		
CE16V8HD-15	CE16V8HD-PLC	28	PLCC		4.2	PinSite	0201	
CE16V8Q-10/5	CE16V8Q/4	20	DIP	49	3.9	Site 48/40		
CE16V8Q-10/5	CE16V8Q/4-PL	20	PLCC	49	3.9	ChipSite		
CE16V8Q-10/5	CE16V8Q/4-PL	20	PLCC	49	3.9	PinSite	0201	
CE16V8Q-10/5	CE16V8Q/4-SO	20	SO	49	4.1	ChipSite		
CE16V8Q-10/5	CE16V8Q/4-SO	20	SO	49	4.1	PinSite	0302/0301	.300 SOIC
CE16V8Q-15	CE16V8Q	20	DIP	49	3.9	Site 48/40		
CE16V8Q-15	CE16V8Q-PLCC	20	PLCC	49	3.9	ChipSite		
CE16V8Q-15	CE16V8Q-PLCC	20	PLCC	49	3.9	PinSite	0201	
CE16V8Q-15/4	CE16V8Q/4	20	DIP	49	3.9	Site 48/40		
CE16V8Q-15/4	CE16V8Q/4-PL	20	PLCC	49	3.9	ChipSite		
CE16V8Q-15/4	CE16V8Q/4-PL	20	PLCC	49	3.9	PinSite	0201	
CE16V8Q-15/4	CE16V8Q/4-SO	20	SO	49	4.1	ChipSite		
CE16V8Q-15/4	CE16V8Q/4-SO	20	SO	49	4.1	PinSite	0302/0301	.300 SOIC
CE16V8Q-25	CE16V8Q	20	DIP	49	3.9	Site 48/40		
CE16V8Q-25	CE16V8Q-PLCC	20	PLCC	49	3.9	ChipSite		
CE16V8Q-25	CE16V8Q-PLCC	20	PLCC	49	3.9	PinSite	0201	
CE16V8Q-25/4	CE16V8Q/4	20	DIP	49	3.9	Site 48/40		
CE16V8Q-25/4	CE16V8Q/4-PL	20	PLCC	49	3.9	ChipSite		
CE16V8Q-25/4	CE16V8Q/4-PL	20	PLCC	49	3.9	PinSite	0201	
CE16V8Z-25/4	CE16V8Z	20	DIP		3.9	Site 48/40		
CE16V8Z-25/4	CE16V8Z-PLCC	20	PLCC		3.9	ChipSite		
CE16V8Z-25/4	CE16V8Z-PLCC	20	PLCC		3.9	PinSite	0201	
CE16V8Z-25/4	CE16V8Z-SOIC	20	SO	49	4.2	ChipSite		
CE16V8Z-25/4	CE16V8Z-SOIC	20	SO	49	4.2	PinSite	0302/0301	.300 SOIC
CE20RA10H-15/4	CE20RA10	24	DIP	49	4.1	Site 48/40		
CE20RA10H-15/4	CE20RA10-PLC	28	PLCC	49	4.1	ChipSite		
CE20RA10H-15/4	CE20RA10-PLC	28	PLCC	49	4.1	PinSite	0201	
CE20RA10H-25/4	CE20RA10H/4	24	DIP	49	4.1	Site 48/40		
CE20RA10H-25/4	CE20RA10/4-P	28	PLCC	49	4.1	ChipSite		
CE20RA10H-25/4	CE20RA10/4-P	28	PLCC	49	4.1	PinSite	0201	
CE20RA10Q-15/4	CE20RA10Q/4	24	DIP	49	4.1	Site 48/40		
CE20RA10Q-15/4	CE20RA10/4-P	28	PLCC	49	4.1	ChipSite		
CE20RA10Q-15/4	CE20RA10/4-P	28	PLCC	49	4.1	PinSite	0201	
CE20RA10Q-25/4	CE20RA10Q/4	24	DIP	49	4.1	Site 48/40		
CE20RA10Q-25/4	CE20RA10/4-P	28	PLCC	49	4.1	ChipSite		
CE20RA10Q-25/4	CE20RA10/4-P	28	PLCC	49	4.1	PinSite	0201	
CE20RA10Z	CE20RA10Z	24	DIP		3.9	Site 48/40		
CE20RA10Z	CE20RA10ZPLC	28	PLCC		3.9	ChipSite		
CE20RA10Z	CE20RA10ZPLC	28	PLCC		3.9	PinSite	0201	
CE20V8H-10/4	CE20V8	24	DIP	49	3.9	Site 48/40		
CE20V8H-10/4	CE20V8-FN	28	PLCC	49	4.0	ChipSite		
CE20V8H-10/4	CE20V8-FN	28	PLCC	49	4.0	PinSite	0201	
CE20V8H-15	CE20V8H	24	DIP	49	3.9	Site 48/40		
CE20V8H-15	CE20V8H-PLCC	28	PLCC	49	3.9	ChipSite		
CE20V8H-15	CE20V8H-PLCC	28	PLCC	49	3.9	PinSite	0201	
CE20V8H-15/4	CE20V8	24	DIP	49	3.9	Site 48/40		
CE20V8H-15/4	CE20V8-FN	28	PLCC	49	4.0	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
CE20V8H-15/4	CE20V8-FN	28	PLCC	49	4.0	PinSite	0201	
CE20V8H-25	CE20V8H	24	DIP	49	3.9	Site 48/40		
CE20V8H-25	CE20V8H-PLCC	28	PLCC	49	3.9	ChipSite		
CE20V8H-25	CE20V8H-PLCC	28	PLCC	49	3.9	PinSite	0201	
CE20V8H-25/4	CE20V8H/4	24	DIP	49	3.9	Site 48/40		
CE20V8H-25/4	CE20V8H/4-PL	28	PLCC	49	4.0	ChipSite		
CE20V8H-25/4	CE20V8H/4-PL	28	PLCC	49	4.0	PinSite	0201	
CE20V8H-5/5	CE20V8H/5-PL	28	PLCC	49	4.1	ChipSite		
CE20V8H-5/5	CE20V8H/5-PL	28	PLCC	49	4.1	PinSite	0201	
CE20V8H-7/5	CE20V8H/5	24	DIP	49	4.1	Site 48/40		
CE20V8H-7/5	CE20V8H/5-PL	28	PLCC	49	4.1	ChipSite		
CE20V8H-7/5	CE20V8H/5-PL	28	PLCC	49	4.1	PinSite	0201	
CE20V8Q-15	CE20V8Q	24	DIP	49	3.9	Site 48/40		
CE20V8Q-15	CE20V8Q-PLCC	28	PLCC	49	3.9	ChipSite		
CE20V8Q-15	CE20V8Q-PLCC	28	PLCC	49	3.9	PinSite	0201	
CE20V8Q-15/4	CE20V8Q/4	24	DIP	49	3.9	Site 48/40		
CE20V8Q-15/4	CE20V8Q/4-PL	28	PLCC	49	4.0	ChipSite		
CE20V8Q-15/4	CE20V8Q/4-PL	28	PLCC	49	4.0	PinSite	0201	
CE20V8Q-25	CE20V8Q	24	DIP	49	3.9	Site 48/40		
CE20V8Q-25	CE20V8Q-PLCC	28	PLCC	49	3.9	ChipSite		
CE20V8Q-25	CE20V8Q-PLCC	28	PLCC	49	3.9	PinSite	0201	
CE20V8Q-25/4	CE20V8Q/4	24	DIP	49	3.9	Site 48/40		
CE20V8Q-25/4	CE20V8Q/4-PL	28	PLCC	49	4.0	ChipSite		
CE20V8Q-25/4	CE20V8Q/4-PL	28	PLCC	49	4.0	PinSite	0201	
CE22V10H-10/5	CE22V10H/5	24	DIP	49,28	4.2	PinSite	9901	5101
CE22V10H-10/5	CE22V10H/5	24	DIP	49,28	4.2	Site 48/40		
CE22V10H-10/5	CE22V10H/5-P	28	PLCC	49,28	4.2	ChipSite		
CE22V10H-10/5	CE22V10H/5-P	28	PLCC	49,28	4.2	PinSite	9901/0201	5201
CE22V10H-15	CE22V10H	24	DIP	49	3.9	Site 48/40		
CE22V10H-15	CE22V10H-PLC	28	PLCC	49	3.9	ChipSite		
CE22V10H-15	CE22V10H-PLC	28	PLCC	49	3.9	PinSite	0201	
CE22V10H-15/4	CE22V10H/4	24	DIP	49,28	4.2	Site 48/40		
CE22V10H-15/4	CE22V10H/4-S	24	SO	49	4.2	ChipSite		
CE22V10H-15/4	CE22V10H/4-S	24	SO	49	4.2	PinSite	0302/0301	.300 SOIC
CE22V10H-15/4	CE22V10H/4-P	28	PLCC	49,28	4.2	ChipSite		
CE22V10H-15/4	CE22V10H/4-P	28	PLCC	49,28	4.2	PinSite	0201	
CE22V10H-25	CE22V10	24	DIP	49	4.0	Site 48/40		
CE22V10H-25	CE22V10-SOIC	24	SO	49	4.0	ChipSite		
CE22V10H-25	CE22V10-SOIC	24	SO	49	4.0	PinSite	0302/0301	.300 SOIC
CE22V10H-25	CE22V10-FN	28	PLCC	49	4.0	ChipSite		
CE22V10H-25	CE22V10-FN	28	PLCC	49	4.0	PinSite	0201	
CE22V10H-25/4	CE22V10H/4	24	DIP	49,28	4.2	Site 48/40		
CE22V10H-25/4	CE22V10H/4-S	24	SO	49	4.2	ChipSite		
CE22V10H-25/4	CE22V10H/4-S	24	SO	49	4.2	PinSite	0302/0301	.300 SOIC
CE22V10H-25/4	CE22V10H/4-P	28	PLCC	49,28	4.2	ChipSite		
CE22V10H-25/4	CE22V10H/4-P	28	PLCC	49,28	4.2	PinSite	0201	
CE22V10H-7/5	CE22V10H/5	24	DIP	49,28	4.2	Site 48/40		
CE22V10H-7/5	CE22V10H/5-P	28	PLCC	49,28	4.2	ChipSite		
CE22V10H-7/5	CE22V10H/5-P	28	PLCC	49,28	4.2	PinSite	0201	
CE22V10Q-10/5	CE22V10Q/5	24	DIP	49,28	4.2	Site 48/40		
CE22V10Q-25	CE22V10Q	24	DIP	49	4.0	Site 48/40		
CE22V10Q-25	CE22V10Q-PLC	28	PLCC	49	3.9	ChipSite		
CE22V10Q-25	CE22V10Q-PLC	28	PLCC	49	3.9	PinSite	0201	
CE22V10Q-25/4	CE22V10Q/4	24	DIP	49,28	4.2	Site 48/40		
CE22V10Q-25/4	CE22V10Q/4-P	28	PLCC	49,28	4.2	ChipSite		
CE22V10Q-25/4	CE22V10Q/4-P	28	PLCC	49,28	4.2	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI (continued)								
CE22V10Z-25	CE22V10Z	24	DIP		3.6	Site 48/40		
CE22V10Z-25	CE22V10Z-PLC	28	PLCC		4.1	ChipSite		
CE22V10Z-25	CE22V10Z-PLC	28	PLCC		4.1	PinSite	0201	
CE24V10	CE24V10/H	28	DIP		3.9	Site 48		
CE24V10H-15	CE24V10/H-PL	28	PLCC		3.9	PinSite	0201	
CE26V12H	CE26V12H	28	DIP	53	3.9	Site 48		
CE26V12H	CE26V12HPLCC	28	PLCC	53	3.9	PinSite	0201	
CE26V12H/4	CE26V12H/4	28	DIP		4.1	Site 48		
CE26V12H/4	CE26V12H/4-P	28	PLCC		4.0	PinSite	0201	
CE29M16-25/-35	CE29M16	24	DIP		3.9	Site 48/40		
CE29M16/4	CE29M16/4	24	DIP		3.9	Site 48/40		
CE29M16/4	CE29M16/4PLC	28	PLCC		3.9	ChipSite		
CE29M16/4	CE29M16/4PLC	28	PLCC		3.9	PinSite	0201	
CE29MA16-25/-35	CE29MA16	24	DIP		3.9	Site 48/40		
CE29MA16/4	CE29MA16/4	24	DIP		4.2	Site 48/40		
CE29MA16/4	CE29MA164PLC	28	PLCC		4.2	ChipSite		
CE29MA16/4	CE29MA164PLC	28	PLCC		4.2	PinSite	0201	
CE610	CE610	24	DIP		4.2	PinSite	9901	5101
CE610	CE610	24	DIP		3.9	Site 48/40		
CE610	CE610-PLCC	28	PLCC		3.9	PinSite	9901	5201
CE610H	CE610H	24	DIP		4.2	PinSite	9901	5101
CE610H	CE610H	24	DIP		4.0	Site 48/40		
CE610H	CE610H-PLCC	28	PLCC		4.0	PinSite	9901	5201
MACH110	MACH110-LCC	44	LCC		4.0	ChipSite		
MACH110	MACH110-LCC	44	LCC		4.0	PinSite	0202	
MACH110	MACH110-PLCC	44	PLCC		4.0	ChipSite		
MACH110	MACH110-PLCC	44	PLCC		4.0	PinSite	0201	
MACH110	MACH110-CQFP	44	QFPCAR		4.0	PinSite	9901	0521
MACH120	MACH120-PLCC	68	PLCC		4.0	PinSite	0201	
MACH130	MACH130-PLCC	84	PLCC		4.0	PinSite	0201	
MACH130	MACH130-CQFP	84	QFPCAR		4.0	PinSite	9901	0520
MACH210	MACH210-PLCC	44	PLCC		4.0	ChipSite		
MACH210	MACH210-PLCC	44	PLCC		4.0	PinSite	0201	
MACH210	MACH210-CQFP	44	QFPCAR		4.0	PinSite	9901	0521
MACH215	MACH215-PLCC	44	PLCC		3.9	PinSite	0201	
MACH220	MACH220-PLCC	68	PLCC		4.0	PinSite	0201	
MACH230	MACH230-LCC	84	LCC		3.9	PinSite	0202	
MACH230	MACH230-PLCC	84	PLCC		3.9	PinSite	0201	
MACH435	MACH435-PLCC	84	PLCC		4.1	PinSite	0201	
PLS105	PLS105A/B	28	DIP		2.2	Site 48/40		
PLS105	PLS105-PLCC	28	PLCC		2.2	ChipSite		
PLS105	PLS105-PLCC	28	PLCC		3.0	PinSite	0201	
PLS167	PLS167A/B	24	DIP		2.2	Site 48/40		
PLS168	PLS168A/B	24	DIP		2.2	Site 48/40		
Altera Corporation								
1200	1200	40	DIP		1.0	Site 48/40		
1210	1210	40	DIP		1.0	Site 48/40		
1210	1210-JLCC	44	JLCC		3.3	ChipSite		
1210	1210-JLCC	44	JLCC		3.3	PinSite	0201	
1210	1210-PLCC	44	PLCC		1.0	ChipSite		
1210	1210-PLCC	44	PLCC		3.0	PinSite	0201	
1400	1400	40	DIP		3.6	Site 48/40		
1400	1400-JLCC	44	JLCC		3.6	PinSite	0201	
1800	1800-JLCC	68	JLCC		3.3	ChipSite		
1800	1800-JLCC	68	JLCC		3.3	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Altera Corporation (continued)								
1800	1800-PGA	68	PGA		3.2	PinSite	0402/0401	
1800	1800-PLCC	68	PLCC		2.7	ChipSite		
1800	1800-PLCC	68	PLCC		3.0	PinSite	0201	
1810	1810-PGA	68	PGA		3.9	PinSite	0402/0401	
1810-20/25	1810-20/25PL	68	PLCC		3.3	ChipSite		
1810-20/25	1810-20/25PL	68	PLCC		3.3	PinSite	0201	
1810-20T/25T/35T	1810T-PLCC	68	PLCC	141	3.3	ChipSite		
1810-20T/25T/35T	1810T-PLCC	68	PLCC	141	3.3	PinSite	0201	
1810-20T/25T/35T-NEW	1810T-NEWPLC	68	PLCC	141	3.7	ChipSite		
1810-20T/25T/35T-NEW	1810T-NEWPLC	68	PLCC	141	3.7	PinSite	0201	
1810-35/40	1810-35/40JL	68	JLCC		3.3	ChipSite		
1810-35/40	1810-35/40JL	68	JLCC		3.3	PinSite	0201	
1810-35/40	1810-35/40PL	68	PLCC		3.3	ChipSite		
1810-35/40	1810-35/40PL	68	PLCC		3.3	PinSite	0201	
1830	1830-PLCC	68	PLCC		3.6	ChipSite		
1830	1830-PLCC	68	PLCC		3.6	PinSite	0201	
300	300	20	DIP		1.7	Site 48/40		
310	310	20	DIP	129	3.8	Site 48		
320	320	20	DIP		1.1	Site 48/40		
330	330	20	DIP		3.6	Site 48/40		
330	330-PLCC	20	PLCC		3.6	ChipSite		
330	330-PLCC	20	PLCC		3.6	PinSite	0201	
330	330-SOIC	20	SO		3.7	ChipSite		
330	330-SOIC	20	SO		3.7	PinSite	0302/0301	.300 SOIC
448	448	28	DIP	49,86	2.6	Site 48		
448	448-JLCC	28	JLCC	49,86	2.6	ChipSite		
448	448-JLCC	28	JLCC	49,86	3.0	PinSite	0201	
448	448-PLCC	28	PLCC	49,86	4.1	ChipSite		
448	448-PLCC	28	PLCC	49,86	4.1	PinSite	0201	
5016	5016	20	DIP	55	3.8	Site 48		
5016	5016-PLCC	20	PLCC	55	4.1	PinSite	0201	
5016	5016-SOIC	20	SO	55	4.1	PinSite	0302/0301	.300 SOIC
5032	5032	28	DIP	55	4.0	Site 48		
5032	5032-JLCC	28	JLCC	55	3.9	PinSite	0201	
5032	5032-PLCC	28	PLCC	55	3.9	PinSite	0201	
5064	5064-JLCC	44	JLCC	54	3.7	PinSite	0201	
5064	5064-PLCC	44	PLCC	54	4.1	PinSite	0201	
512	512	24	DIP	49	2.8	Site 48/40		
5128	5128-JLCC	68	JLCC	54	3.8	PinSite	0201	
5128	5128-PGA	68	PGA	54	3.8	PinSite	0402/0401	
5128	5128-PLCC	68	PLCC	54	3.8	PinSite	0201	
5130	5130-JLCC	84	JLCC	54	4.2	PinSite	0201	
5130	5130-PLCC	84	PLCC	54	4.2	PinSite	0201	
5130	5130-PGA	100	PGA	54	4.2	PinSite	9901	0401
5130	5130-QFP	100	QFP	54	4.2	PinSite	9901	0519
5130	5130-CQFP	100	QFPCAR	54	4.2	PinSite	9901	0526
5192	5192-JLCC	84	JLCC	54	4.2	PinSite	0201	
5192	5192-PGA	84	PGA	54	4.2	PinSite	9901	0401
5192	5192-PLCC	84	PLCC	54	4.2	PinSite	0201	
600	600	24	DIP	37	2.7	Site 48/40		
600	600-JLCC	28	JLCC	37	3.3	ChipSite		
600	600-JLCC	28	JLCC	37	3.3	PinSite	0201	
600	600-PLCC	28	PLCC	37	2.7	ChipSite		
600	600-PLCC	28	PLCC	37	3.0	PinSite	0201	
630	630	24	DIP		3.3	Site 48/40		
630	630-SOIC	24	SO		3.7	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Altera Corporation (continued)								
630	630-SOIC	24	SO		3.7	PinSite	0302/0301	.300 SOIC
630	630-PLCC	28	PLCC		3.3	ChipSite		
630	630-PLCC	28	PLCC		3.3	PinSite	0201	
7032	7032-JLCC	44	JLCC		4.2	PinSite	0201	
7032	7032-PLCC	44	PLCC		4.2	PinSite	0201	
7032	7032-QFP	44	QFP		4.2	PinSite	9901	0529
7096	7096-68JLCC	68	JLCC	55	4.2	PinSite	0201	
7096	7096-68PLCC	68	PLCC	55	4.2	PinSite	0201	
7096	7096-84JLCC	84	JLCC	55	4.2	PinSite	0201	
7096	7096-84PLCC	84	PLCC	55	4.2	PinSite	0201	
7192	7192-PGA	160	PGA		4.3	PinSite	9901	0403
7256	7256-192PGA	192	PGA		4.3	PinSite	9901	0404
900	900	40	DIP		3.6	Site 48/40		
900	900-JLCC	44	JLCC		3.6	ChipSite		
900	900-JLCC	44	JLCC		3.6	PinSite	0201	
900	900-PLCC	44	PLCC		3.6	ChipSite		
900	900-PLCC	44	PLCC		3.6	PinSite	0201	
910	910	40	DIP		3.3	Site 48/40		
910	910-JLCC	44	JLCC		3.3	ChipSite		
910	910-JLCC	44	JLCC		3.3	PinSite	0201	
910	910-PLCC	44	PLCC		3.3	ChipSite		
910	910-PLCC	44	PLCC		3.3	PinSite	0201	
910A	910A	40	DIP		3.3	Site 48/40		
910A	910A-JLCC	44	JLCC		3.5	ChipSite		
910A	910A-JLCC	44	JLCC		3.5	PinSite	0201	
910A	910A-PLCC	44	PLCC		3.3	ChipSite		
910A	910A-PLCC	44	PLCC		3.3	PinSite	0201	
910T	910T	40	DIP		3.3	Site 48/40		
910T	910T-PLCC	44	PLCC		3.3	ChipSite		
910T	910T-PLCC	44	PLCC		3.3	PinSite	0201	
EP610DC-15	610-15/20	24	DIP	37	3.6	Site 48/40		
EP610DC-25	610-25/30	24	DIP	37	4.0	Site 48/40		
EP610DC-35	610-35/40	24	DIP	37	4.0	Site 48/40		
EP610JC-15	610-15/20JLC	28	JLCC		3.6	ChipSite		
EP610JC-15	610-15/20JLC	28	JLCC		3.6	PinSite	0201	
EP610JC-25	610-25/30JLC	28	JLCC	37	4.0	ChipSite		
EP610JC-25	610-25/30JLC	28	JLCC	37	4.2	PinSite	9901/0201	5201
EP610JC-35	610-35/40-JLC	28	JLCC	37	4.0	ChipSite		
EP610JC-35	610-35/40-JLC	28	JLCC	37	4.2	PinSite	9901/0201	5201
EP610LC-15	610-15/20PLC	28	PLCC		3.6	ChipSite		
EP610LC-15	610-15/20PLC	28	PLCC		3.6	PinSite	0201	
EP610LC-15T	610T-15/20PL	28	PLCC	37	4.2	PinSite	0201	
EP610LC-20T	610T-15/20PL	28	PLCC	37	4.2	PinSite	0201	
EP610LC-25	610-25/30PLC	28	PLCC	37	4.0	ChipSite		
EP610LC-25	610-25/30PLC	28	PLCC	37	4.0	PinSite	0201	
EP610LC-25T	610T-25PLC	28	PLCC	37	4.2	PinSite	0201	
EP610LC-35	610-35/40-PLC	28	PLCC	37	4.0	ChipSite		
EP610LC-35	610-35/40-PLC	28	PLCC	37	4.0	PinSite	0201	
EP610PC-15T	610T-15/20	24	DIP	37	4.2	Site 48/40		
EP610PC-20T	610T-15/20	24	DIP	37	4.2	Site 48/40		
EP610PC-25T	610T-25	24	DIP	37	4.2	PinSite	9901	5101
EP610PC-25T	610T-25	24	DIP	37	4.0	Site 48/40		
EP610SC-35	610-25/30-SO	24	SO		4.0	ChipSite		
EP610SC-35	610-25/30-SO	24	SO		4.0	PinSite	0302/0301	.300 SOIC
EPS464	EPS464-JLCC	44	JLCC		4.2	PinSite	0201	
EPS464	EPS464-PLCC	44	PLCC		4.2	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Asahi Kasei								
27CX161	27CX161	24	DIP		3.1	Site 48/40		
27CX162	27CX162	24	DIP		3.1	Site 48/40		
27CX321	27CX321	24	DIP	31	3.6	Site 48/40		
27CX322	27CX322	24	DIP	31	3.6	Site 48/40		
27CX641	27CX641	24	DIP	31	3.6	Site 48/40		
27CX642	27CX642	24	DIP	31	3.6	Site 48/40		
28C64	28C64	28	DIP		3.1	Site 48/40		
6420	6420-SOIC	8	SO		4.2	PinSite	0302/0301	.150 SOIC
6440	6440-SOIC	8	SO		4.2	PinSite	0302/0301	.150 SOIC
93C45	93C45	8	DIP		4.0	Site 48/40		
93C45F	93C45-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
93C47	93C47	8	DIP		3.5	Site 48/40		
93C55	93C55	8	DIP		4.2	Site 48/40		
93C55	93C55-SOIC	8	SO		4.2	PinSite	0302/0301	.150 SOIC
93C57	93C57	8	DIP		3.5	Site 48/40		
93C57	93C57-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
93C65	93C65-SOIC	8	SO		4.2	PinSite	0302/0301	.150 SOIC
93C67	93C67	8	DIP		3.5	Site 48/40		
93C67	93C67-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
Atmel Corporation								
18V8Z	ATV18V8Z	20	DIP		3.6	Site 48/40		
18V8Z	ATV18V8ZPLCC	20	PLCC		3.6	ChipSite		
18V8Z	ATV18V8ZPLCC	20	PLCC		3.6	PinSite	0201	
22LV10	22LV10	24	DIP		4.0	Site 48/40		
22LV10L	22LV10L	24	DIP		4.0	Site 48/40		
22V10	22V10	24	DIP		3.9	Site 48/40		
22V10	22V10-LCC	28	LCC		3.9	ChipSite		
22V10	22V10-LCC	28	LCC		3.9	PinSite	0202	
22V10	22V10-PLCC	28	PLCC		3.9	ChipSite		
22V10	22V10-PLCC	28	PLCC		3.9	PinSite	0201	
22V10B	22V10B	24	DIP		4.1	Site 48/40		
22V10B	22V10B-LCC	28	LCC		4.2	ChipSite		
22V10B	22V10B-LCC	28	LCC		4.2	PinSite	0202	
22V10B	22V10B-PLCC	28	PLCC		4.2	ChipSite		
22V10B	22V10B-PLCC	28	PLCC		4.2	PinSite	0201	
2500L	2500	40	DIP		2.6	Site 48/40		
2500L	2500-LCC	44	LCC		3.6	ChipSite		
2500L	2500-LCC	44	LCC		3.6	PinSite	0202	
2500L	2500-PLCC	44	PLCC		2.8	ChipSite		
2500L	2500-PLCC	44	PLCC		3.0	PinSite	0201	
2552	ATV2552-JLCC	68	JLCC		3.6	PinSite	0201	
2552	ATV2552PLCC*	68	PLCC		3.6	PinSite	0201	
2552	ATV2552PLCC*	68	PLCC	42,44	3.6	Site 48/40		
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
27C010	27C010	32	DIP		2.8	SetSite		
27C010	27C010	32	DIP		2.7	Site 48/40		
27C010	27C010-JLCC	32	JLCC		3.2	ChipSite		
27C010	27C010-JLCC	32	JLCC		3.2	PinSite	0201	
27C010	27C010-LCC	32	LCC	44	2.8	ChipSite		
27C010	27C010-LCC	32	LCC	44	3.0	PinSite	0202	
27C010	27C010-PLCC	32	PLCC		2.8	ChipSite		
27C010	27C010-PLCC	32	PLCC		3.0	PinSite	0201	
27C040	27C040	32	DIP		3.8	SetSite		
27C040	27C040	32	DIP		3.8	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Atmel Corporation (continued)								
27C040	27C040-LCC	32	LCC		4.2	PinSite	0202	
27C040	27C040-PLCC	32	PLCC		4.2	ChipSite		
27C040	27C040-PLCC	32	PLCC		4.2	PinSite	0201	
27C1024	27C1024	40	DIP		3.9	SetSite		
27C1024	27C1024	40	DIP		3.9	Site 48/40		
27C1024	27C1024-LCC	44	LCC	44	3.9	ChipSite		
27C1024	27C1024-LCC	44	LCC	44	3.9	PinSite	0202	
27C1024	27C1024-PLCC	44	PLCC		4.2	ChipSite		
27C1024	27C1024-PLCC	44	PLCC		4.2	PinSite	0201	
27C128	27C128	28	DIP		2.5	SetSite		
27C128	27C128	28	DIP		2.5	Site 48/40		
27C256	27C256	28	DIP		2.1	SetSite		
27C256	27C256	28	DIP		2.1	Site 48/40		
27C256	27C256-LCC	32	LCC	44	2.3	ChipSite		
27C256	27C256-LCC	32	LCC	44	3.0	PinSite	0202	
27C256	27C256-PLCC	32	PLCC		2.1	ChipSite		
27C256	27C256-PLCC	32	PLCC		3.0	PinSite	0201	
27C256R	27C256R	28	DIP		3.0	SetSite		
27C256R	27C256R	28	DIP		3.0	Site 48/40		
27C256R	27C256R-LCC	32	LCC	44	3.1	ChipSite		
27C256R	27C256R-LCC	32	LCC	44	3.1	PinSite	0202	
27C256R	27C256R-PLCC	32	PLCC		3.1	ChipSite		
27C256R	27C256R-PLCC	32	PLCC		3.1	PinSite	0201	
27C512	27C512	28	DIP		2.0	SetSite		
27C512	27C512	28	DIP		2.0	Site 48/40		
27C512	27C512-LCC	32	LCC	44	2.4	ChipSite		
27C512	27C512-LCC	32	LCC	44	3.0	PinSite	0202	
27C512	27C512-PLCC	32	PLCC		2.1	ChipSite		
27C512	27C512-PLCC	32	PLCC		3.0	PinSite	0201	
27C512R	27C512R	28	DIP		2.7	SetSite		
27C512R	27C512R	28	DIP		2.7	Site 48/40		
27C512R	27C512R-JLCC	32	JLCC		3.2	ChipSite		
27C512R	27C512R-JLCC	32	JLCC		3.2	PinSite	0201	
27C512R	27C512R-LCC	32	LCC	44	3.2	ChipSite		
27C512R	27C512R-LCC	32	LCC	44	3.2	PinSite	0202	
27C512R	27C512R-PLCC	32	PLCC		3.2	ChipSite		
27C512R	27C512R-PLCC	32	PLCC		3.2	PinSite	0201	
27C513	27C513	28	DIP		2.0	SetSite		
27C513	27C513	28	DIP		2.0	Site 48/40		
27C513R	27C513R	28	DIP		3.1	SetSite		
27C513R	27C513R	28	DIP		3.1	Site 48/40		
27HC1024	27HC1024	40	DIP		3.9	Site 48/40		
27HC1024	27HC1024-JLC	44	JLCC		4.2	ChipSite		
27HC1024	27HC1024-JLC	44	JLCC		4.2	PinSite	0201	
27HC1024	27HC1024-LCC	44	LCC		4.1	PinSite	0202	
27HC1024	27HC1024-PLC	44	PLCC		4.1	ChipSite		
27HC1024	27HC1024-PLC	44	PLCC		4.1	PinSite	0201	
27HC256	27HC256	28	DIP		2.2	SetSite		
27HC256	27HC256	28	DIP		2.2	Site 48/40		
27HC256	27HC256-LCC	32	LCC	44	2.3	ChipSite		
27HC256	27HC256-LCC	32	LCC	44	3.0	PinSite	0202	
27HC256	27HC256-PLCC	32	PLCC		2.2	ChipSite		
27HC256	27HC256-PLCC	32	PLCC		3.0	PinSite	0201	
27HC256R	27HC256R	28	DIP		4.1	SetSite		
27HC256R	27HC256R	28	DIP		4.1	Site 48/40		
27HC256R	27HC256R-PLC	32	PLCC		4.1	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Atmel Corporation (continued)								
27HC256R	27HC256R-PLC	32	PLCC		4.1	PinSite	0201	
27HC64	27HC64/L	28	DIP		2.1	SetSite		
27HC64	27HC64/L	28	DIP		2.1	Site 48/40		
27HC64	27HC64-LCC	32	LCC	44	2.4	ChipSite		
27HC64	27HC64-LCC	32	LCC	44	3.0	PinSite	0202	
27HC64	27HC64-PLCC	32	PLCC		2.3	ChipSite		
27HC64	27HC64-PLCC	32	PLCC		3.0	PinSite	0201	
27HC641	27HC641/L	24	DIP		2.0	SetSite		
27HC641	27HC641/L	24	DIP		2.0	Site 48/40		
27HC641	27HC641-LCC	28	LCC	44	2.3	ChipSite		
27HC641	27HC641-LCC	28	LCC	44	3.0	PinSite	0202	
27HC641	27HC641-PLCC	28	PLCC		2.3	ChipSite		
27HC641	27HC641-PLCC	28	PLCC		3.0	PinSite	0201	
27HC641R	27HC641R	24	DIP		3.4	Site 48/40		
27HC642	27HC642/L	24	DIP		2.8	SetSite		
27HC642	27HC642/L	24	DIP		2.0	Site 48/40		
27HC642R	27HC642R	24	DIP		3.5	Site 48/40		
27LV010	27LV010	32	DIP		3.9	SetSite		
27LV010	27LV010	32	DIP		3.9	Site 48/40		
27LV010	27LV010-LCC	32	LCC		4.2	ChipSite		
27LV010	27LV010-LCC	32	LCC		4.2	PinSite	0202	
27LV010	27LV010-PLCC	32	PLCC		4.2	ChipSite		
27LV010	27LV010-PLCC	32	PLCC		4.2	PinSite	0201	
27LV040	27LV040	32	DIP		3.9	SetSite		
27LV040	27LV040	32	DIP		3.9	Site 48/40		
27LV256R	27LV256R	28	DIP		3.9	SetSite		
27LV256R	27LV256R	28	DIP		3.9	Site 48/40		
27LV256R	27LV256R-LCC	32	LCC		4.2	ChipSite		
27LV256R	27LV256R-LCC	32	LCC		4.2	PinSite	0202	
27LV256R	27LV256R-PLC	32	PLCC		4.2	ChipSite		
27LV256R	27LV256R-PLC	32	PLCC		4.2	PinSite	0201	
27LV512R	27LV512R	28	DIP		3.9	SetSite		
27LV512R	27LV512R	28	DIP		3.9	Site 48/40		
27LV512R	27LV512R-LCC	32	LCC		4.2	ChipSite		
27LV512R	27LV512R-LCC	32	LCC		4.2	PinSite	0202	
27LV512R	27LV512R-PLC	32	PLCC		4.2	ChipSite		
27LV512R	27LV512R-PLC	32	PLCC		4.2	PinSite	0201	
28C010	28C010	32	DIP	36	4.0	Site 48/40		
28C010	28C010-LCC	44	LCC	36	4.0	ChipSite		
28C010	28C010-LCC	44	LCC	36	4.0	PinSite	0202	
28C04	28C04	24	DIP		2.5	Site 48/40		
28C1024	28C1024	40	DIP		3.5	Site 48/40		
28C16	28C16	24	DIP		2.8	SetSite		
28C16	28C16	24	DIP		2.1	Site 48/40		
28C16	28C16-PLCC	32	PLCC		2.1	ChipSite		
28C16	28C16-PLCC	32	PLCC		3.0	PinSite	0201	
28C17	28C17	28	DIP		2.6	Site 48/40		
28C256	28C256	28	DIP	36	3.0	SetSite		
28C256	28C256	28	DIP	36	2.4	Site 48/40		
28C256	28C256-PGA	28	PGA	36	3.6	PinSite	0402	
28C256	28C256-PLCC	32	PLCC	36	2.5	ChipSite		
28C256	28C256-PLCC	32	PLCC	36	3.0	PinSite	0201	
28C64	28C64	28	DIP		2.0	SetSite		
28C64	28C64	28	DIP		2.1	Site 48/40		
28C64	28C64-PLCC	32	PLCC		2.1	ChipSite		
28C64	28C64-PLCC	32	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Atmel Corporation (continued)								
28HC16	28HC16/N	24	DIP		2.8	SetSite		
28HC16	28HC16/N	24	DIP		2.3	Site 48/40		
28HC191	28HC191/L	24	DIP		2.8	SetSite		
28HC191	28HC191/L	24	DIP		2.5	Site 48/40		
28HC256	28HC256	28	DIP	36	2.5	Site 48/40		
28HC291	28HC291/L	24	DIP		2.5	Site 48/40		
28HC64	28HC64	28	DIP		2.5	Site 48/40		
28HC64	28HC64-PLCC	32	PLCC		2.5	ChipSite		
28HC64	28HC64-PLCC	32	PLCC		3.0	PinSite	0201	
28MC010	28MC010	32	DIP	147,36	4.0	SetSite		
28MC010	28MC010	32	DIP	147,36	4.0	Site 48/40		
28PC64	28PC64	28	DIP		3.3	SetSite		
28PC64	28PC64	28	DIP		2.5	Site 48/40		
28PC64	28PC64-PLCC	32	PLCC		2.5	ChipSite		
28PC64	28PC64-PLCC	32	PLCC		3.0	PinSite	0201	
29C010	29C010	32	DIP	203	3.6	Site 48/40		
29C010	29C010-PLCC	32	PLCC	203	3.9	ChipSite		
29C010	29C010-PLCC	32	PLCC	203	3.9	PinSite	0201	
29C256	29C256	28	DIP	36	3.0	Site 48/40		
29C256	29C256-PLCC	32	PLCC	36	3.6	ChipSite		
29C256	29C256-PLCC	32	PLCC	36	3.6	PinSite	0201	
29C257	29C257	32	DIP	114	4.1	Site 48/40		
29C257	29C257-PLCC	32	PLCC		4.1	ChipSite		
29C257	29C257-PLCC	32	PLCC		4.1	PinSite	0201	
29C512	29C512	32	DIP	203	4.0	Site 48/40		
29C512	29C512-PLCC	32	PLCC	203	4.0	ChipSite		
29C512	29C512-PLCC	32	PLCC	203	4.0	PinSite	0201	
29LV512	29LV512	32	DIP		4.2	Site 48/40		
29LV512	29LV512-PLCC	32	PLCC		4.2	ChipSite		
29LV512	29LV512-PLCC	32	PLCC		4.2	PinSite	0201	
32C16	32C16	40	DIP		3.9	SetSite		
32C16	32C16	40	DIP		3.9	Site 48/40		
415	ATV415	28	DIP		3.6	Site 48/40		
415	ATV415-PLCC	28	PLCC		3.6	ChipSite		
415	ATV415-PLCC	28	PLCC		3.6	PinSite	0201	
42VA12	ATV42VA12	24	DIP	33	3.6	Site 48/40		
42VA12	ATV42VA12-PL	28	PLCC	33	3.6	ChipSite		
42VA12	ATV42VA12-PL	28	PLCC	33	3.6	PinSite	0201	
5000	5000-PGA	68	PGA	148	3.8	PinSite	0402/0401	
5000	5000-PLCC	68	PLCC		3.6	PinSite	0201	
5100	5100-JLCC	68	JLCC		4.1	PinSite	0201	
5100	5100-LCC	68	LCC		4.1	PinSite	0202	
750	750	24	DIP		2.2	Site 48/40		
750	750-LCC	28	LCC		3.8	ChipSite		
750	750-LCC	28	LCC		3.8	PinSite	0202	
750	750-PLCC	28	PLCC		2.8	ChipSite		
750	750-PLCC	28	PLCC		3.0	PinSite	0201	
ATH3000	ATH3000-JLCC	68	JLCC		3.9	PinSite	0201	
ATH3000	ATH3000-PLCC	68	PLCC		3.9	PinSite	0201	
Catalyst Semiconductor								
22C10	22C10	18	DIP		3.5	Site 48		
22C12	22C12	18	DIP		3.5	Site 48		
24C02	24C02	8	DIP		3.8	Site 48/40		
24C04	24C04	8	DIP		3.8	Site 48/40		
24C08	24C08	8	DIP		4.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Catalyst Semiconductor (continued)								
24C16	24C16	8	DIP		3.8	Site 48/40		
27010	27010	32	DIP		2.8	SetSite		
27010	27010	32	DIP		2.5	Site 48/40		
27128A	27128A	28	DIP		2.2	SetSite		
27128A	27128A	28	DIP		2.2	Site 48/40		
27256	27256	28	DIP		2.2	SetSite		
27256	27256	28	DIP		2.2	Site 48/40		
27512	27512	28	DIP		2.2	SetSite		
27512	27512	28	DIP		2.2	Site 48/40		
2764A	2764A	28	DIP		2.2	SetSite		
2764A	2764A	28	DIP		2.2	Site 48/40		
27C210	27C210	40	DIP		2.8	SetSite		
27C210	27C210	40	DIP		2.5	Site 48/40		
27C210	27C210-PLCC	44	PLCC		3.8	ChipSite		
27C210	27C210-PLCC	44	PLCC		3.8	PinSite	0201	
27HC010	27HC010	32	DIP		3.5	SetSite		
27HC010	27HC010	32	DIP		3.5	Site 48/40		
27HC256	27HC256	28	DIP		2.8	SetSite		
27HC256	27HC256	28	DIP		2.5	Site 48/40		
28C16AP	28C16A	24	DIP		2.2	SetSite		
28C16AP	28C16A	24	DIP		2.2	Site 48/40		
28C17A	28C17A	28	DIP		2.5	SetSite		
28C17A	28C17A	28	DIP		2.5	Site 48/40		
28C256	28C256	28	DIP	36	3.2	Site 48/40		
28C256	28C256-PLCC	32	PLCC	36	3.8	ChipSite		
28C256	28C256-PLCC	32	PLCC	36	3.8	PinSite	0201	
28C64A	28C64A	28	DIP		3.2	SetSite		
28C64A	28C64A	28	DIP		3.2	Site 48/40		
28C64B	28C64B	28	DIP	36	3.9	Site 48/40		
28C64B	28C64B-PLCC	32	PLCC	36	4.2	ChipSite		
28C64B	28C64B-PLCC	32	PLCC	36	4.2	PinSite	0201	
28F010	28F010	32	DIP		4.2	Site 48/40		
28F010	28F010-PLCC	32	PLCC		4.2	ChipSite		
28F010	28F010-PLCC	32	PLCC		4.2	PinSite	0201	
33C104	33C104	8	DIP		2.8	Site 48/40		
35C102	35C102	8	DIP		2.8	Site 48/40		
35C104	35C104	8	DIP		2.8	Site 48/40		
35C704	35C704	8	DIP		3.6	Site 48/40		
59C11	59C11	8	DIP		2.8	Site 48/40		
93C46	93C46	8	DIP		3.6	Site 48/40		
Cypress Semiconductor, Inc.								
100E301/16P8	100E301/16P8	24	DIP		4.2	Site 48/40		
100E301/16P8	100E301-PLCC	28	PLCC	28	4.2	ChipSite		
100E301/16P8	100E301-PLCC	28	PLCC	28	4.2	PinSite	0201	
100E302/16P4	100E302/16P4	24	DIP	20	4.2	Site 48/40		
100E302/16P4	100E302-PLCC	28	PLCC	20,28	4.2	ChipSite		
100E302/16P4	100E302-PLCC	28	PLCC	20,28	4.2	PinSite	0201	
10E16P8	16P8-LCC	28	LCC	44	3.9	ChipSite		
10E16P8	16P8-LCC	28	LCC	44	3.9	PinSite	0202	
10E16P8	16P8-PLCC	28	PLCC		3.9	ChipSite		
10E16P8	16P8-PLCC	28	PLCC		3.9	PinSite	0201	
10E301	10E301-LCC	28	LCC	44	4.2	ChipSite		
10E301	10E301-LCC	28	LCC	44	4.2	PinSite	0202	
10E301	10E301-PLCC	28	PLCC		4.2	ChipSite		
10E301	10E301-PLCC	28	PLCC		4.2	PinSite	0201	
10E301/16P8	10E301/16P8	24	DIP		4.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Cypress Semiconductor, Inc. (continued)								
10E302/16P4	10E302/16P4	24	DIP	20	4.2	Site 48/40		
16L8	16L8	20	DIP		3.0	Site 48/40		
16L8	16L8-LCC	20	LCC	44	3.2	ChipSite		
16L8	16L8-LCC	20	LCC	44	3.2	PinSite	0202	
16L8-4	16L8-4-PLCC	28	PLCC	28	4.2	PinSite	0201	
16L8-5	16L8-5	20	DIP	28	4.2	Site 48/40		
16L8-5	16L8-5-PLCC	20	PLCC		4.2	ChipSite		
16L8-5	16L8-5-PLCC	20	PLCC		4.2	PinSite	0201	
16L8-7	16L8-7	20	DIP	28	4.2	Site 48/40		
16L8-7	16L8-7-PLCC	20	PLCC		4.2	ChipSite		
16L8-7	16L8-7-PLCC	20	PLCC		4.2	PinSite	0201	
16R4	16R4	20	DIP		3.0	Site 48/40		
16R4	16R4-LCC	20	LCC	44	3.5	ChipSite		
16R4	16R4-LCC	20	LCC	44	3.5	PinSite	0202	
16R4-4	16R4-4-PLCC	28	PLCC	28	4.2	PinSite	0201	
16R4-5	16R4-5	20	DIP	28	4.2	Site 48/40		
16R4-5	16R4-5-PLCC	20	PLCC		4.2	ChipSite		
16R4-5	16R4-5-PLCC	20	PLCC		4.2	PinSite	0201	
16R4-7	16R4-7	20	DIP	28	4.2	Site 48/40		
16R4-7	16R4-7-PLCC	20	PLCC		4.2	ChipSite		
16R4-7	16R4-7-PLCC	20	PLCC		4.2	PinSite	0201	
16R6	16R6	20	DIP		3.0	Site 48/40		
16R6	16R6-LCC	20	LCC	44	3.5	ChipSite		
16R6	16R6-LCC	20	LCC	44	3.5	PinSite	0202	
16R6-4	16R6-4-PLCC	28	PLCC	28	4.2	PinSite	0201	
16R6-5	16R6-5	20	DIP	28	4.2	Site 48/40		
16R6-5	16R6-5-PLCC	20	PLCC		4.2	ChipSite		
16R6-5	16R6-5-PLCC	20	PLCC		4.2	PinSite	0201	
16R6-7	16R6-7	20	DIP	28	4.2	Site 48/40		
16R6-7	16R6-7-PLCC	20	PLCC		4.2	ChipSite		
16R6-7	16R6-7-PLCC	20	PLCC		4.2	PinSite	0201	
16R8	16R8	20	DIP		3.0	Site 48/40		
16R8	16R8-LCC	20	LCC	44	3.5	ChipSite		
16R8	16R8-LCC	20	LCC	44	3.5	PinSite	0202	
16R8-4	16R8-4-PLCC	28	PLCC	28	4.2	PinSite	0201	
16R8-5	16R8-5	20	DIP	28	4.2	Site 48/40		
16R8-5	16R8-5-PLCC	20	PLCC		4.2	ChipSite		
16R8-5	16R8-5-PLCC	20	PLCC		4.2	PinSite	0201	
16R8-7	16R8-7	20	DIP	28	4.2	Site 48/40		
16R8-7	16R8-7-PLCC	20	PLCC		4.2	ChipSite		
16R8-7	16R8-7-PLCC	20	PLCC		4.2	PinSite	0201	
18G8	18G8	20	DIP		3.1	Site 48/40		
20G10	20G10A-PLCC	28	PLCC		2.6	ChipSite		
20G10	20G10A-PLCC	28	PLCC		3.0	PinSite	0201	
20G10/A	20G10A	24	DIP		3.0	Site 48/40		
20G10B	20G10B	24	DIP		3.6	Site 48/40		
20G10B	20G10B-PLCC	28	PLCC		3.6	ChipSite		
20G10B	20G10B-PLCC	28	PLCC		3.6	PinSite	0201	
20G10C	20G10C	24	DIP	28	3.8	Site 48/40		
20G10G	20G10G	24	DIP	28	3.8	Site 48/40		
20RA10	20RA10	24	DIP		3.6	Site 48/40		
20RA10	20RA10-NL	28	PLCC		3.6	ChipSite		
20RA10	20RA10-NL	28	PLCC		3.6	PinSite	0201	
22V10/A	22V10A	24	DIP		3.0	Site 48/40		
22V10/A	22V10A-LCC	28	LCC	44	3.0	ChipSite		
22V10/A	22V10A-LCC	28	LCC	44	3.0	PinSite	0202	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Cypress Semiconductor, Inc. (continued)								
22V10/A	22V10A-PLCC	28	PLCC		3.0	ChipSite		
22V10/A	22V10A-PLCC	28	PLCC		3.0	PinSite	0201	
22V10B	22V10B	24	DIP		3.7	Site 48/40		
22V10B	22V10B-JLCC	28	JLCC		3.6	ChipSite		
22V10B	22V10B-JLCC	28	JLCC		3.6	PinSite	0201	
22V10B	22V10B-LCC	28	LCC		4.2	ChipSite		
22V10B	22V10B-LCC	28	LCC		4.2	PinSite	0202	
22V10B	22V10B-PLCC	28	PLCC		3.6	ChipSite		
22V10B	22V10B-PLCC	28	PLCC		3.6	PinSite	0201	
22V10C	22V10C	24	DIP	28	3.2	Site 48/40		
22V10C	22V10C-PLCC	28	PLCC	28	3.2	ChipSite		
22V10C	22V10C-PLCC	28	PLCC	28	3.2	PinSite	0201	
22V10D	22V10D	24	DIP		3.9	Site 48/40		
22V10D	22V10D-PLCC	28	PLCC		4.0	ChipSite		
22V10D	22V10D-PLCC	28	PLCC		4.0	PinSite	0201	
22V10G	22V10G	24	DIP	28	4.2	Site 48/40		
22V10G	22V10G-PLCC	28	PLCC	28	4.2	ChipSite		
22V10G	22V10G-PLCC	28	PLCC	28	4.2	PinSite	0201	
22VP10C	22VP10C	24	DIP	28	3.2	Site 48/40		
22VP10C	22VP10C-PLCC	28	PLCC	28	3.2	ChipSite		
22VP10C	22VP10C-PLCC	28	PLCC	28	3.2	PinSite	0201	
22VP10G	22VP10G	24	DIP	28	4.2	Site 48/40		
22VP10G	22VP10G-PLCC	28	PLCC	28	4.2	ChipSite		
22VP10G	22VP10G-PLCC	28	PLCC	28	4.2	PinSite	0201	
610	610	24	DIP	28	4.1	Site 48/40		
610	610-PLCC	28	PLCC	28	4.2	ChipSite		
610	610-PLCC	28	PLCC	28	4.2	PinSite	0201	
7B333B	7B333B	28	DIP	28	4.2	Site 48		
7B333B	7B333B-LCC	28	LCC	28	4.2	PinSite	0202	
7B333B	7B333B-PLCC	28	PLCC	28	4.2	ChipSite		
7B333B	7B333B-PLCC	28	PLCC	28	4.2	PinSite	0201	
7B336	7B336	28	DIP		3.8	Site 48		
7B336	7B336-PLCC	28	PLCC		3.8	PinSite	0201	
7B337	7B337	28	DIP		3.8	Site 48		
7B338	7B338	28	DIP		3.5	Site 48		
7B338	7B338-PLCC	28	PLCC		3.6	PinSite	0201	
7B339	7B339	28	DIP		3.5	Site 48		
7B339	7B339-PLCC	28	PLCC		3.6	PinSite	0201	
7C225	7C225	24	DIP	45	2.2	Site 48/40		
7C225	7C225-LCC	28	LCC	44,45	3.1	ChipSite		
7C225	7C225-LCC	28	LCC	44,45	3.1	PinSite	0202	
7C235	7C235	24	DIP	1,45	2.2	Site 48/40		
7C235	7C235-LCC	28	LCC	1,44,45	2.8	ChipSite		
7C235	7C235-LCC	28	LCC	1,44,45	3.0	PinSite	0202	
7C235	7C235-PLCC	28	PLCC	1,45	3.1	ChipSite		
7C235	7C235-PLCC	28	PLCC	1,45	3.1	PinSite	0201	
7C245	7C245	24	DIP	3,45	2.2	Site 48/40		
7C245	7C245-SOIC	24	SO	3,45	3.1	ChipSite		
7C245	7C245-SOIC	24	SO	3,45	3.1	PinSite	0302/0301	.300 SOIC
7C245	7C245-LCC	28	LCC	3,44,45	3.1	ChipSite		
7C245	7C245-LCC	28	LCC	3,44,45	3.1	PinSite	0202	
7C245A	7C245A	24	DIP	3	2.3	Site 48/40		
7C245A	7C245A-LCC	28	LCC	3,44	2.8	ChipSite		
7C245A	7C245A-LCC	28	LCC	3,44	3.0	PinSite	0202	
7C245A	7C245A-PLCC	28	PLCC	3,44	4.2	ChipSite		
7C245A	7C245A-PLCC	28	PLCC	3,44	4.2	PinSite	0202	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Cypress Semiconductor, Inc. (continued)								
7C251	7C251	28	DIP		4.1	SetSite		
7C251	7C251	28	DIP		1.6	Site 48/40		
7C251	7C251-LCC	32	LCC	44	3.1	ChipSite		
7C251	7C251-LCC	32	LCC	44	3.1	PinSite	0202	
7C253	7C253	28	DIP		1.6	Site 48/40		
7C254	7C254	28	DIP		1.6	Site 48/40		
7C258	7C258	28	DIP	203,108	4.1	Site 48		
7C258	7C258-JLCC	28	JLCC	203,108	4.1	PinSite	0201	
7C258	7C258-LCC	28	LCC	203,108	4.1	PinSite	0202	
7C258	7C258-PLCC	28	PLCC	203,108	4.1	PinSite	0201	
7C259	7C259-PLCC	44	PLCC	203	4.2	PinSite	0201	
7C261	7C261	24	DIP		4.0	SetSite		
7C261	7C261	24	DIP		4.0	Site 48/40		
7C261	7C261-LCC	28	LCC	44	4.0	ChipSite		
7C261	7C261-LCC	28	LCC	44	4.0	PinSite	0202	
7C263	7C263	24	DIP		4.0	SetSite		
7C263	7C263	24	DIP		4.0	Site 48/40		
7C263	7C263-LCC	28	LCC	44	4.0	ChipSite		
7C263	7C263-LCC	28	LCC	44	4.0	PinSite	0202	
7C263	7C263-PLCC	28	PLCC		4.0	ChipSite		
7C263	7C263-PLCC	28	PLCC		4.0	PinSite	0201	
7C264	7C264	24	DIP		4.0	Site 48/40		
7C265	7C265	28	DIP		2.8	Site 48/40		
7C266	7C266	28	DIP		3.9	Site 48/40		
7C266	7C266-PLCC	32	PLCC		4.2	ChipSite		
7C266	7C266-PLCC	32	PLCC		4.2	PinSite	0201	
7C268	7C268	32	DIP	3	2.1	Site 48/40		
7C269	7C269	28	DIP	4	2.2	Site 48/40		
7C269	7C269-LCC	28	LCC	44	3.1	ChipSite		
7C269	7C269-LCC	28	LCC	44	3.1	PinSite	0202	
7C270	7C270-LCC	44	LCC	203	4.2	ChipSite		
7C270	7C270-LCC	44	LCC	203	4.2	PinSite	0202	
7C270	7C270-PLCC	44	PLCC	203	4.2	ChipSite		
7C270	7C270-PLCC	44	PLCC	203	4.2	PinSite	0201	
7C271	7C271	28	DIP		3.0	Site 48/40		
7C271	7C271-LCC	32	LCC	44	3.1	ChipSite		
7C271	7C271-LCC	32	LCC	44	3.1	PinSite	0202	
7C274	7C274	28	DIP		3.0	Site 48/40		
7C276	7C276-LCC	44	LCC	203	4.2	ChipSite		
7C276	7C276-LCC	44	LCC	203	4.2	PinSite	0202	
7C276	7C276-PLCC	44	PLCC	203	4.2	ChipSite		
7C276	7C276-PLCC	44	PLCC	203	4.2	PinSite	0201	
7C277	7C277	28	DIP	56	3.2	Site 48/40		
7C279	7C279	28	DIP	56	3.1	Site 48/40		
7C281	7C281	24	DIP		2.2	Site 48/40		
7C282	7C282	24	DIP		2.2	Site 48/40		
7C285	7C285	28	DIP		3.3	Site 48/40		
7C285	7C285-LCC	32	LCC	44	3.4	PinSite	0202	
7C286	7C286	28	DIP		3.3	Site 48/40		
7C287	7C287	28	DIP	95	3.3	Site 48/40		
7C287	7C287-LCC	32	LCC	95	3.6	PinSite	0202	
7C289	7C289	32	DIP	95	3.3	Site 48		
7C291	7C291	24	DIP		2.2	Site 48/40		
7C291	7C291-LCC	28	LCC	44	3.1	ChipSite		
7C291	7C291-LCC	28	LCC	44	3.1	PinSite	0202	
7C291	7C291-PLCC	28	PLCC		2.2	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Microchip Technology Inc. (continued)								
28C64/A	28C64/A-SOIC	28	SO		3.4	PinSite	0302/0301	.300 SOIC
28C64/A	28C64/A-LCC	32	LCC	44	3.2	ChipSite		
28C64/A	28C64/A-LCC	32	LCC	44	3.2	PinSite	0202	
28C64/A	28C64/A-PLCC	32	PLCC		2.3	ChipSite		
28C64/A	28C64/A-PLCC	32	PLCC		3.0	PinSite	0201	
5911	5911	8	DIP		3.6	Site 48/40		
59C11	59C11	8	DIP		3.2	Site 48/40		
59C11-SN	59C11-SN	8	SO		3.9	PinSite	0302/0301	.150 SOIC
8582	8582	8	DIP		3.6	Site 48/40		
85C72	85C72	8	DIP		3.3	Site 48/40		
85C82	85C82	8	DIP		3.3	Site 48/40		
85C92	85C92	8	DIP		3.6	Site 48/40		
93C06	93C06	8	DIP		3.2	Site 48/40		
93C46	93C46	8	DIP		3.2	Site 48/40		
Mikroelektronik								
2716	2716	24	DIP		3.4	Site 48/40		
2732	2732	24	DIP		3.4	Site 48/40		
Mitsubishi Electronics of America								
2708	2708	24	DIP		2.0	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		2.0	Site 48/40		
2716	2716	24	DIP		2.2	SetSite		
2716	2716	24	DIP		2.2	Site 48/40		
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
2732	2732	24	DIP		3.8	SetSite		
2732	2732	24	DIP		3.8	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
27401A	27401A	32	DIP		3.8	Site 48/40		
27401A	27401A-SOIC	32	SO		4.1	PinSite	0302	.450 SOIC
27512	27512/P	28	DIP		2.0	SetSite		
27512	27512/P	28	DIP		2.0	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		
27C100	27C100	32	DIP		2.8	SetSite		
27C100	27C100	32	DIP		2.8	Site 48/40		
27C100	27C100-JLCC	32	JLCC		2.8	ChipSite		
27C100	27C100-JLCC	32	JLCC		3.0	PinSite	0201	
27C100	27C100-PLCC	32	PLCC		2.8	ChipSite		
27C100	27C100-PLCC	32	PLCC		3.0	PinSite	0201	
27C101	27C101	32	DIP		2.8	SetSite		
27C101	27C101	32	DIP		2.8	Site 48/40		
27C101	27C101-PLCC	32	PLCC		2.8	ChipSite		
27C101	27C101-PLCC	32	PLCC		3.0	PinSite	0201	
27C101	27C101-SOIC	32	SO		4.1	PinSite	0302	.450 SOIC
27C102	27C102	40	DIP		2.8	SetSite		
27C102	27C102	40	DIP		2.8	Site 48/40		
27C102	27C102-JLCC	44	JLCC		3.3	ChipSite		
27C102	27C102-JLCC	44	JLCC		3.3	PinSite	0201	
27C102	27C102-PLCC	44	PLCC		2.8	ChipSite		
27C102	27C102-PLCC	44	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Mitsubishi Electronics of America (continued)								
27C128	27C128	28	DIP		2.0	SetSite		
27C128	27C128	28	DIP		2.0	Site 48/40		
27C201	27C201	32	DIP		2.8	SetSite		
27C201	27C201	32	DIP		2.8	Site 48/40		
27C201	27C201-JLCC	32	JLCC		3.3	ChipSite		
27C201	27C201-JLCC	32	JLCC		3.3	PinSite	0201	
27C201	27C201-SOIC	32	SO		4.1	PinSite	0302	.450 SOIC
27C202	27C202	40	DIP		2.8	SetSite		
27C202	27C202	40	DIP		2.8	Site 48/40		
27C202	27C202-SOIC	40	SO		4.1	PinSite	0302	.450 SOIC
27C202	27C202-JLCC	44	JLCC		3.6	ChipSite		
27C202	27C202-JLCC	44	JLCC		3.6	PinSite	0201	
27C202	27C202-PLCC	44	PLCC		3.6	ChipSite		
27C202	27C202-PLCC	44	PLCC		3.6	PinSite	0201	
27C256	27C256	28	DIP		2.1	SetSite		
27C256	27C256	28	DIP		2.1	Site 48/40		
27C256A	27C256A	28	DIP		2.8	SetSite		
27C256A	27C256A	28	DIP		2.8	Site 48/40		
27C256A	27C256A-SOIC	28	SO		4.1	PinSite	0302/0301	.350 SOIC
27C401	27C401	32	DIP		3.8	SetSite		
27C401	27C401	32	DIP		3.1	Site 48/40		
27C402	27C402	40	DIP		3.6	SetSite		
27C402	27C402	40	DIP		3.1	Site 48/40		
27C512A	27C512A	28	DIP		2.8	SetSite		
27C512A	27C512A	28	DIP		2.4	Site 48/40		
27C512A	27C512A-SOIC	28	SO		4.1	PinSite	0302/0301	.350 SOIC
28C64A	28C64A	28	DIP		3.5	Site 48/40		
28C64A	28C64A-SOIC	28	SO		4.1	PinSite	0302/0301	.350 SOIC
28F101	28F101	32	DIP		4.2	Site 48/40		
28F101	28F101-PLCC	32	PLCC		4.2	ChipSite		
28F101	28F101-PLCC	32	PLCC		4.2	PinSite	0201	
28F101	28F101-SOIC	32	SO		4.2	PinSite	0302	.450 SOIC
28F102	28F102	40	DIP		4.0	Site 48/40		
3128-M6	3128-M6*	60	CARD	92	3.4	Site 48/40		
3128-M7	3128-M7*	50	CARD	93	3.4	Site 48/40		
31M0-M6	31M0-M6*	60	CARD	92	3.4	Site 48/40		
31M0-M7	31M0-M7*	50	CARD	93	3.4	Site 48/40		
3256-M6	3256-M6*	60	CARD	92	3.4	Site 48/40		
3256-M7	3256-M7*	50	CARD	93	3.4	Site 48/40		
32M0-M6	32M0-M6*	60	CARD	92	3.4	Site 48/40		
32M0-M7	32M0-M7*	50	CARD	93	3.4	Site 48/40		
3512-M6	3512-M6*	60	CARD	92	3.4	Site 48/40		
3512-M7	3512-M7*	50	CARD	93	3.4	Site 48/40		
37410E6FP	37410E6-QFP*	80	QFP	71	3.2	Site 48/40		
37450E4	37450E4SDIP*	64	SDIP	110	3.6	Site 48/40		
37450E4	37450E4-QFP*	80	QFP	111	3.6	Site 48/40		
37450E8	37450E8SDIP*	64	SDIP	75	3.2	Site 48/40		
37450E8	37450E8-QFP*	80	QFP	74	3.2	Site 48/40		
37470E8	37470E8SDIP*	32	SDIP	72	3.2	Site 48/40		
37471E8	37471E8SDIP*	42	SDIP	72	3.2	Site 48/40		
37471E8	37471E8-QFP*	56	QFP	73	3.2	Site 48/40		
37700E2	37700E2-LCC*	80	LCC	65	3.2	Site 48/40		
37700E4	37700E4-LCC*	80	LCC	66	3.2	Site 48/40		
37701E2	37701E2SDIP*	64	SDIP	112	3.4	Site 48/40		
37701E4	37701E4SDIP*	64	SDIP	113	3.4	Site 48/40		
37702E2	37702E2-LCC*	80	LCC	65	3.8	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Mitsubishi Electronics of America (continued)								
37702E2	37702E2-QFP*	80	QFP	186	4.0	Site 48/40		
37702E4	37702E4-LCC*	80	LCC	213	4.2	Site 48/40		
37702E4	37702E4-QFP*	80	QFP	211	4.2	Site 48/40		
37702E6	37702E6-LCC*	80	LCC	214	4.2	Site 48/40		
37702E6	37702E6-QFP*	80	QFP	212	4.2	Site 48/40		
37703E2	37703E2SDIP*	64	SDIP	112	4.0	Site 48/40		
37703E4	37703E4SDIP*	64	SDIP	113	4.0	Site 48/40		
37705E2	37705E2SDIP*	64	SDIP	112	4.0	Site 48/40		
37796E4	37796E4PLCC*	84	PLCC	76	3.2	Site 48/40		
4128-F3	4128-F3*	60	CARD	92	3.4	Site 48/40		
4128-F4	4128-F4*	50	CARD	93	3.4	Site 48/40		
41M0-F1	41M0-F1*	60	CARD	92	3.4	Site 48/40		
41M0-F2	41M0-F2*	50	CARD	93	3.4	Site 48/40		
41M1-F1	41M1-F1*	60	CARD	92	3.4	Site 48/40		
41M1-F2	41M1-F2*	50	CARD	93	3.4	Site 48/40		
4256-F3	4256-F3*	60	CARD	92	3.4	Site 48/40		
4256-F4	4256-F4*	50	CARD	93	3.4	Site 48/40		
4257-F3	4257-F3*	60	CARD	92	3.4	Site 48/40		
4257-F4	4257-F4*	50	CARD	93	3.4	Site 48/40		
42M0-F1	42M0-F1*	60	CARD	92	3.4	Site 48/40		
42M0-F2	42M0-F2*	50	CARD	93	3.4	Site 48/40		
42M1-F1	42M1-F1*	60	CARD	92	3.4	Site 48/40		
42M1-F2	42M1-F2*	50	CARD	93	3.4	Site 48/40		
4512-F3	4512-F3*	60	CARD	92	3.4	Site 48/40		
4512-F4	4512-F4*	50	CARD	93	3.4	Site 48/40		
4513-F3	4513-F3*	60	CARD	92	3.4	Site 48/40		
4513-F4	4513-F4*	50	CARD	93	3.4	Site 48/40		
50727E	50727E-SDIP*	42	SDIP	77,109	3.6	Site 48/40		
50727E	50727E-SOIC*	42	SO	77,109	3.6	Site 48/40		
50746E	50746E-SDIP*	64	SDIP	67	3.6	Site 48/40		
50746E	50746E-QFP*	72	QFP	68	3.6	Site 48/40		
50747E	50747E-SDIP*	64	SDIP	69	3.6	Site 48/40		
50747E	50747E-QFP*	72	QFP	70	3.6	Site 48/40		
50927E	50927E-SDIP*	30	SDIP	78,109	3.2	Site 48/40		
50927E	50927E-SOIC*	36	SO	78,109	3.6	Site 48/40		
54700A	54700A	16	DIP		2.0	Site 48/40		
54701A	54701A	16	DIP		2.0	Site 48/40		
54730A	54730A	16	DIP		2.0	Site 48/40		
54731A	54731A	16	DIP		2.0	Site 48/40		
54740A	54740A	18	DIP		2.0	Site 48/40		
54741A	54741A	18	DIP		2.0	Site 48/40		
808A-F1	808A-F1*	32	CARD	92	3.4	Site 48/40		
8128-F1	8128A-F1*	60	CARD	92	3.4	Site 48/40		
816A-F1	816A-F1*	32	CARD	92	3.4	Site 48/40		
8192-F1	8192-F1*	60	CARD	92,114	3.4	Site 48/40		
81M1-G1	81M1-G1*	68	CARD	156	4.0	Site 48/40		
832A-F1	832A-F1*	32	CARD	92	3.4	Site 48/40		
8513-G1	8513_G1*	68	CARD	156	4.0	Site 48/40		
864A-F1	864A-F1*	32	CARD	92	3.4	Site 48/40		
M6M72561J	72561-PLCC	68	PLCC	215	4.2	PinSite	0201	
Mitsubishi Plastics								
0016EEBOC20	0016EEB0C20*	32	CARD	90	3.2	Site 48/40		
0016EEBSC20	0016EEBSC20*	32	CARD	90	3.3	Site 48/40		
0064EEBHN30	0064EEBHN30*	32	CARD	87	3.2	Site 48/40		
0064EEPHC25	0064EEPHC25*	32	CARD	87	3.3	Site 48/40		
0064EP10N15	0064EP10N15*	32	CARD	87	3.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Mitsubishi Plastics (continued)								
0128EEBH030	0128EEBH030*	32	CARD	87	3.2	Site 48/40		
0128EEPHD25	0128EEPHD25*	32	CARD	87	3.2	Site 48/40		
0256EEPHC21	0256EEPHC21*	32	CARD	102	3.3	Site 48/40		
0256EP1FC20	0256EP1FC20*	32	CARD	87	3.2	Site 48/40		
0512EEPHD21	0512EEPHD21*	32	CARD	102	3.3	Site 48/40		
0512EP1FC22	0512EP1FC22*	32	CARD	88	3.2	Site 48/40		
0512EP1TC20	0512EP1TC20*	32	CARD	88	4.2	Site 48		
1024EP1HC25	1024EP1HC25*	32	CARD	89	3.2	Site 48/40		
Motorola Inc.								
10139	10139	16	DIP	19	1.2	Site 48/40		
10149AL10	10149AL10	16	DIP		2.7	Site 48/40		
10149L10	10149L10	16	DIP	19	2.7	Site 48/40		
10149L25	10149L25	16	DIP	19	3.2	Site 48/40		
2532	2532	24	DIP		2.0	SetSite		
2532	2532	24	DIP		2.0	Site 48/40		
2708	2708	24	DIP		2.0	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
2716	2716	24	DIP		2.0	SetSite		
2716	2716	24	DIP		2.0	Site 48/40		
2816	2816	24	DIP		2.0	SetSite		
2816	2816	24	DIP		2.0	Site 48/40		
68701	68701	40	DIP	7,21	1.1	Site 48/40		
68701U4	68701U4	40	DIP	7,21	1.2	Site 48/40		
68705P3	68705P3	28	DIP	8,21	2.4	Site 48/40		
68705P5	68705P5	28	DIP	8,21,25	2.4	Site 48/40		
68705R3	68705R3	40	DIP	8,21	2.4	Site 48/40		
68705R5	68705R5	40	DIP	6,8,21	2.4	Site 48/40		
68705S3	68705S3-1TJ6	28	DIP	6,8,21	3.5	Site 48/40		
68705S3-A20T	68705S3-A20T	28	DIP	6,21,131	4.2	Site 48/40		
68705U3	68705U3	40	DIP	8,21	2.4	Site 48/40		
68705U5	68705U5	40	DIP	6,8,21	2.4	Site 48/40		
68708	68708	24	DIP		2.0	Site 48/40		
68764	68764	24	DIP		2.0	SetSite		
68764	68764	24	DIP		1.7	Site 48/40		
68766	68766	24	DIP		2.0	SetSite		
68766	68766	24	DIP		1.7	Site 48/40		
68HC11A1	68HC11A1	48	DIP	140,173,178	3.4	Site 48		
68HC11A1-FN	68HC11A1-FN	52	PLCC	140,173,178	2.0	ChipSite		
68HC11A1-FN	68HC11A1-FN	52	PLCC	140,173,178	3.0	PinSite	0201	
68HC11A8-FN	68HC11A8-FN	52	PLCC	10,140,173,178	2.0	ChipSite		
68HC11A8-FN	68HC11A8-FN	52	PLCC	10,140,173,178	3.0	PinSite	0201	
68HC11F1-FN	68HC11F1-FN	68	PLCC	130,172,173,174	3.9	PinSite	0201	
68HC11K4	68HC11K4	84	PLCC	130,171,173,178	3.9	PinSite	0201	
68HC705B5	68HC705B5-FN	52	PLCC	21,131,140	3.5	PinSite	0201	
68HC705C8	68HC705C8	40	DIP	2,21,35	2.6	Site 48/40		
68HC705C8-FN	68HC705C8-FN	44	PLCC	2,21,35	2.6	ChipSite		
68HC705C8-FN	68HC705C8-FN	44	PLCC	2,21,35	3.0	PinSite	0201	
68HC705C9	68HC705C9	40	DIP	140	3.7	Site 48/40		
68HC705C9	68HC705C9-FN	44	PLCC	21,140	3.7	ChipSite		
68HC705C9	68HC705C9-FN	44	PLCC	21,140	3.7	PinSite	0201	
68HC705D9	68HC705D9	40	DIP	140	3.7	Site 48/40		
68HC705D9	68HC705D9-FN	44	PLCC	21,140	3.7	ChipSite		
68HC705D9	68HC705D9-FN	44	PLCC	21,140	3.7	PinSite	0201	
68HC705E1	68HC705E1	28	DIP	21,130,140,176	3.9	Site 48		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Motorola Inc. (continued)								
68HC705J2	68HC705J2	20	DIP	21,140,143	3.6	Site 48/40		
68HC705J2	68HC705J2DW	20	SO	21,140,131,143	4.1	ChipSite		
68HC705J2	68HC705J2DW	20	SO	21,140,131,143	4.1	PinSite	0302/0301	.300 SOIC
68HC705K1	68HC705K1	16	DIP	21,131,204	4.1	Site 48/40		
68HC705K1	68HC705K1DW	16	SO	21,131,204	4.1	PinSite	0302/0301	.300 SOIC
68HC705P9	68HC705P9	28	DIP	21,139,140	3.7	Site 48/40		
68HC705P9	68HC705P9DW	28	SO	139,140	3.7	ChipSite		
68HC705P9	68HC705P9DW	28	SO	139,140	3.7	PinSite	0302/0301	.300 SOIC
68HC705P9(0D54E)	68HC705P9*	28	DIP	21,139,140	3.7	Site 48/40		
68HC705P9(0D54E)	68HC705P9DW*	28	SO	139,140	3.7	ChipSite		
68HC705P9(0D54E)	68HC705P9DW*	28	SO	139,140	3.7	PinSite	0302/0301	.300 SOIC
68HC711D3	68HC711D3	40	DIP		3.5	Site 48/40		
68HC711D3	68HC711D3-FN	44	PLCC		3.5	PinSite	0201	
68HC711E9	68HC711E9-FN	52	PLCC	21,131,132	3.6	ChipSite		
68HC711E9	68HC711E9-FN	52	PLCC	21,131,132	3.6	PinSite	0201	
68HC711K4	68HC711K4-JL	84	JLCC	21,131,173,175	3.9	PinSite	0201	
68HC805B6-FN	68HC805B6-FN	52	PLCC	35	3.1	PinSite	0201	
68HC805C4	68HC805C4	40	DIP	35	2.6	Site 48/40		
68HC805C4-FN	68HC805C4-FN	44	PLCC	35	2.6	ChipSite		
68HC805C4-FN	68HC805C4-FN	44	PLCC	35	3.0	PinSite	0201	
68HC811A2	68HC811A2	48	DIP	11	2.2	Site 48		
68HC811A2-FN	68HC811A2-FN	52	PLCC	11	2.0	ChipSite		
68HC811A2-FN	68HC811A2-FN	52	PLCC	11	3.0	PinSite	0201	
68HC811E2	68HC811E2	48	DIP	11	3.6	Site 48		
68HC811E2-FN	68HC811E2-FN	52	PLCC	11	2.7	ChipSite		
68HC811E2-FN	68HC811E2-FN	52	PLCC	11	3.0	PinSite	0201	
76161	76161	24	DIP		2.2	Site 48/40		
7620	7620	16	DIP		2.2	Site 48/40		
7621	7621	16	DIP		2.2	Site 48/40		
7640	7640	24	DIP		2.2	Site 48/40		
7641	7641	24	DIP		2.2	Site 48/40		
7642	7642	18	DIP		2.2	Site 48/40		
7643	7643	18	DIP		2.2	Site 48/40		
7680	7680	24	DIP		2.2	Site 48/40		
7681	7681	24	DIP		2.2	Site 48/40		
7684	7684	18	DIP		2.2	Site 48/40		
7685	7685	18	DIP		2.2	Site 48/40		
TMS2716	TMS2716	24	DIP		2.5	SetSite		
TMS2716	TMS2716	24	DIP		2.5	Site 48/40		
NEC Electronics Corp.								
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		2.0	Site 48/40		
2716	2716	24	DIP		3.2	SetSite		
2716	2716	24	DIP		3.2	Site 48/40		
27256	27256	28	DIP		2.0	SetSite		
27256	27256	28	DIP		2.0	Site 48/40		
27256A	27256A	28	DIP		2.4	SetSite		
27256A	27256A	28	DIP		2.4	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
27512	27512	28	DIP		2.0	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
NEC Electronics Corp. (continued)								
27C1000	27C1000	32	DIP		2.3	SetSite		
27C1000	27C1000	32	DIP		2.3	Site 48/40		
27C1000A	27C1000A	32	DIP		2.6	SetSite		
27C1000A	27C1000A	32	DIP		2.6	Site 48/40		
27C1001	27C1001	32	DIP		2.2	SetSite		
27C1001	27C1001	32	DIP		2.2	Site 48/40		
27C1001A	27C1001A	32	DIP		2.6	SetSite		
27C1001A	27C1001A	32	DIP		2.6	Site 48/40		
27C1024	27C1024	40	DIP		2.4	SetSite		
27C1024	27C1024	40	DIP		2.4	Site 48/40		
27C1024A	27C1024A	40	DIP		2.6	Site 48/40		
27C2001	27C2001	32	DIP		2.3	SetSite		
27C2001	27C2001	32	DIP		2.3	Site 48/40		
27C256	27C256	28	DIP		2.0	SetSite		
27C256	27C256	28	DIP		2.0	Site 48/40		
27C256	27C256-LCC	28	LCC	44	2.1	ChipSite		
27C256	27C256-LCC	28	LCC	44	3.0	PinSite	0202	
27C256A	27C256A	28	DIP		3.1	SetSite		
27C256A	27C256A	28	DIP		3.1	Site 48/40		
27C256A	27C256A-SOIC	28	SO		4.0	PinSite	0302/0301	.350 SOIC
27C256A	27C256A-LCC	32	LCC	44	2.3	ChipSite		
27C256A	27C256A-LCC	32	LCC	44	3.0	PinSite	0202	
27C4000	27C4000	40	DIP		3.4	Site 48/40		
27C4000	27C4000-SOIC	40	SO		4.1	PinSite	0302	.450 SOIC
27C4001	27C4001	32	DIP		3.6	SetSite		
27C4001	27C4001	32	DIP		2.4	Site 48/40		
27C4001	27C4001-SOIC	32	SO		4.1	PinSite	0302	.450 SOIC
27C4096	27C4096	40	DIP		3.0	Site 48/40		
27C4096	27C4096-SOIC	40	SO		4.1	PinSite	0302	.450 SOIC
27C512	27C512	28	DIP		2.4	SetSite		
27C512	27C512	28	DIP		2.4	Site 48/40		
27C512	27C512-SOIC	28	SO		4.0	PinSite	0302/0301	.350 SOIC
27C512	27C512-LCC	32	LCC	44	4.0	PinSite	0202	
27C64	27C64	28	DIP		2.8	SetSite		
27C64	27C64	28	DIP		2.0	Site 48/40		
27C8000	27C8000	42	DIP		3.9	Site 48		
27C8000	27C8000-SOIC	44	SOP		4.1	PinSite	0302	.530 SOIC
27C8001	27C8001	32	DIP		3.4	Site 48/40		
27C8001	27C8001-SOIC	32	SO		4.1	PinSite	0302	.450 SOIC
27HC65	27HC65	24	DIP		2.8	Site 48/40		
28C256	28C256	28	DIP	36	2.8	Site 48/40		
28C64	28C64	28	DIP		2.5	SetSite		
28C64	28C64	28	DIP		2.5	Site 48/40		
28C64A	28C64A	28	DIP		3.8	Site 48/40		
71P301	71P301KA*	44	LCC	181	4.0	Site 48/40		
71P301	71P301KB*	64	LCC	182	4.0	Site 48/40		
71P301GF	71P301-QFP*	64	QFP	184	4.0	Site 48/40		
71P301GQ	71P301-QUIP*	64	QUIP	184	4.0	Site 48/40		
71P301L	71P301-PLCC*	44	PLCC	185	4.0	Site 48/40		
71P301RQ	71P301-QUIP*	64	QUIP	184	4.0	Site 48/40		
75P008	75P008-SDIP	42	SDIP		3.9	PinSite	9901	0602
75P008	75P008-QFP	44	QFP		3.9	PinSite	9901	0505
75P036	75P036-QFP	64	QFP		3.9	PinSite	9901	0503
75P036CW	75P036-SDIP	64	SDIP		4.0	PinSite	9901	0601
75P108	75P108-QFP	64	QFP		3.9	PinSite	9901	0501
75P108	75P108-SDIP	64	SDIP		3.9	PinSite	9901	0601

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
NEC Electronics Corp. (continued)								
75P108B	75P108B-QFP	64	QFP		3.9	PinSite	9901	0501
75P108B	75P108B-SDIP	64	SDIP		3.9	PinSite	9901	0601
75P116	75P116-QFP	64	QFP		3.9	PinSite	9901	0501
75P116	75P116-SDIP	64	SDIP		3.9	PinSite	9901	0601
75P216A	75P216A-SDIP	64	SDIP		3.9	PinSite	9901	0601
75P218	75P218-QFP	64	QFP		3.9	PinSite	9901	0501
75P218	75P218-SDIP	64	SDIP		3.9	PinSite	9901	0601
75P218KB	75P218-LCC	64	LCC		4.0	PinSite	9901	0202
75P238	75P238-QFP	94	QFP		3.9	PinSite	9901	0506
75P238KF	75P238-LCC	94	LCC		4.0	PinSite	9901	0216
75P308	75P308-LCC	80	LCC		3.9	PinSite	9901	0201
75P308	75P308-QFP	80	QFP		3.8	PinSite	9901	0502
75P316	75P316-QFP	80	QFP		3.8	PinSite	9901	0502
75P316A	75P316A-LCC	80	LCC		4.0	PinSite	9901	0201
75P316AGF	75P316A-QFP	64	QFP		3.9	PinSite	9901	0502
75P328	75P328-QFP	80	QFP		3.9	PinSite	9901	0504
75P336GC	75P336-QFP	80	QFP		4.0	PinSite	9901	0504
75P402	75P402	28	DIP		3.8	Site 48/40		
75P402CT	75P402-SDIP	28	SDIP		3.9	PinSite	9901	0603
75P402GB	75P402-QFP	44	QFP		4.0	PinSite	9901	0505
75P516	75P516-LCC	80	LCC		3.9	PinSite	9901	0201
75P516	75P516-QFP	80	QFP		3.9	PinSite	9901	0502
75P518	75P518-LCC	80	LCC		3.9	PinSite	9901	0201
75P518	75P518-QFP	80	QFP		3.9	PinSite	9901	0502
75P54	75P54-SDIP	20	SDIP		3.9	PinSite	9901	0603
75P54	75P54-SOIC	20	SO		4.0	PinSite	9901	0301
75P56	75P56-SDIP	24	SDIP		3.9	PinSite	9901	0603
75P56	75P56-SOIC	24	SO		3.9	PinSite	9901	0301
75P64	75P64-SDIP	20	SDIP		3.9	PinSite	9901	0603
75P64	75P64-SOIC	20	SO		3.9	PinSite	9901	0301
75P66	75P66-SDIP	24	SDIP		3.9	PinSite	9901	0603
75P66	75P66-SOIC	24	SO		3.9	PinSite	9901	0301
77P20	77P20	28	DIP	23	2.3	Site 48/40		
77P230	77P230-PGA	68	PGA		3.1	PinSite	0402/0401	
77P25	77P25	28	DIP	27	2.4	Site 48/40		
77P25	77P25-PLCC	44	PLCC	27	3.3	PinSite	0201	
77P56	77P56CR	20	DIP		2.8	Site 48		
78CP14	78CP14-QFP*	64	QFP	100	3.6	Site 48/40		
78CP14	78CP14-SDIP*	64	SDIP	84	3.2	Site 48/40		
78CP14	78CP14-PLCC	68	PLCC		3.4	ChipSite		
78CP14	78CP14-PLCC	68	PLCC		3.4	PinSite	0201	
78P014CW	78P014-SDIP	64	SDIP		4.1	PinSite	9901	0604
78P014GC	78P014-QFP	64	QFP		4.1	PinSite	9901	0510
78P214	78P214-QFP*	64	QFP	115,116	3.6	Site 48/40		
78P214	78P214-SDIP*	64	SDIP	85,116	3.6	Site 48/40		
78P214	78P214-PLCC*	68	PLCC		3.6	PinSite	0201	
78P214	78P214-PLCC*	68	PLCC	102,116,137	3.6	Site 48/40		
78P224	78P224-PLCC	84	PLCC		3.4	PinSite	0201	
78P312A	78P312A-QFP*	64	QFP	165	3.8	Site 48/40		
78P312A	78P312APLCC*	68	PLCC		3.3	PinSite	0201	
78P312A	78P312APLCC*	68	PLCC	167	3.8	Site 48/40		
78P312ACW	78P312ASDIP*	64	SDIP	164	3.8	Site 48/40		
78P312AGQ	78P312AQUIP*	64	QUIP	166	3.8	Site 48/40		
78P322	78P322KC*	68	LCC	9	3.8	Site 48/40		
78P322	78P322-PLCC*	68	PLCC	34	3.8	Site 48/40		
78P322	78P322KD*	74	LCC	5	3.8	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
NEC Electronics Corp. (continued)								
78P322	78P322GJ*	74	QFP	169	3.8	Site 48/40		
78P322	78P322GP*	80	QFP	168	3.8	Site 48/40		
78P324	78P324KD*	68	LCC	160	3.8	Site 48/40		
78P324	78P324-PLCC*	68	PLCC	159	3.8	Site 48/40		
78P324	78P324KC*	74	LCC	157	3.8	Site 48/40		
78P324	78P324-QFP*	74	QFP	158	3.8	Site 48/40		
78P328	78P328-QFP*	64	QFP	123	3.8	Site 48/40		
78P328	78P328-SDIP*	64	SDIP	124	3.8	Site 48/40		
78P334	78P334-LCC*	84	LCC	161	3.8	Site 48/40		
78P334	78P334-PLCC*	84	PLCC	163	3.8	Site 48/40		
78P334	78P334-QFP*	94	QFP	162	3.8	Site 48/40		
8741A	8741A	40	DIP		3.5	Site 48/40		
8748	8748	40	DIP		1.5	Site 48/40		
8748H	8748H	40	DIP		1.6	Site 48/40		
8749H	8749H	40	DIP		1.6	Site 48/40		
B400	B400	16	DIP		2.1	Site 48/40		
B401	B401	20	DIP		2.1	Site 48/40		
B402	B402	16	DIP		2.1	Site 48/40		
B403	B403	16	DIP		2.1	Site 48/40		
B404	B404	20	DIP		2.1	Site 48/40		
B405	B405	24	DIP		2.1	Site 48/40		
B406	B406	18	DIP		2.1	Site 48/40		
B407	B407	18	DIP		2.1	Site 48/40		
B408	B408	24	DIP		2.1	Site 48/40		
B409	B409	24	DIP		2.1	Site 48/40		
B410	B410	16	DIP		2.1	Site 48/40		
B412	B412	16	DIP		2.1	Site 48/40		
B417	B417	24	DIP		2.1	Site 48/40		
B419	B419	24	DIP		2.1	Site 48/40		
B421	B421	20	DIP		2.1	Site 48/40		
B423	B423	16	DIP		2.1	Site 48/40		
B424	B424	20	DIP		2.1	Site 48/40		
B425	B425	24	DIP		2.1	Site 48/40		
B426	B426	18	DIP		2.1	Site 48/40		
B427	B427	18	DIP		2.1	Site 48/40		
B428	B428	24	DIP		2.1	Site 48/40		
B429	B429	24	DIP		2.4	Site 48/40		
B431	B431	20	DIP		2.4	Site 48/40		
National Semiconductor Corp.								
10016C4	10016C4	28	PLCC	119	3.0	ChipSite		
10016C4	10016C4	28	PLCC	119	3.0	PinSite	0201	
10016LC4	10016LC4	24	DIP		2.7	Site 48/40		
10016LC8	10016LC8	24	DIP		2.7	Site 48/40		
10016LD4	10016LD4	24	DIP		2.7	Site 48/40		
10016LD8	10016LD8	24	DIP		2.7	Site 48/40		
10016LM4	10016LM4	24	DIP		2.7	Site 48/40		
10016P4	10016P4A/2	24	DIP	19,20	2.7	Site 48/40		
10016P8	10016P8/3	24	DIP	19	2.7	Site 48/40		
10016P8	10016P8/3PLC	28	PLCC	119	3.5	ChipSite		
10016P8	10016P8/3PLC	28	PLCC	119	3.5	PinSite	0201	
10016PE8	10016PE8	28	PLCC	119	3.4	ChipSite		
10016PE8	10016PE8	28	PLCC	119	3.4	PinSite	0201	
10016RC4	10016RC4	24	DIP		2.7	Site 48/40		
10016RC8	10016RC8	24	DIP		2.7	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
10016RD4	10016RD4	24	DIP		2.7	Site 48/40		
10016RD8	10016RD8	24	DIP	19	2.7	Site 48/40		
10016RM4	10016RM4/A	24	DIP		2.7	Site 48/40		
1016C4	1016C4/2PLCC	28	PLCC	119	3.0	ChipSite		
1016C4	1016C4/2PLCC	28	PLCC	119	3.0	PinSite	0201	
1016LC4	1016LC4	24	DIP		2.7	Site 48/40		
1016LC8	1016LC8	24	DIP		2.7	Site 48/40		
1016LD4	1016LD4	24	DIP		2.7	Site 48/40		
1016LD8	1016LD8	24	DIP		2.7	Site 48/40		
1016LM4	1016LM4	24	DIP		2.7	Site 48/40		
1016P4	1016P4A/2	24	DIP	19,20	2.7	Site 48/40		
1016P8	1016P8/3	24	DIP	19	2.7	Site 48/40		
1016P8	1016P8/3PLCC	28	PLCC	119	3.5	ChipSite		
1016P8	1016P8/3PLCC	28	PLCC	119	3.5	PinSite	0201	
1016PE8	1016PE8-PLCC	28	PLCC	119	3.4	ChipSite		
1016PE8	1016PE8-PLCC	28	PLCC	119	3.4	PinSite	0201	
1016RC4	1016RC4	24	DIP		2.7	Site 48/40		
1016RC8	1016RC8	24	DIP		2.7	Site 48/40		
1016RD4	1016RD4	24	DIP		2.7	Site 48/40		
1016RD8	1016RD8	24	DIP	19	2.7	Site 48/40		
1016RM4	1016RM4/A	24	DIP		2.7	Site 48/40		
10E149	10E149	16	DIP		2.6	Site 48/40		
10H8/A/A2	10H8/A/A2	20	DIP		3.0	Site 48/40		
10H8/A2	10H8-PLCC	20	PLCC		3.0	ChipSite		
10H8/A2	10H8-PLCC	20	PLCC		3.0	PinSite	0201	
10L8/A/A2	10L8/A/A2	20	DIP		3.0	Site 48/40		
10L8/A2	10L8-PLCC	20	PLCC		3.0	ChipSite		
10L8/A2	10L8-PLCC	20	PLCC		3.0	PinSite	0201	
12H6/A/A2	12H6/A/A2	20	DIP		3.0	Site 48/40		
12H6/A2	12H6-PLCC	20	PLCC		3.0	ChipSite		
12H6/A2	12H6-PLCC	20	PLCC		3.0	PinSite	0201	
12L10/A	12L10/A	24	DIP		3.0	Site 48/40		
12L6/A/A2	12L6/A/A2	20	DIP		3.0	Site 48/40		
12L6/A2	12L6-PLCC	20	PLCC		3.0	ChipSite		
12L6/A2	12L6-PLCC	20	PLCC		3.0	PinSite	0201	
14H4/A/A2	14H4/A/A2	20	DIP		3.0	Site 48/40		
14H4/A2	14H4-PLCC	20	PLCC		3.0	ChipSite		
14H4/A2	14H4-PLCC	20	PLCC		3.0	PinSite	0201	
14L4/A/A2	14L4/A/A2	20	DIP		3.0	Site 48/40		
14L4/A2	14L4-PLCC	20	PLCC		3.0	ChipSite		
14L4/A2	14L4-PLCC	20	PLCC		3.0	PinSite	0201	
14L8/A	14L8/A	24	DIP		3.0	Site 48/40		
16C1/A/A2	16C1/A/A2	20	DIP		3.0	Site 48/40		
16C1/A2	16C1-PLCC	20	PLCC		3.0	ChipSite		
16C1/A2	16C1-PLCC	20	PLCC		3.0	PinSite	0201	
16H2/A/A2	16H2/A/A2	20	DIP		3.0	Site 48/40		
16H2/A2	16H2-PLCC	20	PLCC		3.0	ChipSite		
16H2/A2	16H2-PLCC	20	PLCC		3.0	PinSite	0201	
16L2/A/A2	16L2/A/A2	20	DIP		3.0	Site 48/40		
16L2/A2	16L2-PLCC	20	PLCC		3.0	ChipSite		
16L2/A2	16L2-PLCC	20	PLCC		3.0	PinSite	0201	
16L6/A	16L6/A/A2	24	DIP		3.0	Site 48/40		
16L8-7	16L8D/7	20	DIP		3.4	Site 48/40		
16L8-7	16L8D/7-PLCC	20	PLCC		3.1	ChipSite		
16L8-7	16L8D/7-PLCC	20	PLCC		3.1	PinSite	0201	
16L8/A/A2	16L8/A/A2	20	DIP		3.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
16L8/A/A2	16L8/A-PLCC	20	PLCC		3.0	ChipSite		
16L8/A/A2	16L8/A-PLCC	20	PLCC		3.0	PinSite	0201	
16L8B	16L8B/B2-PLCC	20	PLCC		2.4	ChipSite		
16L8B	16L8B/B2-PLCC	20	PLCC		3.0	PinSite	0201	
16L8B/B2	16L8B/B2	20	DIP		3.0	Site 48/40		
16L8D	16L8D/7	20	DIP		2.6	Site 48/40		
16L8D	16L8D/7-PLCC	20	PLCC		2.8	ChipSite		
16L8D	16L8D/7-PLCC	20	PLCC		3.0	PinSite	0201	
16R4	16R4/A/A2	20	DIP		3.0	Site 48/40		
16R4	16R4/A-PLCC	20	PLCC		3.0	ChipSite		
16R4	16R4/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R4-7	16R4D/7	20	DIP		3.4	Site 48/40		
16R4-7	16R4D/7-PLCC	20	PLCC		3.4	ChipSite		
16R4-7	16R4D/7-PLCC	20	PLCC		3.4	PinSite	0201	
16R4B	16R4B-PLCC	20	PLCC		3.0	ChipSite		
16R4B	16R4B-PLCC	20	PLCC		3.0	PinSite	0201	
16R4B/B2	16R4B	20	DIP		3.0	Site 48/40		
16R4D	16R4D/7	20	DIP		2.6	Site 48/40		
16R4D	16R4D/7-PLCC	20	PLCC		3.2	ChipSite		
16R4D	16R4D/7-PLCC	20	PLCC		3.2	PinSite	0201	
16R6	16R6/A/A2	20	DIP		3.0	Site 48/40		
16R6	16R6/A-PLCC	20	PLCC		3.0	ChipSite		
16R6	16R6/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R6-7	16R6D/7	20	DIP		3.4	Site 48/40		
16R6-7	16R6D/7-PLCC	20	PLCC		3.4	ChipSite		
16R6-7	16R6D/7-PLCC	20	PLCC		3.4	PinSite	0201	
16R6B	16R6B-PLCC	20	PLCC		3.0	ChipSite		
16R6B	16R6B-PLCC	20	PLCC		3.0	PinSite	0201	
16R6B/B2	16R6B	20	DIP		3.0	Site 48/40		
16R6D	16R6D/7	20	DIP		2.6	Site 48/40		
16R6D	16R6D/7-PLCC	20	PLCC		3.2	ChipSite		
16R6D	16R6D/7-PLCC	20	PLCC		3.2	PinSite	0201	
16R8	16R8/A/A2	20	DIP		3.0	Site 48/40		
16R8	16R8/A-PLCC	20	PLCC		3.0	ChipSite		
16R8	16R8/A-PLCC	20	PLCC		3.0	PinSite	0201	
16R8-7	16R8D/7	20	DIP		3.4	Site 48/40		
16R8-7	16R8D/7-PLCC	20	PLCC		3.4	ChipSite		
16R8-7	16R8D/7-PLCC	20	PLCC		3.4	PinSite	0201	
16R8B	16R8B-PLCC	20	PLCC		3.0	ChipSite		
16R8B	16R8B-PLCC	20	PLCC		3.0	PinSite	0201	
16R8B/B2	16R8B	20	DIP		3.0	Site 48/40		
16R8D	16R8D/7	20	DIP		2.6	Site 48/40		
16R8D	16R8D/7-PLCC	20	PLCC		3.2	ChipSite		
16R8D	16R8D/7-PLCC	20	PLCC		3.2	PinSite	0201	
16RA8	16RA8	20	DIP		3.6	Site 48/40		
16RA8	16RA8-PLCC	20	PLCC		3.6	ChipSite		
16RA8	16RA8-PLCC	20	PLCC		3.6	PinSite	0201	
16V8	16V8/A/QS	20	DIP	22,49	3.6	Site 48/40		
16V8	16V8/A-PLCC	20	PLCC	22,49	3.6	ChipSite		
16V8	16V8/A-PLCC	20	PLCC	22,49	3.6	PinSite	0201	
16V8-10	16V8_7/10	20	DIP	22,49	3.6	Site 48/40		
16V8-10	16V8_7/10-PL	20	PLCC	22,49	3.6	ChipSite		
16V8-10	16V8_7/10-PL	20	PLCC	22,49	3.6	PinSite	0201	
16V8-7	16V8_7/10	20	DIP	22,49	3.6	Site 48/40		
16V8-7	16V8_7/10-PL	20	PLCC	22,49	3.6	ChipSite		
16V8-7	16V8_7/10-PL	20	PLCC	22,49	3.6	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
16V8A	16V8/A/QS	20	DIP	22,49	3.6	Site 48/40		
16V8A	16V8QS-PLCC	20	PLCC	22,49	3.6	ChipSite		
16V8A	16V8QS-PLCC	20	PLCC	22,49	3.6	PinSite	0201	
18L4/A	18L4/A	24	DIP		3.0	Site 48/40		
20C1	20C1	24	DIP		3.0	Site 48/40		
20C1-XV	20C1-XV	28	PLCC		3.0	ChipSite		
20C1-XV	20C1-XV	28	PLCC		3.0	PinSite	0201	
20L10/A	20L10/A	24	DIP		3.0	Site 48/40		
20L10/A-XV	20L10/A-XV	28	PLCC		3.0	ChipSite		
20L10/A-XV	20L10/A-XV	28	PLCC		3.0	PinSite	0201	
20L10A-V	20L10/A-V	28	PLCC		3.0	ChipSite		
20L10A-V	20L10/A-V	28	PLCC		3.0	PinSite	0201	
20L2/A	20L2/A	24	DIP		3.0	Site 48/40		
20L8-5	20L8D/7/5	24	DIP		3.6	Site 48/40		
20L8-5	20L8D/7/5-PL	28	PLCC		3.6	ChipSite		
20L8-5	20L8D/7/5-PL	28	PLCC		3.6	PinSite	0201	
20L8-7	20L8D/7/5	24	DIP		3.4	Site 48/40		
20L8-7	20L8D/7/5-PL	28	PLCC		3.4	ChipSite		
20L8-7	20L8D/7/5-PL	28	PLCC		3.6	PinSite	0201	
20L8A	20L8/A	24	DIP		3.0	Site 48/40		
20L8A-V	20L8A-V	28	PLCC		3.0	ChipSite		
20L8A-V	20L8A-V	28	PLCC		3.0	PinSite	0201	
20L8A-XV	20L8A-XV	28	PLCC		3.0	ChipSite		
20L8A-XV	20L8A-XV	28	PLCC		3.0	PinSite	0201	
20L8B	20L8B	24	DIP		3.0	Site 48/40		
20L8B-V	20L8B-V	28	PLCC		3.0	ChipSite		
20L8B-V	20L8B-V	28	PLCC		3.0	PinSite	0201	
20L8B-XV	20L8B-XV	28	PLCC		3.0	ChipSite		
20L8B-XV	20L8B-XV	28	PLCC		3.0	PinSite	0201	
20L8D	20L8D/7/5	24	DIP		2.8	Site 48/40		
20L8D	20L8D/7/5-PL	28	PLCC		3.4	ChipSite		
20L8D	20L8D/7/5-PL	28	PLCC		3.4	PinSite	0201	
20P8B	20P8B	24	DIP		1.5	Site 48/40		
20P8B-V	20P8B-V	28	PLCC		3.3	ChipSite		
20P8B-V	20P8B-V	28	PLCC		3.3	PinSite	0201	
20R4-5	20R4D/7/5	24	DIP		3.6	Site 48/40		
20R4-5	20R4D/7/5-PL	28	PLCC		3.6	ChipSite		
20R4-5	20R4D/7/5-PL	28	PLCC		3.6	PinSite	0201	
20R4-7	20R4D/7/5	24	DIP		3.4	Site 48/40		
20R4-7	20R4D/7/5-PL	28	PLCC		3.4	ChipSite		
20R4-7	20R4D/7/5-PL	28	PLCC		3.4	PinSite	0201	
20R4A	20R4A/B	24	DIP		3.0	Site 48/40		
20R4A-XV	20R4A-PLCC	28	PLCC		3.0	ChipSite		
20R4A-XV	20R4A-PLCC	28	PLCC		3.0	PinSite	0201	
20R4B	20R4A/B	24	DIP		3.0	Site 48/40		
20R4B-V	20R4B-V	28	PLCC		3.0	ChipSite		
20R4B-V	20R4B-V	28	PLCC		3.0	PinSite	0201	
20R4B-XV	20R4B-XV	28	PLCC		3.0	ChipSite		
20R4B-XV	20R4B-XV	28	PLCC		3.0	PinSite	0201	
20R4D	20R4D/7/5	24	DIP		2.8	Site 48/40		
20R4D	20R4D/7/5-PL	28	PLCC		3.4	ChipSite		
20R4D	20R4D/7/5-PL	28	PLCC		3.4	PinSite	0201	
20R6-5	20R6D/7/5	24	DIP		3.6	Site 48/40		
20R6-5	20R6D/7/5-PL	28	PLCC		3.6	ChipSite		
20R6-5	20R6D/7/5-PL	28	PLCC		3.6	PinSite	0201	
20R6-7	20R6D/7/5	24	DIP		3.4	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
20R6-7	20R6D/7/5-PL	28	PLCC		3.4	ChipSite		
20R6-7	20R6D/7/5-PL	28	PLCC		3.4	PinSite	0201	
20R6A	20R6A/B	24	DIP		3.0	Site 48/40		
20R6A-XV	20R6A-PLCC	28	PLCC		3.0	ChipSite		
20R6A-XV	20R6A-PLCC	28	PLCC		3.0	PinSite	0201	
20R6B	20R6A/B	24	DIP		3.0	Site 48/40		
20R6B-V	20R6B-V	28	PLCC		3.0	ChipSite		
20R6B-V	20R6B-V	28	PLCC		3.0	PinSite	0201	
20R6B-XV	20R6B-XV	28	PLCC		3.0	ChipSite		
20R6B-XV	20R6B-XV	28	PLCC		3.0	PinSite	0201	
20R6D	20R6D/7/5	24	DIP		2.8	Site 48/40		
20R6D	20R6D/7/5-PL	28	PLCC		3.4	ChipSite		
20R6D	20R6D/7/5-PL	28	PLCC		3.4	PinSite	0201	
20R8-5	20R8D/7/5	24	DIP		3.6	Site 48/40		
20R8-5	20R8D/7/5-PL	28	PLCC		3.6	ChipSite		
20R8-5	20R8D/7/5-PL	28	PLCC		3.6	PinSite	0201	
20R8-7	20R8D/7/5	24	DIP		3.4	Site 48/40		
20R8-7	20R8D/7/5-PL	28	PLCC		3.4	ChipSite		
20R8-7	20R8D/7/5-PL	28	PLCC		3.4	PinSite	0201	
20R8A	20R8A/B	24	DIP		3.0	Site 48/40		
20R8A-XV	20R8A-PLCC	28	PLCC		3.0	ChipSite		
20R8A-XV	20R8A-PLCC	28	PLCC		3.0	PinSite	0201	
20R8B	20R8A/B	24	DIP		3.0	Site 48/40		
20R8B-V	20R8B-V	28	PLCC		3.0	ChipSite		
20R8B-V	20R8B-V	28	PLCC		3.0	PinSite	0201	
20R8B-XV	20R8B-XV	28	PLCC		3.0	ChipSite		
20R8B-XV	20R8B-XV	28	PLCC		3.0	PinSite	0201	
20R8D	20R8D/7/5	24	DIP		2.8	Site 48/40		
20R8D	20R8D/7/5-PL	28	PLCC		3.4	ChipSite		
20R8D	20R8D/7/5-PL	28	PLCC		3.4	PinSite	0201	
20RA10	20RA10	24	DIP		2.4	Site 48/40		
20RA10	20RA10GAL	24	DIP	32	3.5	Site 48/40		
20RA10	20RA10GALPLC	28	PLCC	32	3.5	ChipSite		
20RA10	20RA10GALPLC	28	PLCC	32	3.5	PinSite	0201	
20RA10-V	20RA10-V	28	PLCC		3.4	ChipSite		
20RA10-V	20RA10-V	28	PLCC		3.4	PinSite	0201	
20RA10-XV	20RA10-XV	28	PLCC		1.6	ChipSite		
20RA10-XV	20RA10-XV	28	PLCC		3.0	PinSite	0201	
20RA10UES	20RA10GALUES	24	DIP	32	3.5	Site 48/40		
20RA10UES	20RA10GU-PLC	28	PLCC	32	3.5	ChipSite		
20RA10UES	20RA10GU-PLC	28	PLCC	32	3.5	PinSite	0201	
20RP4B	20RP4B	24	DIP		1.5	Site 48/40		
20RP6B	20RP6B	24	DIP		1.5	Site 48/40		
20RP8B	20RP8B	24	DIP		1.5	Site 48/40		
20V8	20V8/A/QS	24	DIP	22,49	3.6	Site 48/40		
20V8	20V8/A-PLCC	28	PLCC	22,49	3.6	ChipSite		
20V8	20V8/A-PLCC	28	PLCC	22,49	3.6	PinSite	0201	
20V8-10	20V8_7/10	24	DIP	22,49	3.6	Site 48/40		
20V8-10	20V8_7/10-PL	28	PLCC	22,49	3.6	ChipSite		
20V8-10	20V8_7/10-PL	28	PLCC	22,49	3.6	PinSite	0201	
20V8-7	20V8_7/10	24	DIP	22,49	3.6	Site 48/40		
20V8-7	20V8_7/10-PL	28	PLCC	22,49	3.6	ChipSite		
20V8-7	20V8_7/10-PL	28	PLCC	22,49	3.6	PinSite	0201	
20V8/A/QS	20V8/A/QS	24	DIP	22,49	3.6	Site 48/40		
20V8/A/QS	20V8QS-PLCC	28	PLCC	22,49	3.6	ChipSite		
20V8/A/QS	20V8QS-PLCC	28	PLCC	22,49	3.6	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
20X10	20X10	24	DIP		3.0	Site 48/40		
20X10A	20X10A	24	DIP		3.0	Site 48/40		
20X10A-V	20X10A-V	28	PLCC		3.0	ChipSite		
20X10A-V	20X10A-V	28	PLCC		3.0	PinSite	0201	
20X4	20X4	24	DIP		3.0	Site 48/40		
20X4A	20X4A	24	DIP		3.0	Site 48/40		
20X4A-V	20X4A-V	28	PLCC		3.3	ChipSite		
20X4A-V	20X4A-V	28	PLCC		3.3	PinSite	0201	
20X8	20X8	24	DIP		3.0	Site 48/40		
20X8-XV	20X8-XV	28	PLCC		3.0	ChipSite		
20X8-XV	20X8-XV	28	PLCC		3.0	PinSite	0201	
20X8A	20X8A	24	DIP		3.0	Site 48/40		
20X8A-V	20X8A-V	28	PLCC		3.0	ChipSite		
20X8A-V	20X8A-V	28	PLCC		3.0	PinSite	0201	
22CV10-10	22CV10-10	24	DIP	33	4.2	Site 48/40		
22CV10-10	22CV10-10-PL	28	PLCC	33	4.2	ChipSite		
22CV10-10	22CV10-10-PL	28	PLCC	33	4.2	PinSite	0201	
22CV10-7	22CV10-7	24	DIP	33	4.2	Site 48/40		
22CV10-7	22CV10-7-PLC	28	PLCC	33	4.2	ChipSite		
22CV10-7	22CV10-7-PLC	28	PLCC	33	4.2	PinSite	0201	
22V10	22V10	24	DIP		3.6	Site 48/40		
22V10	22V10-PLCC	28	PLCC		3.6	ChipSite		
22V10	22V10-PLCC	28	PLCC		3.6	PinSite	0201	
22V10UES	22V10UES	24	DIP		3.6	Site 48/40		
22V10UES	22V10UES-PLC	28	PLCC		3.6	ChipSite		
22V10UES	22V10UES-PLC	28	PLCC		3.6	PinSite	0201	
2532	2532	24	DIP		2.0	SetSite		
2532	2532	24	DIP		2.0	Site 48/40		
2708	2708	24	DIP		2.0	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
2716	2716	24	DIP		2.0	SetSite		
2716	2716	24	DIP		2.0	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2758A	2758A	24	DIP		2.0	SetSite		
2758A	2758A	24	DIP		2.0	Site 48/40		
2758B	2758B	24	DIP		2.0	SetSite		
2758B	2758B	24	DIP		2.0	Site 48/40		
27C010	27C010	32	DIP		2.2	SetSite		
27C010	27C010	32	DIP		2.2	Site 48/40		
27C010	27C010-PLCC	32	PLCC		3.1	ChipSite		
27C010	27C010-PLCC	32	PLCC		3.1	PinSite	0201	
27C020	27C020	32	DIP		4.2	SetSite		
27C020	27C020	32	DIP		4.2	Site 48/40		
27C040	27C040	32	DIP		3.5	Site 48/40		
27C1024	27C1024	40	DIP		2.2	SetSite		
27C1024	27C1024	40	DIP		2.2	Site 48/40		
27C128B	27C128B	28	DIP		3.0	SetSite		
27C128B	27C128B	28	DIP		2.6	Site 48/40		
27C128B	27C128B-PLCC	32	PLCC		3.4	ChipSite		
27C128B	27C128B-PLCC	32	PLCC		3.4	PinSite	0201	
27C16	27C16	24	DIP		2.0	SetSite		
27C16	27C16	24	DIP		2.0	Site 48/40		
27C16B	27C16B	24	DIP		2.7	Site 48/40		
27C16H	27C16H	24	DIP		2.0	SetSite		
27C16H	27C16H	24	DIP		2.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
27C210	27C210	40	DIP		3.5	Site 48/40		
27C210	27C210-PLCC	44	PLCC		3.9	ChipSite		
27C210	27C210-PLCC	44	PLCC		3.9	PinSite	0201	
27C256	27C256	28	DIP		2.0	SetSite		
27C256	27C256	28	DIP		1.7	Site 48/40		
27C256B	27C256B	28	DIP		3.0	SetSite		
27C256B	27C256B	28	DIP		2.5	Site 48/40		
27C256B	27C256B-PLCC	32	PLCC		3.1	ChipSite		
27C256B	27C256B-PLCC	32	PLCC		3.1	PinSite	0201	
27C32	27C32	24	DIP		2.0	SetSite		
27C32	27C32	24	DIP		2.0	Site 48/40		
27C32B	27C32B	24	DIP		2.7	SetSite		
27C32B	27C32B	24	DIP		2.7	Site 48/40		
27C32H	27C32H	24	DIP		2.0	SetSite		
27C32H	27C32H	24	DIP		1.3	Site 48/40		
27C512	27C512	28	DIP		2.0	SetSite		
27C512	27C512	28	DIP		3.6	Site 48/40		
27C512A	27C512A	28	DIP		2.2	SetSite		
27C512A	27C512A	28	DIP		2.2	Site 48/40		
27C512A	27C512A-PLCC	32	PLCC		3.1	ChipSite		
27C512A	27C512A-PLCC	32	PLCC		3.1	PinSite	0201	
27C58A	27C58A	24	DIP		2.0	SetSite		
27C58A	27C58A	24	DIP		2.0	Site 48/40		
27C58B	27C58B	24	DIP		2.0	SetSite		
27C58B	27C58B	24	DIP		2.0	Site 48/40		
27C64	27C64	28	DIP		2.0	SetSite		
27C64	27C64	28	DIP		1.7	Site 48/40		
27C64B	27C64B	28	DIP		2.3	SetSite		
27C64B	27C64B	28	DIP		2.3	Site 48/40		
27CP128	27CP128	28	DIP		2.0	SetSite		
27CP128	27CP128	28	DIP		1.7	Site 48/40		
27LC256	27LC256	28	DIP		4.1	Site 48/40		
27LC512	27LC512	28	DIP		4.1	Site 48/40		
27LC512	27LC512-PLCC	32	PLCC		4.1	ChipSite		
27LC512	27LC512-PLCC	32	PLCC		4.1	PinSite	0201	
27LC64	27LC64	28	DIP		3.9	Site 48		
27LV010	27LV010-PLCC	32	PLCC		3.9	ChipSite		
27LV010	27LV010-PLCC	32	PLCC		3.9	PinSite	0201	
27LV010	27LV010-TSOP	32	TSOP		4.2	PinSite	9901	0702
27LV210	27LV210	40	DIP		4.1	Site 48/40		
27LV210	27LV210-PLCC	44	PLCC		4.1	ChipSite		
27LV210	27LV210-PLCC	44	PLCC		4.1	PinSite	0201	
27LV512	27LV512-PLCC	32	PLCC		4.1	ChipSite		
27LV512	27LV512-PLCC	32	PLCC		4.1	PinSite	0201	
27LV512	27LV512-TSOP	32	TSOP		4.2	PinSite	9901	0702
27P210	27P210	40	DIP		3.9	Site 48/40		
27P210	27P210-PLCC	44	PLCC		4.2	ChipSite		
27P210	27P210-PLCC	44	PLCC		4.2	PinSite	0201	
27P512	27P512	28	DIP		3.9	Site 48/40		
27P512	27P512-PLCC	32	PLCC		4.1	ChipSite		
27P512	27P512-PLCC	32	PLCC		4.1	PinSite	0201	
2816	2816	24	DIP		2.0	SetSite		
2816	2816	24	DIP		2.0	Site 48/40		
2864	2864	28	DIP		2.8	SetSite		
2864	2864	28	DIP		2.0	Site 48/40		
48F512	48F512	32	DIP		2.8	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
54LS471	54LS471	20	DIP		2.2	Site 48/40		
54S188	54S188	16	DIP		2.2	Site 48/40		
54S287	54S287	16	DIP		2.2	Site 48/40		
54S288	54S288	16	DIP		2.2	Site 48/40		
54S387	54S387	16	DIP		2.2	Site 48/40		
54S472	54S472	20	DIP		2.2	Site 48/40		
54S473	54S473	20	DIP		2.2	Site 48/40		
54S474	54S474	24	DIP		2.2	Site 48/40		
54S475	54S475	24	DIP		2.2	Site 48/40		
54S570	54S570	16	DIP		2.2	Site 48/40		
54S571	54S571	16	DIP		2.2	Site 48/40		
54S572	54S572	18	DIP		2.2	Site 48/40		
54S573	54S573	18	DIP		2.2	Site 48/40		
6001	6001	24	DIP	49	3.6	Site 48/40		
6001	6001-PLCC	28	PLCC	49	3.6	ChipSite		
6001	6001-PLCC	28	PLCC	49	3.6	PinSite	0201	
74LS471	74LS471	20	DIP		2.2	Site 48/40		
74LS471	74LS471-PLCC	20	PLCC		4.0	PinSite	0201	
74S188	74S188	16	DIP		2.2	Site 48/40		
74S287	74S287	16	DIP		2.2	Site 48/40		
74S288	74S288	16	DIP		2.2	Site 48/40		
74S288	74S288-PLCC	20	PLCC		3.4	PinSite	0201	
74S387	74S387	16	DIP		2.2	Site 48/40		
74S472	74S472	20	DIP		2.2	Site 48/40		
74S472	74S472-PLCC	20	PLCC		2.4	ChipSite		
74S472	74S472-PLCC	20	PLCC		3.0	PinSite	0201	
74S473	74S473	20	DIP		2.2	Site 48/40		
74S474	74S474	24	DIP		2.2	Site 48/40		
74S475	74S475	24	DIP		2.2	Site 48/40		
74S570	74S570	16	DIP		2.2	Site 48/40		
74S571	74S571	16	DIP		2.2	Site 48/40		
74S572	74S572	18	DIP		2.2	Site 48/40		
74S573	74S573	18	DIP		2.2	Site 48/40		
77S180	77S180	24	DIP		2.2	Site 48/40		
77S181	77S181	24	DIP		2.2	Site 48/40		
77S184	77S184	18	DIP		2.2	Site 48/40		
77S185	77S185	18	DIP		2.2	Site 48/40		
77S190	77S190	24	DIP		2.2	Site 48/40		
77S191	77S191	24	DIP		2.2	Site 48/40		
77S280	77S280	24	DIP		2.2	Site 48/40		
77S281	77S281	24	DIP		2.2	Site 48/40		
77S290	77S290	24	DIP		2.2	Site 48/40		
77S291	77S291	24	DIP		2.2	Site 48/40		
77S295	77S295	24	DIP		2.2	Site 48/40		
77S296	77S296	24	DIP		2.2	Site 48/40		
77SR181	77SR181	24	DIP	1	2.2	Site 48/40		
77SR183	77SR183	24	DIP	1	2.2	Site 48/40		
77SR191	77SR191	24	DIP	3	2.3	Site 48/40		
77SR193	77SR193	24	DIP	3	2.3	Site 48/40		
77SR25	77SR25	24	DIP		2.2	Site 48/40		
77SR474	77SR474	24	DIP		2.2	Site 48/40		
77SR476	77SR476	24	DIP	1	2.2	Site 48/40		
77X288	77X288	16	DIP		2.2	Site 48/40		
87S180	87S180	24	DIP		2.2	Site 48/40		
87S181	87S181	24	DIP		2.2	Site 48/40		
87S184	87S184	18	DIP		2.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. (continued)								
87S185	87S185	18	DIP		2.2	Site 48/40		
87S190	87S190	24	DIP		2.2	Site 48/40		
87S191	87S191	24	DIP		2.2	Site 48/40		
87S280	87S280	24	DIP		2.2	Site 48/40		
87S281	87S281	24	DIP		2.2	Site 48/40		
87S290	87S290	24	DIP		2.2	Site 48/40		
87S291	87S291	24	DIP		2.2	Site 48/40		
87S295	87S295	24	DIP		2.2	Site 48/40		
87S296	87S296	24	DIP		2.2	Site 48/40		
87S421	87S421	24	DIP		2.8	Site 48/40		
87SR181	87SR181	24	DIP	1	2.2	Site 48/40		
87SR183	87SR183	24	DIP	1	2.2	Site 48/40		
87SR191	87SR191	24	DIP	3	2.3	Site 48/40		
87SR193	87SR193	24	DIP	3	2.3	Site 48/40		
87SR25	87SR25	24	DIP		2.2	Site 48/40		
87SR474	87SR474	24	DIP		2.2	Site 48/40		
87SR476	87SR476	24	DIP	1	2.2	Site 48/40		
87X288	87X288	16	DIP		2.2	Site 48/40		
9346	9346	8	DIP		2.8	Site 48/40		
93C06	93C06	8	DIP		3.1	Site 48/40		
93C46	93C46	8	DIP		3.1	Site 48/40		
93C46	93C46M-SOIC	14	SO		3.9	PinSite	0302/0301	.150 SOIC
93C56	93C56	8	DIP		3.1	Site 48/40		
93C66	93C66	8	DIP		3.1	Site 48/40		
93CS06	93CS06	8	DIP		3.1	Site 48/40		
93CS46	93CS46	8	DIP		3.1	Site 48/40		
93CS66	93CS66	8	DIP		3.1	Site 48/40		
93Z665	93Z665	24	DIP		2.2	Site 48/40		
93Z667	93Z667	24	DIP		2.2	Site 48/40		
9716	9716	24	DIP		2.0	SetSite		
9716	9716	24	DIP		2.0	Site 48/40		
9816A	9816A	24	DIP		2.0	SetSite		
9816A	9816A	24	DIP		2.0	Site 48/40		
9817	9817	28	DIP		2.5	SetSite		
9817	9817	28	DIP		2.5	Site 48/40		
9817A	9817A	28	DIP		2.5	SetSite		
9817A	9817A	28	DIP		2.5	Site 48/40		
COP842	842	20	DIP		3.2	Site 48		
COP8640	8640	28	DIP		3.3	Site 48		
COP8780C	8780C	40	DIP	2,21,145	3.9	Site 48		
COP8780C	8780C-JLCC	44	JLCC	2,21,145	3.9	PinSite	0201	
COP8780C	8780C-PLCC	44	PLCC	2,21,145	3.9	PinSite	0201	
COP8781C	8781C	28	DIP	2,21,145	3.9	Site 48		
COP8782C	8782C	20	DIP	2,21,145	3.9	Site 48		
COP880	880	40	DIP		3.3	Site 48		
COP881	881	28	DIP		3.3	Site 48		
COP884	884	28	DIP		3.3	Site 48		
COP888	888-JLCC	44	JLCC		3.3	PinSite	0201	
HPC46083	46083-JLCC	68	JLCC		3.0	PinSite	0201	
HPC467064	467064	68	JLCC	144	3.8	PinSite	0201	
MAPL128	MAPL128	28	PLCC		3.4	ChipSite		
MAPL128	MAPL128	28	PLCC		3.4	PinSite	0201	
MAPL144	MAPL144-PLCC	44	PLCC		3.8	PinSite	0201	
MAPL244	MAPL244-PLCC	44	PLCC		4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Oki Electric Industry Co., Ltd.								
16811	16811	8	DIP		4.0	Site 48/40		
16851	16851	8	DIP		4.0	Site 48/40		
16911	16911	8	DIP		4.0	Site 48/40		
16951	16951	8	DIP		4.0	Site 48/40		
2532	2532	24	DIP		2.0	SetSite		
2532	2532	24	DIP		2.0	Site 48/40		
2708	2708	24	DIP		2.8	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
271000	271000	32	DIP		3.0	SetSite		
271000	271000	32	DIP		2.8	Site 48/40		
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		2.0	Site 48/40		
27128A	27128A	28	DIP		2.7	SetSite		
27128A	27128A	28	DIP		2.7	Site 48/40		
2716	2716	24	DIP		2.0	SetSite		
2716	2716	24	DIP		2.0	Site 48/40		
27256	27256	28	DIP		3.0	SetSite		
27256	27256	28	DIP		3.0	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
27512	27512	28	DIP		2.2	SetSite		
27512	27512	28	DIP		2.2	Site 48/40		
2758	2758	24	DIP		2.0	SetSite		
2758	2758	24	DIP		2.0	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		
2764A	2764A	28	DIP		2.2	Site 48/40		
27C2000	27C2000	32	DIP		3.1	SetSite		
27C2000	27C2000	32	DIP		3.1	Site 48/40		
27C256H	27C256H	28	DIP		2.8	Site 48/40		
27C802	27C802	42	DIP		4.2	Site 48		
27C802	27C802-SOIC	44	SO		4.2	PinSite	0302	.530 SOIC
27C822	27C822	42	DIP		4.2	Site 48		
27C822	27C822-SOIC	44	SO		4.2	PinSite	0302	.530 SOIC
27C832	27C832	42	DIP		4.2	Site 48		
27C832	27C832-SOIC	44	SO		4.2	PinSite	0302/0301	.530 SOIC
2816A	2816A	24	DIP		2.8	SetSite		
2816A	2816A	24	DIP		2.2	Site 48/40		
28C16A	28C16A	24	DIP		2.8	SetSite		
28C16A	28C16A	24	DIP		2.2	Site 48/40		
28C64A	28C64A	28	DIP		2.8	SetSite		
28C64A	28C64A	28	DIP		2.8	Site 48/40		
Omni-Wave Semiconductor								
27C101	27C101	32	DIP		3.9	SetSite		
27C101	27C101	32	DIP		3.5	Site 48/40		
27C1024	27C1024	40	DIP		3.5	Site 48/40		
27C256	27C256	28	DIP		3.5	Site 48/40		
PLX Technology								
448	PLX448	24	DIP		2.4	Site 48/40		
464	PLX464	24	DIP		2.7	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Panasonic Semiconductor								
27C256	27C256	28	DIP		3.0	SetSite		
27C256	27C256	28	DIP		3.0	Site 48/40		
27C512	27C512	28	DIP		3.0	SetSite		
27C512	27C512	28	DIP		3.0	Site 48/40		
27C64A	27C64A	28	DIP		3.0	Site 48/40		
Philips Semiconductor								
100149	100149/A/B	16	DIP		3.1	Site 48/40		
100149A	100149/A/B	16	DIP		3.6	Site 48/40		
100149B	100149/A/B	16	DIP		3.6	Site 48/40		
10020EV8	10020EV8	24	DIP		4.2	Site 48/40		
10020EV8	10020EV8PLCC	28	PLCC	119	4.2	ChipSite		
10020EV8	10020EV8PLCC	28	PLCC	119	4.2	PinSite	0201	
10149	10149	16	DIP	19	3.1	Site 48/40		
10149A	10149A	16	DIP		3.1	Site 48/40		
10H20EV8	10H20EV8	24	DIP	28	4.2	Site 48/40		
10H20EV8	10H20EV8PLCC	28	PLCC	28,119	4.2	ChipSite		
10H20EV8	10H20EV8PLCC	28	PLCC	28,119	4.2	PinSite	0201	
10P256	100P256	18	DIP		3.6	Site 48		
27C010	27C010	32	DIP		4.2	SetSite		
27C010	27C010	32	DIP		3.4	Site 48/40		
27C010	27C010-PLCC	32	PLCC		4.0	ChipSite		
27C010	27C010-PLCC	32	PLCC		4.0	PinSite	0201	
27C210	27C210	40	DIP		3.0	SetSite		
27C210	27C210	40	DIP		2.7	Site 48/40		
27C210	27C210-PLCC	44	PLCC		2.7	ChipSite		
27C210	27C210-PLCC	44	PLCC		3.0	PinSite	0201	
27C256	27C256	28	DIP		2.2	SetSite		
27C256	27C256	28	DIP		2.2	Site 48/40		
27C256	27C256-PLCC	32	PLCC		2.4	ChipSite		
27C256	27C256-PLCC	32	PLCC		3.0	PinSite	0201	
27C512	27C512	28	DIP		2.5	SetSite		
27C512	27C512	28	DIP		2.5	Site 48/40		
27C512	27C512-SOIC	28	SO		4.2	PinSite	0302/0301	.220 SOIC
27C512	27C512-PLCC	32	PLCC		2.7	ChipSite		
27C512	27C512-PLCC	32	PLCC		3.0	PinSite	0201	
27C64A	27C64A	28	DIP		2.2	SetSite		
27C64A	27C64A	28	DIP		2.2	Site 48/40		
27C64A	27C64A-PLCC	32	PLCC		2.5	ChipSite		
27C64A	27C64A-PLCC	32	PLCC		3.0	PinSite	0201	
27HC641	27HC641	24	DIP		2.8	SetSite		
27HC641	27HC641	24	DIP		2.8	Site 48/40		
27HC641	27HC641-PLCC	28	PLCC		2.8	ChipSite		
27HC641	27HC641-PLCC	28	PLCC		3.0	PinSite	0201	
82123	82123	16	DIP		1.4	Site 48/40		
82HS187	82HS187	24	DIP	1	4.2	Site 48/40		
82HS187	82HS187-PLCC	28	PLCC	1	4.2	ChipSite		
82HS187	82HS187-PLCC	28	PLCC	1	4.2	PinSite	0201	
82HS189	82HS189	24	DIP	1	4.2	Site 48/40		
82HS189	82HS189-PLCC	28	PLCC	1	4.2	ChipSite		
82HS189	82HS189-PLCC	28	PLCC	1	4.2	PinSite	0201	
82HS191	82HS191	24	DIP		4.2	Site 48/40		
82HS191	82HS191-PLCC	28	PLCC		4.2	ChipSite		
82HS191	82HS191-PLCC	28	PLCC		4.2	PinSite	0201	
82HS195	82HS195	20	DIP		4.2	Site 48/40		
82HS195	82HS195-PLCC	20	PLCC		4.2	ChipSite		
82HS195	82HS195-PLCC	20	PLCC		4.2	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Philips Semiconductor (continued)								
82HS321	82HS321	24	DIP		4.2	Site 48/40		
82HS321	82HS321-PLCC	28	PLCC		4.2	ChipSite		
82HS321	82HS321-PLCC	28	PLCC		4.2	PinSite	0201	
82HS641	82HS641	24	DIP		4.0	Site 48/40		
82HS641	82HS641-LCC	28	LCC		4.0	ChipSite		
82HS641	82HS641-LCC	28	LCC		4.0	PinSite	0202	
82HS641	82HS641-PLCC	28	PLCC		4.0	ChipSite		
82HS641	82HS641-PLCC	28	PLCC		4.0	PinSite	0201	
82LS135	82LS135	20	DIP		1.4	Site 48/40		
82LS135	82LS135-PLCC	20	PLCC		3.0	ChipSite		
82LS135	82LS135-PLCC	20	PLCC		3.0	PinSite	0201	
82LS180	82LS180	24	DIP		1.4	Site 48/40		
82LS181	82LS181	24	DIP		1.4	Site 48/40		
82S100	82S100	28	DIP		3.6	Site 48/40		
82S100	82S100-PLCC	28	PLCC		3.6	ChipSite		
82S100	82S100-PLCC	28	PLCC		3.6	PinSite	0201	
82S101	82S101	28	DIP		3.6	Site 48/40		
82S101	82S101-PLCC	28	PLCC		3.6	ChipSite		
82S101	82S101-PLCC	28	PLCC		3.6	PinSite	0201	
82S105	82S105	28	DIP		3.6	Site 48/40		
82S105	82S105-PLCC	28	PLCC		3.6	ChipSite		
82S105	82S105-PLCC	28	PLCC		3.6	PinSite	0201	
82S115	82S115	24	DIP		1.1	Site 48/40		
82S123	82S123	16	DIP		1.4	Site 48/40		
82S123	82S123-SOIC	16	SO		1.6	ChipSite		
82S123	82S123-SOIC	16	SO		3.0	PinSite	0302/0301	.300 SOIC
82S123	82S123-PLCC	20	PLCC		1.6	ChipSite		
82S123	82S123-PLCC	20	PLCC		3.0	PinSite	0201	
82S126	82S126	16	DIP		1.7	Site 48/40		
82S126	82S126-SOIC	16	SO		3.0	ChipSite		
82S126	82S126-SOIC	16	SO		3.0	PinSite	0302/0301	.300 SOIC
82S126	82S126-PLCC	20	PLCC		3.0	ChipSite		
82S126	82S126-PLCC	20	PLCC		3.0	PinSite	0201	
82S129	82S129	16	DIP		1.7	Site 48/40		
82S129	82S129-SOIC	16	SO		3.0	ChipSite		
82S129	82S129-SOIC	16	SO		3.0	PinSite	0302/0301	.300 SOIC
82S129	82S129-PLCC	20	PLCC		2.5	ChipSite		
82S129	82S129-PLCC	20	PLCC		3.0	PinSite	0201	
82S130	82S130	16	DIP		1.7	Site 48/40		
82S130	82S130-SOIC	16	SO		2.8	ChipSite		
82S130	82S130-SOIC	16	SO		3.0	PinSite	0302/0301	.300 SOIC
82S130	82S130-PLCC	20	PLCC		2.4	ChipSite		
82S130	82S130-PLCC	20	PLCC		3.0	PinSite	0201	
82S131	82S131	16	DIP		1.7	Site 48/40		
82S131	82S131-SOIC	16	SO		2.8	ChipSite		
82S131	82S131-SOIC	16	SO		3.0	PinSite	0302/0301	.300 SOIC
82S131	82S131-PLCC	20	PLCC		2.4	ChipSite		
82S131	82S131-PLCC	20	PLCC		3.0	PinSite	0201	
82S135	82S135	20	DIP		1.4	Site 48/40		
82S136	82S136	18	DIP		1.4	Site 48/40		
82S137	82S137	18	DIP		1.4	Site 48/40		
82S137	82S137-PLCC	20	PLCC		3.0	ChipSite		
82S137	82S137-PLCC	20	PLCC		3.0	PinSite	0201	
82S140	82S140	24	DIP		1.4	Site 48/40		
82S141	82S141	24	DIP		1.4	Site 48/40		
82S141	82S141-PLCC	28	PLCC		2.4	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Philips Semiconductor (continued)								
82S141	82S141-PLCC	28	PLCC		3.0	PinSite	0201	
82S146	82S146	20	DIP		1.4	Site 48/40		
82S147	82S147	20	DIP		1.4	Site 48/40		
82S147	82S147-PLCC	20	PLCC		2.4	ChipSite		
82S147	82S147-PLCC	20	PLCC		3.0	PinSite	0201	
82S153	82S153	20	DIP		4.1	Site 48/40		
82S153	82S153-PLCC	20	PLCC		4.1	ChipSite		
82S153	82S153-PLCC	20	PLCC		4.1	PinSite	0201	
82S180	82S180	24	DIP		1.4	Site 48/40		
82S181	82S181	24	DIP		1.4	Site 48/40		
82S181	82S181-PLCC	28	PLCC		2.4	ChipSite		
82S181	82S181-PLCC	28	PLCC		3.0	PinSite	0201	
82S182	82S182	24	DIP		1.4	Site 48/40		
82S183	82S183	24	DIP		1.4	Site 48/40		
82S183	82S183-PLCC	28	PLCC		2.5	ChipSite		
82S183	82S183-PLCC	28	PLCC		3.0	PinSite	0201	
82S184	82S184	18	DIP		1.4	Site 48/40		
82S185	82S185	18	DIP		1.4	Site 48/40		
82S185	82S185-PLCC	20	PLCC		3.0	ChipSite		
82S185	82S185-PLCC	20	PLCC		3.0	PinSite	0201	
82S190	82S190	24	DIP		1.4	Site 48/40		
82S191	82S191	24	DIP		1.4	Site 48/40		
82S191	82S191-PLCC	28	PLCC		2.4	ChipSite		
82S191	82S191-PLCC	28	PLCC		3.0	PinSite	0201	
82S23	82S23	16	DIP		1.6	Site 48/40		
82S23	82S23-SOIC	16	SO		1.4	ChipSite		
82S23	82S23-SOIC	16	SO		3.0	PinSite	0302/0301	.300 SOIC
82S23	82S23-PLCC	20	PLCC		1.6	ChipSite		
82S23	82S23-PLCC	20	PLCC		3.0	PinSite	0201	
82S2708	82S2708	24	DIP		1.4	Site 48/40		
82US123	82US123	16	DIP		2.6	Site 48/40		
82US123	82US123-PLCC	20	PLCC		2.6	ChipSite		
82US123	82US123-PLCC	20	PLCC		3.0	PinSite	0201	
82US23	82US23	16	DIP		2.8	Site 48/40		
82US23	82US23-SOIC	16	SO		3.0	ChipSite		
82US23	82US23-SOIC	16	SO		3.0	PinSite	0302/0301	.300 SOIC
82US23	82US23-PLCC	20	PLCC		2.6	ChipSite		
82US23	82US23-PLCC	20	PLCC		3.0	PinSite	0201	
87C054	87C054	42	DIP	131,140	4.0	PinSite	9901	0602
87C451	87C451-CLCC	68	JLCC	2,44	2.8	ChipSite		
87C451	87C451-CLCC	68	JLCC	2,44	3.0	PinSite	0201	
87C451	87C451-PLCC	68	PLCC	2	2.8	ChipSite		
87C451	87C451-PLCC	68	PLCC	2	3.0	PinSite	0201	
87C51	87C51	40	DIP	2	3.8	Site 48/40		
87C51	87C51-JLCC	44	JLCC	2,44	3.8	ChipSite		
87C51	87C51-JLCC	44	JLCC	2,44	3.8	PinSite	0201	
87C51	87C51-LCC	44	LCC	2,44	3.8	ChipSite		
87C51	87C51-LCC	44	LCC	2,44	3.8	PinSite	0202	
87C51	87C51-PLCC	44	PLCC	2	3.8	ChipSite		
87C51	87C51-PLCC	44	PLCC	2	3.8	PinSite	0201	
87C51FB	87C51FB	40	DIP	2	3.8	Site 48/40		
87C51FB	87C51FB-JLCC	44	JLCC	2	4.2	ChipSite		
87C51FB	87C51FB-JLCC	44	JLCC	2	4.2	PinSite	0201	
87C51FB	87C51FB-PLCC	44	PLCC	2	4.2	ChipSite		
87C51FB	87C51FB-PLCC	44	PLCC	2	4.2	PinSite	0201	
87C52	87C52	40	DIP		3.1	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Philips Semiconductor (continued)								
87C52	87C52-JLCC	44	JLCC		3.1	ChipSite		
87C52	87C52-JLCC	44	JLCC		3.1	PinSite	0201	
87C52	87C52-QFP	44	QFP		4.2	PinSite	9901	0508
87C524	87C524	40	DIP		3.8	Site 48/40		
87C524	87C524-PLCC	44	PLCC		3.9	ChipSite		
87C524	87C524-PLCC	44	PLCC		3.9	PinSite	0201	
87C528	87C528	40	DIP	180	4.0	Site 48/40		
87C528	87C528-JLCC	44	JLCC	180	4.0	ChipSite		
87C528	87C528-JLCC	44	JLCC	180	4.0	PinSite	0201	
87C528	87C528-LCC	44	LCC	180	4.0	ChipSite		
87C528	87C528-LCC	44	LCC	180	4.0	PinSite	0202	
87C528	87C528-PLCC	44	PLCC	180	4.0	ChipSite		
87C528	87C528-PLCC	44	PLCC	180	4.0	PinSite	0201	
87C528	87C528-QFP	44	QFP	180	4.0	PinSite	9901	0508
87C550	87C550	40	DIP		3.9	Site 48/40		
87C550(COM)	87C550-CLCC	44	JLCC	44	2.8	ChipSite		
87C550(COM)	87C550-CLCC	44	JLCC	44	3.0	PinSite	0201	
87C550(COM)	87C550-PLCC	44	PLCC	44	2.8	ChipSite		
87C550(COM)	87C550-PLCC	44	PLCC	44	3.0	PinSite	0201	
87C552	87C552-CLCC	68	JLCC	2,44	3.1	ChipSite		
87C552	87C552-CLCC	68	JLCC	2,44	3.1	PinSite	0201	
87C552	87C552-PLCC	68	PLCC	2,44	4.1	ChipSite		
87C552	87C552-PLCC	68	PLCC	2,44	4.1	PinSite	0201	
87C575	87C575	40	DIP	2	3.9	Site 48/40		
87C575	87C575-JLCC	44	JLCC	2	4.1	ChipSite		
87C575	87C575-JLCC	44	JLCC	2	4.1	PinSite	0201	
87C575	87C575-LCC	44	LCC	2	4.1	ChipSite		
87C575	87C575-LCC	44	LCC	2	4.1	PinSite	0202	
87C575	87C575-PLCC	44	PLCC	2	4.1	ChipSite		
87C575	87C575-PLCC	44	PLCC	2	4.1	PinSite	0201	
87C592	87C592-JLCC	68	JLCC	2	3.8	ChipSite		
87C592	87C592-JLCC	68	JLCC	2	3.8	PinSite	0201	
87C592	87C592-LCC	68	LCC	2	3.8	ChipSite		
87C592	87C592-LCC	68	LCC	2	3.8	PinSite	0202	
87C592	87C592-PLCC	68	PLCC	2	3.8	ChipSite		
87C592	87C592-PLCC	68	PLCC	2	3.8	PinSite	0201	
87C652	87C652	40	DIP	2	3.7	Site 48/40		
87C652	87C652-JLCC	44	JLCC	2	4.0	ChipSite		
87C652	87C652-JLCC	44	JLCC	2	4.0	PinSite	0201	
87C652	87C652-LCC	44	LCC	2	3.7	ChipSite		
87C652	87C652-LCC	44	LCC	2	3.7	PinSite	0202	
87C652	87C652-PLCC	44	PLCC	2	4.0	ChipSite		
87C652	87C652-PLCC	44	PLCC	2	4.0	PinSite	0201	
87C654	87C654	40	DIP	2	3.7	Site 48/40		
87C654	87C654-LCC	44	PLCC	2	3.7	ChipSite		
87C654	87C654-LCC	44	PLCC	2	3.7	PinSite	0201	
87C654	87C654-QFP	44	QFP		4.2	PinSite	9901	0508
87C751	87C751	24	DIP	29	2.3	Site 48/40		
87C751	87C751-PLCC	28	PLCC	29	2.6	ChipSite		
87C751	87C751-PLCC	28	PLCC	29	3.0	PinSite	0201	
87C752	87C752	28	DIP	29	2.6	Site 48/40		
87C752	87C752-PLCC	28	PLCC	29	2.8	ChipSite		
87C752	87C752-PLCC	28	PLCC	29	3.0	PinSite	0201	
CK2605	CK2605	20	DIP		4.0	Site 48/40		
PHD16N8	PHD16N8	20	DIP		3.0	Site 48/40		
PHD16N8	PHD16N8-PLCC	20	PLCC		3.0	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Philips Semiconductor (continued)								
PHD16N8	PHD16N8-PLCC	20	PLCC		3.0	PinSite	0201	
PHD48N22	PHD48N22-PL*	68	PLCC		3.0	PinSite	0201	
PHD48N22	PHD48N22-PL*	68	PLCC	42	3.0	Site 48/40		
PL22V10	PL22V10	24	DIP	33	3.6	Site 48/40		
PL22V10	PL22V10-SOIC	24	SO		4.1	PinSite	0302/0301	.300 SOIC
PL22V10	PL22V10-PLCC	28	PLCC	33	3.6	ChipSite		
PL22V10	PL22V10-PLCC	28	PLCC	33	3.6	PinSite	0201	
PLC153	PLC153	20	DIP		2.1	Site 48/40		
PLC153	PLC153-PLCC	20	PLCC		2.4	ChipSite		
PLC153	PLC153-PLCC	20	PLCC		3.0	PinSite	0201	
PLC16V8	PLC16V8	20	DIP		2.1	Site 48/40		
PLC16V8	PLC16V8-PLCC	20	PLCC		2.4	ChipSite		
PLC16V8	PLC16V8-PLCC	20	PLCC		3.0	PinSite	0201	
PLC18V8Z	PLC18V8Z	20	DIP		2.6	Site 48/40		
PLC18V8Z	PLC18V8ZPLCC	20	PLCC		2.8	ChipSite		
PLC18V8Z	PLC18V8ZPLCC	20	PLCC		3.0	PinSite	0201	
PLC18V8Z	PLC18V8Z-SO	20	SO		4.1	PinSite	0302/0301	.300 SOIC
PLC20V8	PLC20V8	24	DIP		2.1	Site 48/40		
PLC20V8	PLC20V8-PLCC	28	PLCC		2.4	ChipSite		
PLC20V8	PLC20V8-PLCC	28	PLCC		3.0	PinSite	0201	
PLC415	PLC415	28	DIP		2.6	Site 48/40		
PLC415	PLC415-PLCC	28	PLCC		2.7	ChipSite		
PLC415	PLC415-PLCC	28	PLCC		3.0	PinSite	0201	
PLC42VA12	PLC42VA12	24	DIP	33	3.5	Site 48/40		
PLC42VA12	PLC42VA12-PL	28	PLCC	33	3.5	ChipSite		
PLC42VA12	PLC42VA12-PL	28	PLCC	33	3.5	PinSite	0201	
PLC473	PLC473	24	DIP		2.1	Site 48/40		
PLC473	PLC473-PLCC	28	PLCC		2.4	ChipSite		
PLC473	PLC473-PLCC	28	PLCC		3.0	PinSite	0201	
PLHS153	PLHS153	20	DIP		2.1	Site 48/40		
PLHS153	PLHS153-PLCC	20	PLCC		2.5	ChipSite		
PLHS153	PLHS153-PLCC	20	PLCC		3.0	PinSite	0201	
PLHS16L8	PLHS16L8	20	DIP		2.1	Site 48/40		
PLHS16L8	PLHS16L8-PLC	20	PLCC		2.5	ChipSite		
PLHS16L8	PLHS16L8-PLC	20	PLCC		3.0	PinSite	0201	
PLHS18P8	PLHS18P8/A	20	DIP		2.1	Site 48/40		
PLHS18P8	PLHS18P8PLCC	20	PLCC		2.1	ChipSite		
PLHS18P8	PLHS18P8PLCC	20	PLCC		3.0	PinSite	0201	
PLHS473	PLHS473	24	DIP		2.2	Site 48/40		
PLHS473	PLHS473-PLCC	28	PLCC		2.2	ChipSite		
PLHS473	PLHS473-PLCC	28	PLCC		3.0	PinSite	0201	
PLHS501	PLHS501-PLCC	52	PLCC		1.7	ChipSite		
PLHS501	PLHS501-PLCC	52	PLCC		3.0	PinSite	0201	
PLHS502	PLHS502PLCC*	68	PLCC		3.2	PinSite	0201	
PLHS502	PLHS502PLCC*	68	PLCC	41	2.8	Site 48/40		
PLHS601	PLHS601PLCC*	68	PLCC		3.1	PinSite	0201	
PLHS601	PLHS601PLCC*	68	PLCC	41	3.1	Site 48/40		
PLS100	PLS100	28	DIP		2.5	Site 48/40		
PLS100	PLS100-PLCC	28	PLCC		2.5	ChipSite		
PLS100	PLS100-PLCC	28	PLCC		3.0	PinSite	0201	
PLS101	PLS101	28	DIP		2.5	Site 48/40		
PLS101	PLS101-PLCC	28	PLCC		2.5	ChipSite		
PLS101	PLS101-PLCC	28	PLCC		3.0	PinSite	0201	
PLS102	PLS102	28	DIP		1.5	Site 48/40		
PLS103	PLS103	28	DIP		1.5	Site 48/40		
PLS103	PLS103-PLCC	28	PLCC		2.6	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Philips Semiconductor (continued)								
PLS103	PLS103-PLCC	28	PLCC		3.0	PinSite	0201	
PLS105	PLS105/A	28	DIP		1.5	Site 48/40		
PLS105	PLS105/A-PLC	28	PLCC		1.5	ChipSite		
PLS105	PLS105/A-PLC	28	PLCC		3.0	PinSite	0201	
PLS151	PLS151	20	DIP		4.1	Site 48/40		
PLS151	PLS151-PLCC	20	PLCC		4.1	ChipSite		
PLS151	PLS151-PLCC	20	PLCC		4.1	PinSite	0201	
PLS152	PLS152	20	DIP		4.1	Site 48/40		
PLS152	PLS152-PLCC	20	PLCC		4.1	ChipSite		
PLS152	PLS152-PLCC	20	PLCC		4.1	PinSite	0201	
PLS153	PLS153/A	20	DIP		4.1	Site 48/40		
PLS153	PLS153/A-PLC	20	PLCC		4.1	ChipSite		
PLS153	PLS153/A-PLC	20	PLCC		4.1	PinSite	0201	
PLS155	PLS155	20	DIP		1.5	Site 48/40		
PLS155	PLS155-PLCC	20	PLCC		1.5	ChipSite		
PLS155	PLS155-PLCC	20	PLCC		3.0	PinSite	0201	
PLS157	PLS157	20	DIP		1.5	Site 48/40		
PLS157	PLS157-PLCC	20	PLCC		1.5	ChipSite		
PLS157	PLS157-PLCC	20	PLCC		3.0	PinSite	0201	
PLS159	PLS159	20	DIP		1.5	Site 48/40		
PLS159	PLS159-PLCC	20	PLCC		1.5	ChipSite		
PLS159	PLS159-PLCC	20	PLCC		3.0	PinSite	0201	
PLS159A	PLS159A	20	DIP		4.1	Site 48/40		
PLS159A	PLS159A-PLCC	20	PLCC		4.1	ChipSite		
PLS159A	PLS159A-PLCC	20	PLCC		4.1	PinSite	0201	
PLS161	PLS161	24	DIP		2.5	Site 48/40		
PLS162	PLS162	24	DIP		1.5	Site 48/40		
PLS163	PLS163	24	DIP		1.5	Site 48/40		
PLS167	PLS167/A	24	DIP		1.5	Site 48/40		
PLS167	PLS167/A-LCC	28	PLCC		1.5	ChipSite		
PLS167	PLS167/A-LCC	28	PLCC		3.0	PinSite	0201	
PLS168	PLS168/A	24	DIP		1.5	Site 48/40		
PLS168	PLS168/A-LCC	28	PLCC		1.5	ChipSite		
PLS168	PLS168/A-LCC	28	PLCC		3.0	PinSite	0201	
PLS173	PLS173	24	DIP		4.1	Site 48/40		
PLS173	PLS173-PLCC	28	PLCC		4.1	ChipSite		
PLS173	PLS173-PLCC	28	PLCC		4.1	PinSite	0201	
PLS179	PLS179	24	DIP		4.1	Site 48/40		
PLS179	PLS179-PLCC	28	PLCC		4.1	ChipSite		
PLS179	PLS179-PLCC	28	PLCC		4.1	PinSite	0201	
PLUS105	PLUS105	28	DIP		4.2	Site 48/40		
PLUS105	PLUS105-PLCC	28	PLCC		4.2	ChipSite		
PLUS105	PLUS105-PLCC	28	PLCC		4.2	PinSite	0201	
PLUS153	PLUS153	20	DIP		4.1	Site 48/40		
PLUS153	PLUS153-PLCC	20	PLCC		4.1	ChipSite		
PLUS153	PLUS153-PLCC	20	PLCC		4.1	PinSite	0201	
PLUS16L8	PLUS16L8	20	DIP		4.1	Site 48/40		
PLUS16L8	PLUS16L8PLCC	20	PLCC		4.1	ChipSite		
PLUS16L8	PLUS16L8PLCC	20	PLCC		4.1	PinSite	0201	
PLUS16R4	PLUS16R4	20	DIP		4.1	Site 48/40		
PLUS16R4	PLUS16R4PLCC	20	PLCC		4.1	ChipSite		
PLUS16R4	PLUS16R4PLCC	20	PLCC		4.1	PinSite	0201	
PLUS16R6	PLUS16R6	20	DIP		4.1	Site 48/40		
PLUS16R6	PLUS16R6PLCC	20	PLCC		4.1	ChipSite		
PLUS16R6	PLUS16R6PLCC	20	PLCC		4.1	PinSite	0201	
PLUS16R8	PLUS16R8	20	DIP		4.1	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Philips Semiconductor (continued)								
PLUS16R8	PLUS16R8PLCC	20	PLCC		4.1	ChipSite		
PLUS16R8	PLUS16R8PLCC	20	PLCC		4.1	PinSite	0201	
PLUS173	PLUS173	24	DIP		4.1	Site 48/40		
PLUS173	PLUS173-PLCC	28	PLCC		4.1	ChipSite		
PLUS173	PLUS173-PLCC	28	PLCC		4.1	PinSite	0201	
PLUS20L8	PLUS20L8	24	DIP		4.1	Site 48/40		
PLUS20L8	PLUS20L8-FN	28	PLCC		4.1	ChipSite		
PLUS20L8	PLUS20L8-FN	28	PLCC		4.1	PinSite	0201	
PLUS20R4	PLUS20R4	24	DIP		4.1	Site 48/40		
PLUS20R4	PLUS20R4-FN	28	PLCC		4.1	ChipSite		
PLUS20R4	PLUS20R4-FN	28	PLCC		4.1	PinSite	0201	
PLUS20R6	PLUS20R6	24	DIP		4.1	Site 48/40		
PLUS20R6	PLUS20R6-FN	28	PLCC		4.1	ChipSite		
PLUS20R6	PLUS20R6-FN	28	PLCC		4.1	PinSite	0201	
PLUS20R8	PLUS20R8	24	DIP		4.1	Site 48/40		
PLUS20R8	PLUS20R8-FN	28	PLCC		4.1	ChipSite		
PLUS20R8	PLUS20R8-FN	28	PLCC		4.1	PinSite	0201	
PLUS405	PLUS405	28	DIP		4.2	Site 48/40		
PLUS405	PLUS405-PLCC	28	PLCC		4.2	ChipSite		
PLUS405	PLUS405-PLCC	28	PLCC		4.2	PinSite	0201	
PLV2500	2500	40	DIP		3.6	Site 48/40		
PLV5000	5000-PLCC	68	PLCC		3.6	PinSite	0201	
PLV750	750	24	DIP		3.6	Site 48/40		
PLV750	750-PLCC	28	PLCC		3.6	ChipSite		
PLV750	750-PLCC	28	PLCC		3.6	PinSite	0201	
PML2552	PML2552-JLCC	68	JLCC		3.2	PinSite	0201	
PML2552	PML2552PLCC*	68	PLCC		3.0	PinSite	0201	
PML2552	PML2552PLCC*	68	PLCC	42,44	2.8	Site 48/40		
PML2852	PML2852JLCC*	84	JLCC		3.5	PinSite	0201	
PML2852	PML2852JLCC*	84	JLCC	128	3.8	Site 48/40		
PML2852	PML2852PLCC*	84	PLCC		3.5	PinSite	0201	
PML2852	PML2852PLCC*	84	PLCC	128	3.8	Site 48/40		
Plus Logic								
2020	2020-JLCC	84	JLCC	94	3.4	PinSite	0201	
2020	2020-PLCC	84	PLCC	94	3.4	PinSite	0201	
QuickLogic Corporation								
QL12X16-0PL68C	QL12X16-68	68	PLCC		4.2	PinSite	0201	
QL12X16-0PL84C	QL12X16-84	84	PLCC		4.2	PinSite	0201	
QL8X12-0PL44C	QL8X12A-44	44	PLCC		4.2	PinSite	0201	
QL8X12A-0PL68C	QL8X12A-68	68	PLCC		4.1	PinSite	0201	
Raytheon								
29613/A	29613	16	DIP		2.1	Site 48/40		
29621/A	29621	20	DIP		2.1	Site 48/40		
29623/A	29623	20	DIP		2.1	Site 48/40		
29631/A	29631	24	DIP		2.1	Site 48/40		
29633/A	29633	24	DIP		2.1	Site 48/40		
29651/A	29651	18	DIP		2.1	Site 48/40		
29653/A	29653	18	DIP		2.1	Site 48/40		
29671/A	29671	24	DIP		2.1	Site 48/40		
29671/A	29671-LCC	28	LCC	44	2.6	ChipSite		
29671/A	29671-LCC	28	LCC	44	3.0	PinSite	0202	
29671SM	29671SM	24	DIP		2.1	Site 48/40		
29673	29673	24	DIP		2.1	Site 48/40		
29673SM	29673SM	24	DIP		2.1	Site 48/40		
29681/A	29681	24	DIP		2.1	Site 48/40		
29681SM	29681SM	24	DIP		2.1	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Cypress Semiconductor, Inc. (continued)								
7C291	7C291-PLCC	28	PLCC		3.0	PinSite	0201	
7C291A	7C291A	24	DIP		2.3	Site 48/40		
7C291A	7C291A-SOIC	24	SO		3.4	ChipSite		
7C291A	7C291A-SOIC	24	SO		3.4	PinSite	0302/0301	.300 SOIC
7C291A	7C291A-PLCC	28	PLCC		3.6	ChipSite		
7C291A	7C291A-PLCC	28	PLCC		3.6	PinSite	0201	
7C292	7C292	24	DIP		2.2	Site 48/40		
7C292A	7C292A	24	DIP		2.3	Site 48/40		
7C293A	7C293A	24	DIP		2.8	Site 48/40		
7C330	7C330	28	DIP		2.8	Site 48/40		
7C330	7C330-JLCC	28	JLCC	28	3.2	PinSite	0201	
7C330	7C330-LCC	28	LCC	28,44	3.2	PinSite	0202	
7C330	7C330-PLCC	28	PLCC	28	3.2	PinSite	0201	
7C331	7C331	28	DIP		2.8	Site 48/40		
7C331	7C331-LCC	28	LCC	28,44	3.2	PinSite	0202	
7C331	7C331-PLCC	28	PLCC	28	3.2	PinSite	0201	
7C331	7C331-JLCC	32	JLCC	28	3.6	PinSite	0201	
7C332	7C332	28	DIP		2.8	Site 48/40		
7C332	7C332-JLCC	28	JLCC		3.5	PinSite	0201	
7C332	7C332-LCC	28	LCC		3.5	PinSite	0202	
7C332	7C332-PLCC	28	PLCC		3.5	PinSite	0201	
7C335	7C335	28	DIP		4.0	Site 48		
7C335	7C335-PLCC	28	PLCC		4.2	PinSite	0201	
7C341	7C341-JLCC	84	JLCC	54	4.2	PinSite	0201	
7C341	7C341-PGA	84	PGA	54	4.2	PinSite	9901	0401
7C341	7C341-PLCC	84	PLCC	54	4.2	PinSite	0201	
7C342	7C342-JLCC	68	JLCC	54	3.8	PinSite	0201	
7C342	7C342-PGA	68	PGA	54	3.8	PinSite	0402/0401	
7C342	7C342-PLCC	68	PLCC	54	3.8	PinSite	0201	
7C342	7C342-QFP	68	QFPCAR	54	3.8	PinSite	9901	0517
7C343	7C343-JLCC	44	JLCC	54	3.3	PinSite	0201	
7C343	7C343-PLCC	44	PLCC	54	4.1	PinSite	0201	
7C344	7C344	28	DIP	55	3.9	Site 48		
7C344	7C344-JLCC	28	JLCC	55	3.9	PinSite	0201	
7C344	7C344-PLCC	28	PLCC	55	3.9	PinSite	0201	
7C361	7C361	28	DIP		3.6	Site 48		
7C361	7C361-JLCC	28	JLCC		3.7	PinSite	0201	
CG7C324	CG7C324-PLCC	28	PLCC		4.0	ChipSite		
CG7C324	CG7C324-PLCC	28	PLCC		4.0	PinSite	0201	
CY7C381-0JC	7C381-PLCC	44	PLCC		4.2	PinSite	0201	
CY7C382-0JC	7C382-PLCC	68	PLCC		4.2	PinSite	0201	
CY7C383-0JC	7C383-PLCC	68	PLCC		4.2	PinSite	0201	
CY7C384-0JC	7C384-PLCC	84	PLCC		4.2	PinSite	0201	
Dallas Semiconductor								
1235Y	1235Y	28	DIP		4.0	Site 48/40		
1245Y	1245Y	32	DIP		4.0	Site 48/40		
Exel Microelectronics, Inc.								
2804	2804	24	DIP		2.8	SetSite		
2804	2804	24	DIP		2.1	Site 48/40		
2804A	2804A	24	DIP		3.2	SetSite		
2804A	2804A	24	DIP		3.2	Site 48/40		
2816A	2816A	24	DIP		2.1	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Exel Microelectronics, Inc. (continued)								
2816A	2816A	24	DIP		2.1	Site 48/40		
2816A	2816A-PLCC	32	PLCC		3.2	ChipSite		
2816A	2816A-PLCC	32	PLCC		3.2	PinSite	0201	
2864A	2864A	28	DIP		2.5	SetSite		
2864A	2864A	28	DIP		2.5	Site 48/40		
2864A	2864A-PLCC	32	PLCC		3.3	ChipSite		
2864A	2864A-PLCC	32	PLCC		3.3	PinSite	0201	
2865A	2865A	28	DIP		2.5	SetSite		
2865A	2865A	28	DIP		2.5	Site 48/40		
2865A	2865A-PLCC	32	PLCC		3.3	PinSite	0201	
28C16A	28C16A	24	DIP		3.5	Site 48/40		
46C15	46C15	24	DIP	31	2.0	SetSite		
46C15	46C15	24	DIP	31	1.4	Site 48/40		
46C16	46C16	24	DIP	31	2.5	SetSite		
46C16	46C16	24	DIP	31	2.5	Site 48/40		
78C800	78C800	24	DIP		2.1	Site 48/40		
78C800	78C800-PLCC	28	PLCC		2.1	ChipSite		
78C800	78C800-PLCC	28	PLCC		3.0	PinSite	0201	
93C46	93C46	8	DIP		3.2	Site 48/40		
Fairchild Semiconductor Corp.								
16L8	16L8	20	DIP		2.0	Site 48/40		
16P8	16P8A/B	20	DIP		2.0	Site 48/40		
16R4	16R4	20	DIP		2.0	Site 48/40		
16R6	16R6	20	DIP		2.0	Site 48/40		
16R8	16R8	20	DIP		2.0	Site 48/40		
16RP4	16RP4A/B	20	DIP		2.0	Site 48/40		
16RP6	16RP6A/B	20	DIP		2.0	Site 48/40		
16RP8	16RP8A/B	20	DIP		2.0	Site 48/40		
2708	2708	24	DIP		2.0	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
93438	93438	24	DIP		3.0	Site 48/40		
93448	93448	24	DIP		3.0	Site 48/40		
93451	93451	24	DIP		2.2	Site 48/40		
93510	93510	24	DIP		2.2	Site 48/40		
93511	93511	24	DIP		2.2	Site 48/40		
93Z450	93Z450	24	DIP		2.2	Site 48/40		
93Z451	93Z451	24	DIP		1.0	Site 48/40		
93Z458	93Z458	28	DIP		2.0	Site 48/40		
93Z459	93Z459	28	DIP		2.0	Site 48/40		
93Z510	93Z510	24	DIP		1.6	Site 48/40		
93Z511	93Z511	24	DIP		1.0	Site 48/40		
93Z564	93Z564	24	DIP		2.2	Site 48/40		
93Z565	93Z565	24	DIP		2.2	Site 48/40		
93Z565	93Z565-LCC	24	LCC	44	2.2	ChipSite		
93Z565	93Z565-LCC	24	LCC	44	3.0	PinSite	0202	
93Z665	93Z665	24	DIP		2.2	Site 48/40		
93Z667	93Z667	24	DIP		2.2	Site 48/40		
Fujitsu Microelectronics, Inc.								
2212	2212	18	DIP		4.1	Site 48		
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		2.0	Site 48/40		
2716	2716	24	DIP		2.0	SetSite		
2716	2716	24	DIP		2.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Fujitsu Microelectronics, Inc. (continued)								
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		
27C1000	27C1000	32	DIP		2.0	SetSite		
27C1000	27C1000	32	DIP		2.0	Site 48/40		
27C1000	27C1000-JLCC	32	JLCC		3.8	ChipSite		
27C1000	27C1000-JLCC	32	JLCC		3.8	PinSite	0201	
27C1000	27C1000-SOIC	32	SO		3.9	PinSite	0302	.450 SOIC
27C1000A	27C1000A	32	DIP		3.8	Site 48/40		
27C1001	27C1001	32	DIP		2.0	SetSite		
27C1001	27C1001	32	DIP		2.0	Site 48/40		
27C1001	27C1001-JLCC	32	JLCC		3.0	ChipSite		
27C1001	27C1001-JLCC	32	JLCC		3.0	PinSite	0201	
27C1001	27C1001-SOIC	32	SO		3.9	PinSite	0302	.450 SOIC
27C1001A	27C1001A	32	DIP		3.8	Site 48/40		
27C1024	27C1024	40	DIP		2.0	SetSite		
27C1024	27C1024	40	DIP		2.1	Site 48/40		
27C1024	27C1024-LCC	44	LCC	44	2.8	ChipSite		
27C1024	27C1024-LCC	44	LCC	44	3.0	PinSite	0202	
27C1024	27C1024-PLCC	44	PLCC		3.8	ChipSite		
27C1024	27C1024-PLCC	44	PLCC		3.8	PinSite	0201	
27C1024A	27C1024A	40	DIP		3.8	Site 48/40		
27C1028	27C1028	28	DIP		2.3	Site 48/40		
27C1028	27C1028-LCC	32	LCC	44	2.8	ChipSite		
27C1028	27C1028-LCC	32	LCC	44	3.0	PinSite	0202	
27C128	27C128	28	DIP		2.0	SetSite		
27C128	27C128	28	DIP		2.0	Site 48/40		
27C128	27C128-LCC	32	LCC	44	2.7	ChipSite		
27C128	27C128-LCC	32	LCC	44	3.0	PinSite	0202	
27C2000	27C2000	32	DIP		3.8	Site 48/40		
27C2001	27C2001	32	DIP		3.8	Site 48/40		
27C2048	27C2048	40	DIP		3.8	Site 48/40		
27C256	27C256	28	DIP		2.0	SetSite		
27C256	27C256	28	DIP		2.0	Site 48/40		
27C256A	27C256A	28	DIP		2.1	SetSite		
27C256A	27C256A	28	DIP		2.1	Site 48/40		
27C256A	27C256A-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
27C256A	27C256A-LCC	32	LCC	44	2.8	ChipSite		
27C256A	27C256A-LCC	32	LCC	44	3.0	PinSite	0202	
27C256H	27C256H	28	DIP		2.1	SetSite		
27C256H	27C256H	28	DIP		2.1	Site 48/40		
27C32A	27C32A	24	DIP		2.0	Site 48/40		
27C4000	27C4000	32	DIP		3.4	Site 48/40		
27C4001	27C4001	32	DIP		3.4	Site 48/40		
27C4096	27C4096	40	DIP		3.4	Site 48/40		
27C512	27C512	28	DIP		2.0	SetSite		
27C512	27C512	28	DIP		2.0	Site 48/40		
27C512	27C512HW-LCC	32	LCC	196	4.1	ChipSite		
27C512	27C512HW-LCC	32	LCC	196	4.1	PinSite	0202	
27C512	27C512-PLCC	32	PLCC		2.0	ChipSite		
27C512	27C512-PLCC	32	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Fujitsu Microelectronics, Inc. (continued)								
27C512HW	27C512HW	28	DIP	195	4.1	Site 48/40		
27C64	27C64	28	DIP		2.0	SetSite		
27C64	27C64	28	DIP		2.0	Site 48/40		
27C64	27C64-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
27C64	27C64-LCC	32	LCC	44	3.0	ChipSite		
27C64	27C64-LCC	32	LCC	44	3.0	PinSite	0202	
28C64	28C64	28	DIP		2.0	SetSite		
28C64	28C64	28	DIP		2.0	Site 48/40		
28C65	28C65	28	DIP		2.0	SetSite		
28C65	28C65	28	DIP		2.0	Site 48/40		
28F010	28F010	32	DIP		4.2	Site 48/40		
7051	7051	16	DIP		1.7	Site 48/40		
7052	7052	16	DIP		3.6	Site 48/40		
7056	7056	16	DIP		1.7	Site 48/40		
7111	7111	16	DIP		2.2	Site 48/40		
7112	7112	16	DIP		2.2	Site 48/40		
7112	7112-LCC	20	LCC	44	3.1	ChipSite		
7112	7112-LCC	20	LCC	44	3.1	PinSite	0202	
7113/L	7113/L	16	DIP		2.2	Site 48/40		
7114/L	7114/L	16	DIP		2.2	Site 48/40		
7115	7115	16	DIP		2.2	Site 48/40		
7116	7116	16	DIP		2.2	Site 48/40		
7117	7117	20	DIP		2.2	Site 48/40		
7118	7118	20	DIP		2.2	Site 48/40		
7118	7118-SOIC	20	SO		3.1	ChipSite		
7118	7118-SOIC	20	SO		3.1	PinSite	0302/0301	.300 SOIC
7121	7121	18	DIP		2.2	Site 48/40		
7122	7122	18	DIP		2.2	Site 48/40		
7123	7123	20	DIP		2.2	Site 48/40		
7124	7124	20	DIP		2.2	Site 48/40		
7127	7127	18	DIP		2.2	Site 48/40		
7128	7128	18	DIP		2.2	Site 48/40		
7129	7129	22	DIP		2.2	Site 48/40		
7130	7130	22	DIP		2.2	Site 48/40		
7131	7131	24	DIP		2.2	Site 48/40		
7132	7132	24	DIP		2.2	Site 48/40		
7133	7133	20	DIP		2.2	Site 48/40		
7134	7134	20	DIP		2.2	Site 48/40		
7135	7135	22	DIP		2.2	Site 48/40		
7136	7136	22	DIP		2.2	Site 48/40		
7137	7137	24	DIP		2.2	Site 48/40		
7138	7138	24	DIP		2.2	Site 48/40		
7138	7138-LCC	28	LCC	44	2.8	ChipSite		
7138	7138-LCC	28	LCC	44	3.0	PinSite	0202	
7141	7141	24	DIP		2.2	Site 48/40		
7142	7142	24	DIP		2.2	Site 48/40		
7143	7143	24	DIP		2.2	Site 48/40		
7144	7144	24	DIP		2.2	Site 48/40		
7151	7151	20	DIP		2.2	Site 48/40		
7152	7152	20	DIP		2.2	Site 48/40		
7154	7154	24	DIP		3.4	Site 48/40		
71A38	71A38	24	DIP		4.1	Site 48/40		
71C256	71C256	28	DIP		4.1	Site 48/40		
71C44	71C44	24	DIP		4.1	Site 48/40		
71C46	71C46	28	DIP		4.1	Site 48/40		
7225RA/RS	7225RA/RS	24	DIP		2.5	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Fujitsu Microelectronics, Inc. (continued)								
7226RA/RS	7226RA/RS	24	DIP		2.5	Site 48/40		
7231RA/RS	7231RA/RS	24	DIP	1	2.5	Site 48/40		
7232RA/RS	7232RA/RS	24	DIP	1	2.5	Site 48/40		
7237RA/RS	7237RA/RS	24	DIP	1	2.5	Site 48/40		
7238RA/RS	7238RA/RS	24	DIP	1	2.5	Site 48/40		
7241RA/RS	7241RS	24	DIP	1	2.5	Site 48/40		
7242RA/RS	7242RS	24	DIP	1	2.5	Site 48/40		
8516	8516	24	DIP		2.8	SetSite		
8516	8516	24	DIP		2.0	Site 48/40		
8518	8518	24	DIP		2.0	Site 48/40		
8532	8532	24	DIP		2.0	Site 48/40		
8541P	8541P	8	DIP		3.0	Site 48/40		
8541P	8541P-SOIC	8	SO		4.1	PinSite	0302/0301	.220 SOIC
8742H/N	8742H/N	40	DIP		1.5	Site 48/40		
89P625	89P625QFP*	64	QFP	199	4.1	Site 48/40		
89P625	89P625SDIP*	64	SDIP	198	4.1	Site 48/40		
98A608A	98A608A*	68	CARD	91	3.3	Site 48/40		
98A609A	98A609A*	68	CARD	91	3.3	Site 48/40		
98A610A	98A610A*	68	CARD	91	3.2	Site 48/40		
MB98A6070	98A6070*	68	CARD	117	3.4	Site 48/40		
MB98A6080	98A6080*	68	CARD	117	3.4	Site 48/40		
MB98A6090	98A6090*	68	CARD	117	3.4	Site 48/40		
MB98A6100	98A6100*	68	CARD	117	3.4	Site 48/40		
Goldstar Co. Ltd.								
57HC64	57HC64	24	DIP		2.2	SetSite		
57HC64	57HC64	24	DIP		2.2	Site 48/40		
Harris Corporation								
6617	6617	24	DIP		3.9	Site 48/40		
6617RH	6617RH	24	DIP		3.9	Site 48/40		
6641	6641	24	DIP		3.9	Site 48/40		
6642	6642	24	DIP		4.0	Site 48/40		
6642/883	6642-LCC	28	LCC	44	4.0	PinSite	0202	
7602	7602	16	DIP		2.2	Site 48/40		
7603	7603	16	DIP		2.2	Site 48/40		
7610	7610	16	DIP		2.2	Site 48/40		
7611	7611	16	DIP		2.2	Site 48/40		
76161	76161	24	DIP		1.4	Site 48/40		
76165	76165	20	DIP		2.2	Site 48/40		
7620	7620/A	16	DIP		2.2	Site 48/40		
7621	7621/A	16	DIP		2.2	Site 48/40		
76321	76321	24	DIP		2.2	Site 48/40		
7640	7640	24	DIP		2.2	Site 48/40		
7641	7641	24	DIP		2.2	Site 48/40		
7642	7642/A	18	DIP		2.2	Site 48/40		
7643	7643/A	18	DIP		2.2	Site 48/40		
7649	7649	20	DIP		2.2	Site 48/40		
76641	76641	24	DIP		2.2	Site 48/40		
7681	7681	24	DIP		2.2	Site 48/40		
Hitachi, Ltd.								
27128A	27128A	28	DIP		2.1	SetSite		
27128A	27128A	28	DIP		2.1	Site 48/40		
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
27512	27512	28	DIP		2.0	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Hitachi, Ltd. (continued)								
27512	27512	28	DIP		2.0	Site 48/40		
27C101	27C101	32	DIP		2.8	SetSite		
27C101	27C101	32	DIP		2.8	Site 48/40		
27C101A	27C101A	32	DIP		3.1	Site 48/40		
27C101A	27C101A-SOIC	32	SO		4.1	PinSite	0302	.450 SOIC
27C1024	27C1024	40	DIP		2.8	SetSite		
27C1024	27C1024	40	DIP		2.8	Site 48/40		
27C1024	27C1024-JLCC	44	JLCC		3.0	ChipSite		
27C1024	27C1024-JLCC	44	JLCC		3.0	PinSite	0201	
27C1024	27C1024-PLCC	44	PLCC		4.1	ChipSite		
27C1024	27C1024-PLCC	44	PLCC		4.1	PinSite	0201	
27C256	27C256	28	DIP		2.1	SetSite		
27C256	27C256	28	DIP		2.1	Site 48/40		
27C256	27C256-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
27C256A	27C256A	28	DIP		4.1	Site 48/40		
27C256H	27C256H	28	DIP		2.1	SetSite		
27C256H	27C256H	28	DIP		2.1	Site 48/40		
27C301	27C301	32	DIP		2.8	SetSite		
27C301	27C301	32	DIP		2.8	Site 48/40		
27C301A	27C301A	32	DIP		3.1	Site 48/40		
27C4000	27C4000	40	DIP		4.2	Site 48/40		
27C4001	27C4001	32	DIP		3.4	Site 48/40		
27C4096	27C4096	40	DIP		4.0	SetSite		
27C4096	27C4096	40	DIP		3.0	Site 48/40		
27C4096	27C4096-JLCC	44	JLCC		3.4	ChipSite		
27C4096	27C4096-JLCC	44	JLCC		3.4	PinSite	0201	
27C4096	27C4096-PLCC	44	PLCC		3.4	ChipSite		
27C4096	27C4096-PLCC	44	PLCC		3.4	PinSite	0201	
27C512A	27C512A	28	DIP		4.1	Site 48/40		
27C64	27C64	28	DIP		2.0	SetSite		
27C64	27C64	28	DIP		2.0	Site 48/40		
28F101	28F101	32	DIP		4.0	Site 48/40		
29C101	29C101	32	DIP		4.0	Site 48/40		
29C101B	29C101B	32	DIP		4.0	Site 48/40		
4074019	4074019SDIP*	64	SDIP	83	3.2	Site 48/40		
4074224	4074224SDIP*	28	SDIP	200	4.1	Site 48/40		
4074274	4074274SDIP*	28	SDIP	200	4.1	Site 48		
4074608FS	4074608FQFP*	80	QFP	63	3.2	Site 48/40		
4074608H	4074608HQFP*	80	QFP	104	3.3	Site 48/40		
4074709	4074709SDIP*	64	SDIP	64	3.2	Site 48/40		
4074729	4074729*	64	SDIP	103	3.3	Site 48/40		
4074808FS	4074808FQFP*	80	QFP	63	3.2	Site 48/40		
4074808H	4074808HQFP*	80	QFP	104	3.3	Site 48/40		
462532	462532	24	DIP		2.0	SetSite		
462532	462532	24	DIP		2.0	Site 48/40		
462716	462716	24	DIP		2.0	SetSite		
462716	462716	24	DIP		2.0	Site 48/40		
462732	462732	24	DIP		2.0	SetSite		
462732	462732	24	DIP		2.0	Site 48/40		
48016	48016	24	DIP		2.0	SetSite		
48016	48016	24	DIP		2.0	Site 48/40		
4827128	4827128	28	DIP		2.0	SetSite		
4827128	4827128	28	DIP		2.0	Site 48/40		
482732A	482732A	24	DIP		2.0	SetSite		
482732A	482732A	24	DIP		2.0	Site 48/40		
482764	482764	28	DIP		2.0	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Hitachi, Ltd. (continued)								
482764	482764	28	DIP		2.0	Site 48/40		
58064	58064	28	DIP		2.0	SetSite		
58064	58064	28	DIP		2.0	Site 48/40		
58C1001	58C1001	32	DIP		4.0	Site 48/40		
58C256	58C256	28	DIP		3.1	Site 48/40		
58C256	58C256-SOIC	28	SO		4.2	PinSite	0302/0301	.350 SOIC
58C65	58C65P	28	DIP		2.5	SetSite		
58C65	58C65P	28	DIP		2.5	Site 48/40		
58C66	58C66-SOIC	28	SO		4.2	PinSite	0302/0301	.350 SOIC
63701V0	63701V0	40	DIP		3.5	Site 48/40		
63701X0	63701X0	64	DIP	13	2.0	Site 48/40		
63701Y0	63701Y0	64	DIP	14	2.1	Site 48/40		
63705V0	63705V0	40	DIP		3.5	Site 48/40		
63705Z0	63705Z0	80	FP	16	1.4	Site 48/40		
637A01V0	637A01V0	40	DIP		3.5	Site 48/40		
637A01X0	637A01X0	64	DIP	13	2.0	Site 48/40		
637A01Y0	637A01Y0	64	DIP	14	2.1	Site 48/40		
637A05V0	637A05V0	40	DIP		3.5	Site 48/40		
637A05Z0	637A05Z0	80	FP	16	1.4	Site 48/40		
637B01V0	637B01V0	40	DIP		3.5	Site 48/40		
637B01X0	637B01X0	64	DIP	13	2.0	Site 48/40		
637B01Y0	637B01Y0	64	DIP	14	2.1	Site 48/40		
637B05V0	637B05V0	40	DIP		3.5	Site 48/40		
637B05Z0	637B05Z0	80	FP	16	1.4	Site 48/40		
647180X	647180X-QFP*	80	QFP	62	3.2	Site 48/40		
647180X	647180X-LCC	84	LCC		3.3	PinSite	0202	
6473258	6473258SDIP*	64	SDIP	80	3.3	Site 48/40		
6473308	6473308-QFP*	80	QFP	61	3.2	Site 48/40		
6473308	6473308-LCC	84	LCC		4.0	PinSite	0202	
6473308	6473308-PLCC	84	PLCC		4.1	PinSite	0201	
6473388	6473388-LCC	84	LCC	207	4.2	PinSite	0202	
6475208	6475208SDIP*	64	SDIP	82	3.3	Site 48/40		
6475328	6475328-LCC	84	LCC		4.0	PinSite	0202	
6475328	6475328-PLCC	84	PLCC		4.0	PinSite	0201	
6475328	6475328-QFP*	84	QFP	59	3.2	Site 48/40		
6475368	6475368-LCC	84	LCC	208	4.2	PinSite	0202	
6475368	6475368-PLCC	84	PLCC		4.2	PinSite	0201	
817820	8178204	40	DIP	134	3.6	Site 48/40		
8178232CP	8178232-PLC*	68	PLCC	133	4.0	PinSite	0201	
8178232CP	8178232-PLC*	68	PLCC	135,133	3.6	Site 48/40		
8178234CP	8178234-PLCC	68	PLCC	134	4.0	PinSite	0201	
Hyundai Electronics Industries Co., Ltd.								
18CV8	18CV8	20	DIP		4.2	Site 48/40		
27C64	27C64	28	DIP		2.8	SetSite		
27C64	27C64	28	DIP		1.6	Site 48/40		
93C46	93C46	8	DIP		2.8	Site 48/40		
Integrated Device Technology, Inc.								
78C16A	78C16A	24	DIP		2.1	Site 48/40		
Intel Corporation								
22V10	22V10	24	DIP	151	3.7	Site 48/40		
22V10	22V10-PLCC	28	PLCC	151	3.7	ChipSite		
22V10	22V10-PLCC	28	PLCC	151	3.7	PinSite	0201	
27010	27010	32	DIP		2.0	SetSite		
27010	27010	32	DIP		2.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation (continued)								
27011	27011	28	DIP		2.0	SetSite		
27011	27011	28	DIP		2.0	Site 48/40		
2708	2708	24	DIP		2.0	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		2.0	Site 48/40		
27128A	27128A	28	DIP		2.1	SetSite		
27128A	27128A	28	DIP		2.1	Site 48/40		
27128B	27128B	28	DIP		2.1	SetSite		
27128B	27128B	28	DIP		2.1	Site 48/40		
2716	2716	24	DIP		2.0	SetSite		
2716	2716	24	DIP		2.0	Site 48/40		
27210	27210	40	DIP		2.0	SetSite		
27210	27210	40	DIP		2.1	Site 48/40		
27210	27210-JLCC	44	JLCC		2.6	ChipSite		
27210	27210-JLCC	44	JLCC		3.0	PinSite	0201	
27210	27210-PLCC	44	PLCC		2.6	ChipSite		
27210	27210-PLCC	44	PLCC		3.0	PinSite	0201	
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
27512	27512	28	DIP		2.0	SetSite		
27512	27512	28	DIP		2.0	Site 48/40		
27512	27512-PLCC	32	PLCC		2.2	ChipSite		
27512	27512-PLCC	32	PLCC		3.0	PinSite	0201	
27513	27513	28	DIP		2.0	SetSite		
27513	27513	28	DIP		2.0	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		
2764A	2764A	28	DIP		2.1	SetSite		
2764A	2764A	28	DIP		2.1	Site 48/40		
27960	27960-JLCC	44	JLCC		3.0	PinSite	0201	
27960	27960-PLCC	44	PLCC		3.4	PinSite	0201	
27C010	27C010	32	DIP		2.8	SetSite		
27C010	27C010	32	DIP		2.4	Site 48/40		
27C010	27C010-PLCC	32	PLCC		2.4	ChipSite		
27C010	27C010-PLCC	32	PLCC		3.0	PinSite	0201	
27C010A	27C010A	32	DIP		3.1	SetSite		
27C010A	27C010A	32	DIP		3.1	Site 48/40		
27C011	27C011	28	DIP		3.1	SetSite		
27C011	27C011	28	DIP		3.0	Site 48/40		
27C020	27C020	32	DIP		2.7	SetSite		
27C020	27C020	32	DIP		2.7	Site 48/40		
27C020	27C020-PLCC	32	PLCC		3.1	ChipSite		
27C020	27C020-PLCC	32	PLCC		3.1	PinSite	0201	
27C040	27C040	32	DIP		3.1	SetSite		
27C040	27C040	32	DIP		3.1	Site 48/40		
27C100	27C100	32	DIP		3.0	SetSite		
27C100	27C100	32	DIP		3.0	Site 48/40		
27C128	27C128	28	DIP		2.8	SetSite		
27C128	27C128	28	DIP		2.0	Site 48/40		
27C128	27C128-PLCC	32	PLCC		2.6	ChipSite		
27C128	27C128-PLCC	32	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation (continued)								
27C202	27C202	40	DIP		2.4	Site 48/40		
27C202	27C202-JLCC	44	JLCC		3.2	ChipSite		
27C202	27C202-JLCC	44	JLCC		3.2	PinSite	0201	
27C202	27C202-PLCC	44	PLCC		2.8	ChipSite		
27C202	27C202-PLCC	44	PLCC		3.0	PinSite	0201	
27C203	27C203	40	DIP	3	2.5	Site 48/40		
27C203	27C203-JLCC	44	JLCC	3	3.0	ChipSite		
27C203	27C203-JLCC	44	JLCC	3	3.0	PinSite	0201	
27C203	27C203-PLCC	44	PLCC	3	2.6	ChipSite		
27C203	27C203-PLCC	44	PLCC	3	3.0	PinSite	0201	
27C210	27C210	40	DIP		2.6	SetSite		
27C210	27C210	40	DIP		2.6	Site 48/40		
27C210	27C210-PLCC	44	PLCC		4.0	ChipSite		
27C210	27C210-PLCC	44	PLCC		4.0	PinSite	0201	
27C213	27C213	40	DIP	48	2.8	Site 48/40		
27C220	27C220	40	DIP		3.0	SetSite		
27C220	27C220	40	DIP		2.6	Site 48/40		
27C220	27C220-PLCC	44	PLCC		3.1	ChipSite		
27C220	27C220-PLCC	44	PLCC		3.1	PinSite	0201	
27C240	27C240	40	DIP		3.0	SetSite		
27C240	27C240	40	DIP		2.6	Site 48/40		
27C256	27C256	28	DIP		2.0	SetSite		
27C256	27C256	28	DIP		2.0	Site 48/40		
27C256	27C256-PLCC	32	PLCC		2.0	ChipSite		
27C256	27C256-PLCC	32	PLCC		3.0	PinSite	0201	
27C256A	27C256A	28	DIP		2.6	SetSite		
27C256A	27C256A	28	DIP		2.6	Site 48/40		
27C256A	27C256A-PLCC	32	PLCC		2.6	ChipSite		
27C256A	27C256A-PLCC	32	PLCC		3.0	PinSite	0201	
27C400	27C400	40	DIP		3.2	Site 48/40		
27C512	27C512	28	DIP		3.0	SetSite		
27C512	27C512	28	DIP		2.7	Site 48/40		
27C513	27C513	28	DIP		3.4	Site 48/40		
27C64	27C64	28	DIP		2.1	SetSite		
27C64	27C64	28	DIP		2.1	Site 48/40		
27C64	27C64-PLCC	32	PLCC		2.1	ChipSite		
27C64	27C64-PLCC	32	PLCC		3.0	PinSite	0201	
27C800	27C800	42	DIP		3.3	Site 48		
27F256	27F256	28	DIP		4.0	Site 48/40		
27F64	27F64	28	DIP		4.0	Site 48/40		
2815	2815	24	DIP		2.0	SetSite		
2815	2815	24	DIP		2.0	Site 48/40		
2816	2816	24	DIP		2.0	SetSite		
2816	2816	24	DIP		2.0	Site 48/40		
2816A	2816A	24	DIP		2.1	SetSite		
2816A	2816A	24	DIP		2.1	Site 48/40		
2817A	2817A	28	DIP		2.5	SetSite		
2817A	2817A	28	DIP		2.5	Site 48/40		
2864A	2864A	28	DIP		2.5	SetSite		
2864A	2864A	28	DIP		2.5	Site 48/40		
28F001BX-B	28F001BX-B	32	DIP		4.0	SetSite		
28F001BX-B	28F001BX-B	32	DIP		4.0	Site 48/40		
28F001BX-B	28F001BB-PLC	32	PLCC		4.0	ChipSite		
28F001BX-B	28F001BB-PLC	32	PLCC		4.0	PinSite	0201	
28F001BX-B	28F001BB-TSE	32	TSOP		4.0	PinSite	9901	0702
28F001BX-T	28F001BX-T	32	DIP		4.0	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation (continued)								
28F001BX-T	28F001BX-T	32	DIP		4.0	Site 48/40		
28F001BX-T	28F001BT-PLC	32	PLCC		4.0	ChipSite		
28F001BX-T	28F001BT-PLC	32	PLCC		4.0	PinSite	0201	
28F001BX-T	28F001BT-TSE	32	TSOP		4.0	PinSite	9901	0702
28F002BX-B	28F002BX-B-T	40	TSOP		4.0	PinSite	9901	0701
28F002BX-T	28F002BX-T-T	40	TSOP		4.0	PinSite	9901	0701
28F004BX-B	28F004BX-B-T	40	TSOP		4.0	PinSite	9901	0701
28F004BX-T	28F004BX-T-T	40	TSOP		4.0	PinSite	9901	0701
28F010	28F010	32	DIP		4.2	Site 48/40		
28F010	28F010-PLCC	32	PLCC		4.2	ChipSite		
28F010	28F010-PLCC	32	PLCC		4.2	PinSite	0201	
28F010	28F010-TSOPE	32	TSOP		4.2	PinSite	9901	0702
28F010-P1	28F010	32	DIP		4.2	Site 48/40		
28F010-P1	28F010-PLCC	32	PLCC		4.2	ChipSite		
28F010-P1	28F010-PLCC	32	PLCC		4.2	PinSite	0201	
28F010-R	28F010-TSOPF	32	TSOP		4.2	PinSite	9901	0702
28F020	28F020	32	DIP		4.2	Site 48/40		
28F020	28F020-PLCC	32	PLCC		4.2	ChipSite		
28F020	28F020-PLCC	32	PLCC		4.2	PinSite	0201	
28F020	28F020-TSOPE	32	TSOP		4.2	PinSite	9901	0702
28F020-R	28F020-TSOPF	32	TSOP		4.2	PinSite	9901	0702
28F200BX-B	28F200BX-B-S	44	SOP		4.2	PinSite	0302	.530 SOIC
28F200BX-B	28F200BX-B-S	44	SOP	217	4.2	SetSite		
28F200BX-T	28F200BX-T-S	44	SOP		4.2	PinSite	0302	.530 SOIC
28F200BX-T	28F200BX-T-S	44	SOP	217	4.2	SetSite		
28F256-P1	28F256-P1	32	DIP		4.0	Site 48/40		
28F256-P1	28F256P1PLCC	32	PLCC		4.0	ChipSite		
28F256-P1	28F256P1PLCC	32	PLCC		4.0	PinSite	0201	
28F256-P2	28F256-P2	32	DIP		4.0	Site 48/40		
28F256-P2	28F256P2PLCC	32	PLCC		4.0	ChipSite		
28F256-P2	28F256P2PLCC	32	PLCC		4.0	PinSite	0201	
28F256A	28F256A	32	DIP		4.2	Site 48/40		
28F256A	28F256A-PLCC	32	PLCC		4.2	ChipSite		
28F256A	28F256A-PLCC	32	PLCC		4.2	PinSite	0201	
28F400BX-B	28F400BX-B-S	44	SOP		4.2	PinSite	0302	.530 SOIC
28F400BX-B	28F400BX-B-S	44	SOP	217	4.2	SetSite		
28F400BX-B	28F400BX-B-T	56	TSOP		4.1	PinSite	9901	0703
28F400BX-T	28F400BX-T-S	44	SOP		4.2	PinSite	0302	.530 SOIC
28F400BX-T	28F400BX-T-S	44	SOP	217	4.2	SetSite		
28F400BX-T	28F400BX-T-T	56	TSOP		4.1	PinSite	9901	0703
28F512	28F512	32	DIP		4.2	Site 48/40		
28F512	28F512-PLCC	32	PLCC		4.2	ChipSite		
28F512	28F512-PLCC	32	PLCC		4.2	PinSite	0201	
5AC312	5AC312	24	DIP	49	2.2	Site 48/40		
5AC312	5AC312-PLCC	28	PLCC	49	2.8	ChipSite		
5AC312	5AC312-PLCC	28	PLCC	49	3.0	PinSite	0201	
5AC324	5AC324	40	DIP		3.8	Site 48		
5AC324	5AC324-PLCC	44	PLCC		3.4	PinSite	0201	
5C031	5C031	20	DIP	129	3.9	Site 48/40		
5C032	5C032	20	DIP		1.2	Site 48/40		
5C060	5C060	24	DIP	37	2.7	Site 48/40		
5C060	5C060-PLCC	28	PLCC	37	2.7	ChipSite		
5C060	5C060-PLCC	28	PLCC	37	3.0	PinSite	0201	
5C090	5C090	40	DIP		2.7	Site 48/40		
5C090	5C090-PLCC	44	PLCC		2.7	ChipSite		
5C090	5C090-PLCC	44	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation (continued)								
5C121	5C121	40	DIP		1.0	Site 48/40		
5C180	5C180-JLCC	68	JLCC		3.3	ChipSite		
5C180	5C180-JLCC	68	JLCC		3.3	PinSite	0201	
5C180	5C180-PGA	68	PGA		3.4	PinSite	0402/0401	
5C180	5C180-PLCC	68	PLCC		2.7	ChipSite		
5C180	5C180-PLCC	68	PLCC		3.0	PinSite	0201	
68C257	68C257	28	DIP		2.8	SetSite		
68C257	68C257	28	DIP		2.7	Site 48/40		
68C257	68C257-PLCC	32	PLCC		2.8	ChipSite		
68C257	68C257-PLCC	32	PLCC		3.0	PinSite	0201	
68C257M	68C257M	28	DIP		2.8	SetSite		
68C257M	68C257M	28	DIP		2.7	Site 48/40		
85C060	85C060	24	DIP		3.8	Site 48/40		
85C060	85C060-PLCC	28	PLCC		3.8	ChipSite		
85C060	85C060-PLCC	28	PLCC		3.8	PinSite	0201	
85C090	85C090	40	DIP		3.2	Site 48/40		
85C090	85C090-PLCC	44	PLCC		3.2	ChipSite		
85C090	85C090-PLCC	44	PLCC		3.2	PinSite	0201	
85C220	85C220	20	DIP		2.8	Site 48/40		
85C220	85C220-PLCC	20	PLCC		3.0	ChipSite		
85C220	85C220-PLCC	20	PLCC		3.0	PinSite	0201	
85C224	85C224	24	DIP		3.1	Site 48/40		
85C224	85C224-PLCC	28	PLCC		3.1	ChipSite		
85C224	85C224-PLCC	28	PLCC		3.1	PinSite	0201	
85C22V10	85C22V10	24	DIP	151	3.7	Site 48/40		
85C22V10	85C22V10PLCC	28	PLCC	151	3.7	ChipSite		
85C22V10	85C22V10PLCC	28	PLCC	151	3.7	PinSite	0201	
85C508	85C508	28	DIP		3.4	Site 48/40		
85C508	85C508-PLCC	28	PLCC		4.0	ChipSite		
85C508	85C508-PLCC	28	PLCC		4.0	PinSite	0201	
85C960	85C960	28	DIP		3.4	Site 48/40		
85C960	85C960-PLCC	28	PLCC		3.4	ChipSite		
85C960	85C960-PLCC	28	PLCC		3.4	PinSite	0201	
8741	8741	40	DIP		3.1	Site 48/40		
8741A	8741A	40	DIP		3.1	Site 48/40		
8741AH	8741AH	40	DIP	2	1.5	Site 48/40		
8742	8742	40	DIP		4.0	Site 48/40		
8742AH	8742AH	40	DIP	18,50	2.1	Site 48/40		
8742AH	8742AH-PLCC	44	PLCC	18,50	2.1	ChipSite		
8742AH	8742AH-PLCC	44	PLCC	18,50	3.0	PinSite	0201	
8744H	8744H	40	DIP		2.1	Site 48/40		
8748	8748	40	DIP		1.5	Site 48/40		
8748H	8748H	40	DIP		1.6	Site 48/40		
8749H	8749H	40	DIP		1.6	Site 48/40		
8751	8751	40	DIP		1.6	Site 48/40		
8751BH	8751BH	40	DIP	2	2.6	Site 48/40		
8751BH	8751BH-PLCC	44	PLCC	2	2.7	ChipSite		
8751BH	8751BH-PLCC	44	PLCC	2	3.0	PinSite	0201	
8751H	8751H	40	DIP	2	1.0	Site 48/40		
8751H	8751H-LCC	44	LCC	2,44	1.4	ChipSite		
8751H	8751H-LCC	44	LCC	2,44	3.0	PinSite	0202	
8752BH	8752BH	40	DIP	2	2.1	Site 48/40		
8752BH	8752BH-PLCC	44	PLCC	2	2.1	ChipSite		
8752BH	8752BH-PLCC	44	PLCC	2	3.0	PinSite	0201	
8755A	8755A	40	DIP		1.5	Site 48/40		
8795BH	8795BH	48	DIP	24	3.4	Site 48		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation (continued)								
8796BH	8796BH-LCC	68	LCC	24,44	3.4	ChipSite		
8796BH	8796BH-LCC	68	LCC	24,44	3.4	PinSite	0202	
8797BH	8797BH-LCC	68	LCC	24,44	3.8	ChipSite		
8797BH	8797BH-LCC	68	LCC	24,44	3.8	PinSite	0202	
8797BH	8797BH-PGA	68	PGA	24	3.8	PinSite	0402/0401	
8797BH	8797BH-PLCC	68	PLCC	24,44	4.0	ChipSite		
8797BH	8797BH-PLCC	68	PLCC	24,44	4.0	PinSite	0201	
8797JF	8797JF-PLCC	68	PLCC	24,44	3.2	ChipSite		
8797JF	8797JF-PLCC	68	PLCC	24,44	3.2	PinSite	0201	
8798	8798	48	DIP	24	3.4	Site 48		
87C196JQ	87C196JQ-JLC	52	JLCC	120,191	4.0	PinSite	0201	
87C196JQ	87C196JQ-PLC	52	PLCC	120,191	4.0	PinSite	0201	
87C196JR	87C196JR-JLC	52	JLCC	120,191	4.0	PinSite	0201	
87C196JR	87C196JR-PLC	52	PLCC	120,191	4.0	PinSite	0201	
87C196KB	87C196KB-LCC	68	LCC	30,44	3.7	ChipSite		
87C196KB	87C196KB-LCC	68	LCC	30,44	3.7	PinSite	0202	
87C196KB	87C196KBPLCC	68	PLCC	30	3.7	ChipSite		
87C196KB	87C196KBPLCC	68	PLCC	30	3.7	PinSite	0201	
87C196KB16	87C196KB16-P	68	PLCC	30	3.6	PinSite	0201	
87C196KB16	87C196KB-QFP	80	QFP	30	3.9	PinSite	9901	0507
87C196KC	87C196KCJLCC	68	JLCC	52	3.4	ChipSite		
87C196KC	87C196KCJLCC	68	JLCC	52	3.4	PinSite	0201	
87C196KC	87C196KC-PGA	68	PGA	52	3.4	PinSite	0402/0401	
87C196KC	87C196KC-QFP	80	QFP	52	3.8	PinSite	9901	0507
87C196KC	87C196KC-SQF	80	SQFP	52	3.9	PinSite	9901	0516
87C196KD	87C196KD-JLC	68	JLCC	52	3.8	ChipSite		
87C196KD	87C196KD-JLC	68	JLCC	52	3.8	PinSite	0201	
87C196KD	87C196KD-PLC	68	PLCC	52	4.1	ChipSite		
87C196KD	87C196KD-PLC	68	PLCC	52	4.1	PinSite	0201	
87C196KD	87C196KD-QFP	80	QFP	52	3.8	PinSite	9901	0507
87C196KD	87C196KD-SQF	80	SQFP	52	3.9	PinSite	9901	0516
87C196KJ	87C196KJ-PLC	84	PLCC	193	4.1	PinSite	9901	0228
87C196KQ	87C196KQ-JLC	68	JLCC	120,191	4.0	PinSite	0201	
87C196KQ	87C196KQ-PLC	68	PLCC	120,191	4.0	PinSite	0201	
87C196KR	87C196KR-JLC	68	JLCC	120,191	4.0	PinSite	0201	
87C196KR	87C196KR-PLC	68	PLCC	120,191	4.0	PinSite	0201	
87C196KS	87C196KS-JLC	68	JLCC	120,191	4.0	PinSite	0201	
87C196KS	87C196KS-PLC	68	PLCC	120,191	4.0	PinSite	0201	
87C196KT	87C196KT-JLC	68	JLCC	120,191	4.0	PinSite	0201	
87C196KT	87C196KT-PLC	68	PLCC	120,191	4.0	PinSite	0201	
87C196MC	87C196MC-PLC	84	PLCC	120	3.5	PinSite	0201	
87C196NQ	87C196NQ-PLC	68	PLCC	197,191	4.1	PinSite	0201	
87C196NT	87C196NT-PLC	68	PLCC	197,191	4.1	PinSite	0201	
87C198	87C198-PLCC	52	PLCC	30	3.7	PinSite	0201	
87C198	87C198-QFP	80	QFP	30	3.9	PinSite	9901	0507
87C257	87C257	28	DIP		2.7	SetSite		
87C257	87C257	28	DIP		2.7	Site 48/40		
87C257	87C257-PLCC	32	PLCC		2.7	ChipSite		
87C257	87C257-PLCC	32	PLCC		3.0	PinSite	0201	
87C257I	87C257I	28	DIP		2.8	SetSite		
87C257I	87C257I	28	DIP		2.7	Site 48/40		
87C42	87C42	40	DIP	50,142	3.7	Site 48/40		
87C42	87C42-PLCC	44	PLCC	50,142	3.7	ChipSite		
87C42	87C42-PLCC	44	PLCC	50,142	3.7	PinSite	0201	
87C42	87C42-QFP	44	QFP	50,142	3.9	PinSite	9901	0508
87C452	87C452-PGA*	68	PGA	17	2.1	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation (continued)								
87C51	87C51	40	DIP	2	1.4	Site 48/40		
87C51	87C51-PLCC	44	PLCC	2	1.5	ChipSite		
87C51	87C51-PLCC	44	PLCC	2	3.0	PinSite	0201	
87C51(FX)	87C51-FX	40	DIP	121	3.5	Site 48/40		
87C51(FX)	87C51-FX-PLC	44	PLCC	121	3.5	ChipSite		
87C51(FX)	87C51-FX-PLC	44	PLCC	121	3.5	PinSite	0201	
87C51(FX)	87C51-FX-QFP	44	QFP	121	3.8	PinSite	9901	0508
87C51FA	87C51FA	40	DIP	2	1.4	Site 48/40		
87C51FA	87C51FA-PLCC	44	PLCC	2	2.8	ChipSite		
87C51FA	87C51FA-PLCC	44	PLCC	2	3.0	PinSite	0201	
87C51FA(FX)	87C51FA-FX	40	DIP	121	3.5	Site 48/40		
87C51FA(FX)	87C51FA-FX-P	44	PLCC	121	3.5	ChipSite		
87C51FA(FX)	87C51FA-FX-P	44	PLCC	121	3.5	PinSite	0201	
87C51FA(FX)	87C51FA-FX-Q	44	QFP	121	3.8	PinSite	9901	0508
87C51FB	87C51FB	40	DIP	2	2.6	Site 48/40		
87C51FB	87C51FB-PLCC	44	PLCC	2	2.8	ChipSite		
87C51FB	87C51FB-PLCC	44	PLCC	2	3.0	PinSite	0201	
87C51FB	87C51FB-FX-Q	44	QFP	121	3.8	PinSite	9901	0508
87C51FB(FX)	87C51FB-FX	40	DIP	121	3.5	Site 48/40		
87C51FB(FX)	87C51FB-FX-P	44	PLCC	121	3.5	ChipSite		
87C51FB(FX)	87C51FB-FX-P	44	PLCC	121	3.5	PinSite	0201	
87C51FC	87C51FC	40	DIP	51	3.0	Site 48/40		
87C51FC	87C51FC-PLCC	44	PLCC	51	3.2	PinSite	0201	
87C51FC	87C51FC-QFP	44	QFP	51	3.8	PinSite	9901	0508
87C51GB	87C51GB-JLCC	68	JLCC	107	3.3	PinSite	0201	
87C51SL	87C51SL-BQFP	100	BQFP		4.2	PinSite	9901	0528
87C54	87C54	40	DIP	51	3.5	Site 48/40		
87C54	87C54-PLCC	44	PLCC	51	3.5	PinSite	0201	
87C54	87C54-QFP	44	QFP	51	3.8	PinSite	9901	0508
87C58	87C58	40	DIP	51	3.8	Site 48/40		
87C58	87C58-LCC	44	LCC	51	3.8	PinSite	0202	
87C58	87C58-PLCC	44	PLCC	51	3.8	PinSite	0201	
87C58	87C58-QFP	44	QFP	51	3.8	PinSite	9901	0508
87C64	87C64	28	DIP		2.1	SetSite		
87C64	87C64	28	DIP		2.1	Site 48/40		
87C64	87C64-PLCC	32	PLCC		2.3	ChipSite		
87C64	87C64-PLCC	32	PLCC		3.0	PinSite	0201	
87C75PF	87C75PF	40	DIP	26	2.4	Site 48/40		
87C75PF	87C75PF-PLCC	44	PLCC	26	2.6	ChipSite		
87C75PF	87C75PF-PLCC	44	PLCC	26	3.0	PinSite	0201	
87L42	87L42	40	DIP	50,142	4.1	Site 48/40		
E28F008SA	28F008-TSOPE	40	TSOP		4.0	PinSite	9901	0701
E28F008SA-L	28F008-L-TSE	40	TSOP		4.0	PinSite	9901	0701
F28F008SA	28F008-TSOPF	44	TSOP		4.0	PinSite	9901	0701
F28F008SA-L	28F008-L-TSF	40	TSOP		4.0	PinSite	9901	0701
IFX780-10	FX780-QFP	132	BQFP		4.2	PinSite	9901	0527
IPLD22V10	IPLD22V10	24	DIP		3.8	Site 48/40		
IPLD22V10	IPLD22V10-PL	28	PLCC		3.8	ChipSite		
IPLD22V10	IPLD22V10-PL	28	PLCC		3.8	PinSite	0201	
IPLD610	IPLD610	24	DIP		3.8	Site 48/40		
IPLD610	IPLD610-PLCC	28	PLCC		3.8	ChipSite		
IPLD610	IPLD610-PLCC	28	PLCC		3.8	PinSite	0201	
IPLD910	IPLD910	40	DIP		3.8	Site 48/40		
IPLD910	IPLD910-PLCC	44	PLCC		3.8	ChipSite		
IPLD910	IPLD910-PLCC	44	PLCC		3.8	PinSite	0201	
MC001FLKA	MC001FLKA	68	CARD		4.0	PinSite	9901	0801

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation (continued)								
MC002FLKA	MC002FLKA	68	CARD		4.0	PinSite	9901	0801
MC004FLKA	MC004FLKA	68	CARD		4.0	PinSite	9901	0801
P27128A	P27128A	28	DIP		2.0	SetSite		
P27128A	P27128A	28	DIP		2.0	Site 48/40		
P27256	P27256	28	DIP		2.0	SetSite		
P27256	P27256	28	DIP		2.0	Site 48/40		
P2732A	P2732A	24	DIP		2.0	SetSite		
P2732A	P2732A	24	DIP		2.0	Site 48/40		
P27512	P27512	28	DIP		2.2	SetSite		
P27512	P27512	28	DIP		2.2	Site 48/40		
P2764	P2764	28	DIP		2.0	SetSite		
P2764	P2764	28	DIP		2.0	Site 48/40		
P2764A	P2764A	28	DIP		2.0	SetSite		
P2764A	P2764A	28	DIP		2.0	Site 48/40		
P8741AH	P8741AH	40	DIP	2	1.5	Site 48/40		
P8742AH	P8742AH	40	DIP	18	2.1	Site 48/40		
P8748H	P8748H	40	DIP		1.6	Site 48/40		
P8749H	P8749H	40	DIP		1.6	Site 48/40		
PA28F008SA	28F008SA-SOI	44	SO		4.0	PinSite	0302	.530 SOIC
PA28F008SA-L	28F008-L-SOI	44	SOP		4.0	PinSite	0302	.530 SOIC
International CMOS Technology, Inc.								
153	153	20	DIP	33	2.2	Site 48/40		
173	173	24	DIP	33	2.2	Site 48/40		
18CV8	18CV8	20	DIP		4.2	Site 48/40		
18CV8	18CV8-PLCC	20	PLCC		4.2	ChipSite		
18CV8	18CV8-PLCC	20	PLCC		4.2	PinSite	0201	
20CG10	20CG10	24	DIP	33	2.6	Site 48/40		
20CG10A	20CG10A	24	DIP	33	4.2	Site 48/40		
22CV10	22CV10	24	DIP	33	2.6	Site 48/40		
22CV10	22CV10-PLCC	28	PLCC	33	2.6	ChipSite		
22CV10	22CV10-PLCC	28	PLCC	33	3.0	PinSite	0201	
22CV10A	22CV10A	24	DIP	33	3.6	Site 48/40		
22CV10A	22CV10A-PLCC	28	PLCC	33	3.6	ChipSite		
22CV10A	22CV10A-PLCC	28	PLCC	33	3.6	PinSite	0201	
22CV10A+	22CV10A+	24	DIP		3.6	Site 48/40		
22CV10A+	22CV10A+PLCC	28	PLCC		3.6	ChipSite		
22CV10A+	22CV10A+PLCC	28	PLCC		3.6	PinSite	0201	
22CV10Z	22CV10Z	24	DIP		2.6	Site 48/40		
22CV10Z	22CV10Z-PLCC	28	PLCC		2.7	ChipSite		
22CV10Z	22CV10Z-PLCC	28	PLCC		3.0	PinSite	0201	
253	253	20	DIP		2.2	Site 48/40		
273	273	24	DIP		2.2	Site 48/40		
27CX010	27CX010	32	DIP		3.0	Site 48/40		
27CX256	27CX256	28	DIP		3.5	Site 48/40		
27CX321	27CX321	24	DIP	31	3.6	Site 48/40		
27CX322	27CX322	24	DIP	31	3.6	Site 48/40		
27CX641	27CX641	24	DIP	31	3.6	Site 48/40		
27CX642	27CX642	24	DIP	31	3.6	Site 48/40		
7024	7024	24	DIP		3.3	Site 48/40		
7024	7024-PLCC	28	PLCC		3.3	ChipSite		
7024	7024-PLCC	28	PLCC		3.3	PinSite	0201	
93C46	93C46	8	DIP		2.8	Site 48/40		
93C46A	93C46A	8	DIP		3.4	Site 48/40		
93C56A	93C56A	8	DIP		3.4	Site 48/40		
93C66A	93C66A	8	DIP		3.4	Site 48/40		
93CX56	93CX56	8	DIP		3.5	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
International CMOS Technology, Inc. (continued)								
93CX66	93CX66	8	DIP		3.5	Site 48/40		
Lattice Semiconductor								
16LV8	16LV8	20	DIP	49	4.2	Site 48/40		
16V8	16V8/A/B	20	DIP	49	4.0	Site 48/40		
16V8	16V8/A/BPLCC	20	PLCC	49	4.0	ChipSite		
16V8	16V8/A/BPLCC	20	PLCC	49	4.0	PinSite	0201	
16V8A	16V8/A/B	20	DIP	49	4.0	Site 48/40		
16V8A	16V8/A/B-LCC	20	LCC	49	4.0	ChipSite		
16V8A	16V8/A/B-LCC	20	LCC	49	4.0	PinSite	0202	
16V8A	16V8/A/BPLCC	20	PLCC	49	4.0	ChipSite		
16V8A	16V8/A/BPLCC	20	PLCC	49	4.0	PinSite	0201	
16V8B	16V8/A/B	20	DIP	49	4.0	Site 48/40		
16V8B	16V8/A/BPLCC	20	PLCC	49	4.0	ChipSite		
16V8B	16V8/A/BPLCC	20	PLCC	49	4.0	PinSite	0201	
16V8C	16V8C	20	DIP	49	4.2	Site 48/40		
16V8C	16V8C-PLCC	20	PLCC	49	4.2	ChipSite		
16V8C	16V8C-PLCC	20	PLCC	49	4.2	PinSite	0201	
16V8Z	16V8Z	20	DIP	49	4.2	Site 48/40		
16V8Z	16V8Z-PLCC	20	PLCC	49	4.2	ChipSite		
16V8Z	16V8Z-PLCC	20	PLCC	49	4.2	PinSite	0201	
16VP8B	16VP8B	20	DIP	49	3.8	Site 48		
16VP8B	16VP8B-PLCC	20	PLCC	49	4.0	PinSite	0201	
16Z8	16Z8	24	DIP	28	3.7	Site 48/40		
18V10	18V10	20	DIP	49,28	4.1	Site 48/40		
18V10	18V10-PLCC	20	PLCC	49,28	4.1	ChipSite		
18V10	18V10-PLCC	20	PLCC	49,28	4.1	PinSite	0201	
20LV8	20LV8	24	DIP	49	4.2	Site 48/40		
20RA10	20RA10	24	DIP	49	4.1	Site 48/40		
20RA10	20RA10-LCC	28	LCC	49	4.1	ChipSite		
20RA10	20RA10-LCC	28	LCC	49	4.1	PinSite	0202	
20RA10	20RA10-PLCC	28	PLCC	49	4.1	ChipSite		
20RA10	20RA10-PLCC	28	PLCC	49	4.1	PinSite	0201	
20RA10B	20RA10B	24	DIP		4.1	Site 48/40		
20RA10B	20RA10B-LCC	28	LCC	49	4.1	ChipSite		
20RA10B	20RA10B-LCC	28	LCC	49	4.1	PinSite	0202	
20RA10B	20RA10B-PLCC	28	PLCC	49	4.1	ChipSite		
20RA10B	20RA10B-PLCC	28	PLCC	49	4.1	PinSite	0201	
20RA10BUES	20RA10B-UES	24	DIP	49	4.0	Site 48/40		
20RA10BUES	20RA10B-ULCC	28	LCC	49	4.0	ChipSite		
20RA10BUES	20RA10B-ULCC	28	LCC	49	4.0	PinSite	0202	
20RA10BUES	20RA10B-UPLC	28	PLCC	49	4.0	ChipSite		
20RA10BUES	20RA10B-UPLC	28	PLCC	49	4.0	PinSite	0201	
20RA10UES	20RA10-UES	24	DIP		4.0	Site 48/40		
20RA10UES	20RA10-UESLC	28	LCC	49	4.0	ChipSite		
20RA10UES	20RA10-UESLC	28	LCC	49	4.0	PinSite	0202	
20RA10UES	20RA10-UPLCC	28	PLCC		4.0	ChipSite		
20RA10UES	20RA10-UPLCC	28	PLCC		4.0	PinSite	0201	
20V8	20V8/A/B	24	DIP	49	4.0	Site 48/40		
20V8	20V8/A/BPLCC	28	PLCC	49	4.0	ChipSite		
20V8	20V8/A/BPLCC	28	PLCC	49	4.0	PinSite	0201	
20V8A	20V8/A/B	24	DIP	49	4.0	Site 48/40		
20V8A	20V8/A/B-LCC	28	LCC	49	4.0	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor (continued)								
20V8A	20V8/A/B-LCC	28	LCC	49	4.0	PinSite	0202	
20V8A	20V8/A/BPLCC	28	PLCC	49	4.0	ChipSite		
20V8A	20V8/A/BPLCC	28	PLCC	49	4.0	PinSite	0201	
20V8B	20V8/A/B	24	DIP	49	4.0	Site 48/40		
20V8B	20V8/A/BPLCC	28	PLCC	49	4.0	ChipSite		
20V8B	20V8/A/BPLCC	28	PLCC	49	4.0	PinSite	0201	
20V8C	20V8C	24	DIP	49	4.2	Site 48/40		
20V8C	20V8C-PLCC	28	PLCC	49	4.2	ChipSite		
20V8C	20V8C-PLCC	28	PLCC	49	4.2	PinSite	0201	
20V8Z	20V8Z	24	DIP	49	4.2	Site 48/40		
20V8Z	20V8Z-PLCC	28	PLCC	49	4.2	ChipSite		
20V8Z	20V8Z-PLCC	28	PLCC	49	4.2	PinSite	0201	
20VP8B	20VP8B	24	DIP		3.8	Site 48/40		
20VP8B	20VP8B-PLCC	28	PLCC	49	4.0	PinSite	0201	
20XV10	20XV10/B	24	DIP		3.6	Site 48/40		
20XV10	20XV10/B-PLC	28	PLCC		3.6	ChipSite		
20XV10	20XV10/B-PLC	28	PLCC		3.6	PinSite	0201	
22V10	22V10/B	24	DIP		4.2	Site 48/40		
22V10	22V10/B-LCC	28	LCC	32,49	4.2	ChipSite		
22V10	22V10/B-LCC	28	LCC	32,49	4.2	PinSite	0202	
22V10	22V10/B-PLCC	28	PLCC	32,49	4.2	ChipSite		
22V10	22V10/B-PLCC	28	PLCC	32,49	4.2	PinSite	0201	
22V10B	22V10/B	24	DIP		4.2	PinSite	9901	5101
22V10B	22V10/B	24	DIP		4.2	Site 48/40		
22V10B	22V10/B-LCC	28	LCC	32,49	4.2	ChipSite		
22V10B	22V10/B-LCC	28	LCC	32,49	4.2	PinSite	0202	
22V10B	22V10/B-PLCC	28	PLCC	32,49	4.2	ChipSite		
22V10B	22V10/B-PLCC	28	PLCC	32,49	4.2	PinSite	0201	
22V10B-QP	22V10B-QP	24	DIP		4.2	Site 48/40		
22V10B-QP	22V10BQP-PLC	28	PLCC	32,49	4.2	ChipSite		
22V10B-QP	22V10BQP-PLC	28	PLCC	32,49	4.2	PinSite	0201	
22V10B-QPUES	22V10B-QPUES	24	DIP	32,49	4.1	Site 48/40		
22V10B-QPUES	22V10BQPU-PL	28	PLCC	32,49	4.2	ChipSite		
22V10B-QPUES	22V10BQPU-PL	28	PLCC	32,49	4.2	PinSite	0201	
22V10BUES	22V10/BUES	24	DIP	32,49	4.0	Site 48/40		
22V10BUES	22V10/BU-LCC	28	LCC	32,49	4.0	ChipSite		
22V10BUES	22V10/BU-LCC	28	LCC	32,49	4.0	PinSite	0202	
22V10BUES	22V10/BUPLCC	28	PLCC	32,49	4.0	ChipSite		
22V10BUES	22V10/BUPLCC	28	PLCC	32,49	4.0	PinSite	0201	
22V10C	22V10C	24	DIP	32,49	4.2	Site 48/40		
22V10C	22V10C-PLCC	28	PLCC	32,49	4.2	ChipSite		
22V10C	22V10C-PLCC	28	PLCC	32,49	4.2	PinSite	0201	
22V10CUES	22V10CUES	24	DIP	32,49	4.2	Site 48/40		
22V10CUES	22V10CUES-PL	28	PLCC	32,49	4.2	ChipSite		
22V10CUES	22V10CUES-PL	28	PLCC	32,49	4.2	PinSite	0201	
22V10UES	22V10/BUES	24	DIP	32,49	4.0	Site 48/40		
22V10UES	22V10/BU-LCC	28	LCC	32,49	4.0	ChipSite		
22V10UES	22V10/BU-LCC	28	LCC	32,49	4.0	PinSite	0202	
22V10UES	22V10/BUPLCC	28	PLCC	32,49	4.0	ChipSite		
22V10UES	22V10/BUPLCC	28	PLCC	32,49	4.0	PinSite	0201	
26CV12	26CV12	28	DIP	49	4.1	Site 48		
26CV12	26CV12-LCC	28	LCC	49	4.1	PinSite	0202	
26CV12	26CV12-PLCC	28	PLCC	49	4.1	PinSite	0201	
26CV12B	26CV12B	28	DIP	49	4.1	Site 48		
26CV12B	26CV12B-LCC	28	LCC	49	4.1	PinSite	0202	
26CV12B	26CV12B-PLCC	28	PLCC	49	4.1	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor (continued)								
6001	6001	24	DIP	49	3.9	Site 48/40		
6001	6001-PLCC	28	PLCC	49	4.2	ChipSite		
6001	6001-PLCC	28	PLCC	49	3.9	PinSite	0201	
6001B	6001B	24	DIP	49	3.9	Site 48/40		
6001B	6001B-PLCC	28	PLCC	49	4.2	ChipSite		
6001B	6001B-PLCC	28	PLCC	49	3.9	PinSite	0201	
6002B	6002B	24	DIP		3.9	Site 48/40		
6002B	6002B-PLCC	28	PLCC		3.9	PinSite	0201	
ISPGDS-14	ISPGDS14	20	DIP	32,49	4.0	Site 48		
ISPGDS-14	ISPGDS-14-PL	20	PLCC	32,49	4.1	PinSite	0201	
ISPGDS-18	ISPGDS18	24	DIP	32,49	4.0	Site 48/40		
ISPGDS-22	ISPGDS22	28	DIP	32,49	4.0	Site 48		
ISPGDS-22	ISPGDS-22-PL	28	PLCC	32,49	4.1	PinSite	0201	
ispLSI1016	ISPLSI1016P*	44	PLCC		4.2	PinSite	0201	
ispLSI1016	ISPLSI1016P*	44	PLCC	58	4.2	Site 48/40		
ispLSI1024	ISPLSI1024P*	68	PLCC		4.2	PinSite	0201	
ispLSI1024	ISPLSI1024P*	68	PLCC	97	4.2	Site 48/40		
ispLSI1032	ISPLSI1032P*	84	PLCC		4.2	PinSite	0201	
ispLSI1032	ISPLSI1032P*	84	PLCC	136	4.2	Site 48/40		
ispLSI1048	ISPLSI1048P*	120	QFP	101	4.2	Site 48/40		
pLSI1016	PLSI1016-PL*	44	PLCC		4.1	PinSite	0201	
pLSI1016	PLSI1016-PL*	44	PLCC	58	4.1	Site 48/40		
pLSI1024	PLSI1024-PL*	68	PLCC		4.1	PinSite	0201	
pLSI1024	PLSI1024-PL*	68	PLCC	97	4.1	Site 48/40		
pLSI1032	PLSI1032-PL*	84	PLCC		4.1	PinSite	0201	
pLSI1032	PLSI1032-PL*	84	PLCC	136	4.1	Site 48/40		
pLSI1048	PLSI1048-PL*	120	QFP	101	4.1	Site 48/40		
Macronix Inc.								
27C1000	27C1000	32	DIP		4.0	SetSite		
27C1000	27C1000	32	DIP		4.0	Site 48/40		
27C256	27C256	28	DIP		3.8	SetSite		
27C256	27C256	28	DIP		3.8	Site 48/40		
27C4000	27C4000	32	DIP		4.2	Site 48/40		
27C512	27C512	28	DIP		4.0	SetSite		
27C512	27C512	28	DIP		4.0	Site 48/40		
Microchip Technology Inc.								
16C54	16C54	18	DIP	43	3.3	Site 48		
16C54	16C54-SOIC	18	SO	43	3.3	PinSite	0302/0301	.300 SOIC
16C55	16C55	28	DIP	43	3.3	Site 48		
16C56	16C56	18	DIP	43	3.3	Site 48		
16C57	16C57	28	DIP	43	3.3	Site 48		
16C57	16C57-SOIC	28	SO	43	4.2	PinSite	0302/0301	.300 SOIC
24C01/A	24C01/A	8	DIP		3.3	Site 48/40		
24C01/A/-SN	24C01/A/-SN	8	SO		3.9	PinSite	0302/0301	.150 SOIC
24C02/A	24C02/A	8	DIP		3.3	Site 48/40		
24C02/A-SN	24C02/A-SN	8	SO		3.9	PinSite	0302/0301	.150 SOIC
24C04/A	24C04/A	8	DIP		2.8	Site 48/40		
24C04/A-SN	24C04/A-SN	8	SO		3.9	PinSite	0302/0301	.150 SOIC
24LC16	24LC16	8	DIP		3.7	Site 48/40		
24LC16	24LC16-SOIC	14	SO		3.9	PinSite	0302/0301	.150 SOIC
27256	27256	28	DIP		2.2	SetSite		
27256	27256	28	DIP		2.2	Site 48/40		
27C128	27C128	28	DIP		3.0	SetSite		
27C128	27C128	28	DIP		3.0	Site 48/40		
27C128	27C128-SOIC	28	SO		3.1	ChipSite		
27C128	27C128-SOIC	28	SO		3.1	PinSite	0302/0301	.300 SOIC

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Microchip Technology Inc. (continued)								
27C128	27C128-LCC	32	LCC	44	3.1	ChipSite		
27C128	27C128-LCC	32	LCC	44	3.1	PinSite	0202	
27C128	27C128-PLCC	32	PLCC		3.0	ChipSite		
27C128	27C128-PLCC	32	PLCC		3.0	PinSite	0201	
27C256	27C256	28	DIP		3.0	SetSite		
27C256	27C256	28	DIP		3.0	Site 48/40		
27C256	27C256-SOIC	28	SO		3.1	ChipSite		
27C256	27C256-SOIC	28	SO		3.1	PinSite	0302/0301	.300 SOIC
27C256	27C256-LCC	32	LCC	44	3.1	ChipSite		
27C256	27C256-LCC	32	LCC	44	3.1	PinSite	0202	
27C256	27C256-PLCC	32	PLCC		3.0	ChipSite		
27C256	27C256-PLCC	32	PLCC		3.0	PinSite	0201	
27C512	27C512	28	DIP		3.0	SetSite		
27C512	27C512	28	DIP		3.0	Site 48/40		
27C512	27C512-SOIC	28	SO		3.2	ChipSite		
27C512	27C512-SOIC	28	SO		3.2	PinSite	0302/0301	.300 SOIC
27C512	27C512-LCC	32	LCC	44	3.0	ChipSite		
27C512	27C512-LCC	32	LCC	44	3.0	PinSite	0202	
27C512	27C512-PLCC	32	PLCC		3.1	ChipSite		
27C512	27C512-PLCC	32	PLCC		3.1	PinSite	0201	
27C64	27C64	28	DIP		3.0	SetSite		
27C64	27C64	28	DIP		3.0	Site 48/40		
27C64	27C64-SOIC	28	SO		3.1	ChipSite		
27C64	27C64-SOIC	28	SO		3.1	PinSite	0302/0301	.300 SOIC
27C64	27C64-LCC	32	LCC	44	3.1	ChipSite		
27C64	27C64-LCC	32	LCC	44	3.1	PinSite	0202	
27C64	27C64-PLCC	32	PLCC		3.0	ChipSite		
27C64	27C64-PLCC	32	PLCC		3.0	PinSite	0201	
27HC1616	27HC1616	40	DIP		3.3	Site 48/40		
27HC191	27HC191	24	DIP		2.2	Site 48/40		
27HC256	27HC256	28	DIP		3.0	SetSite		
27HC256	27HC256	28	DIP		3.0	Site 48/40		
27HC256	27HC256-LCC	32	LCC		4.0	ChipSite		
27HC256	27HC256-LCC	32	LCC		4.0	PinSite	0202	
27HC256	27HC256-PLCC	32	PLCC		4.0	ChipSite		
27HC256	27HC256-PLCC	32	PLCC		4.0	PinSite	0201	
27HC291	27HC291	24	DIP		3.6	SetSite		
27HC291	27HC291	24	DIP		2.2	Site 48/40		
27HC64	27HC64	28	DIP		3.0	Site 48/40		
27HC641	27HC641	24	DIP		2.6	Site 48/40		
28C04/A	28C04/A	24	DIP		2.5	Site 48/40		
28C04/A	28C04/A-PLCC	32	PLCC		3.2	ChipSite		
28C04/A	28C04/A-PLCC	32	PLCC		3.2	PinSite	0201	
28C16/A	28C16/A	24	DIP		2.8	SetSite		
28C16/A	28C16/A	24	DIP		2.1	Site 48/40		
28C16/A	28C16/A-PLCC	32	PLCC		2.3	ChipSite		
28C16/A	28C16/A-PLCC	32	PLCC		3.0	PinSite	0201	
28C17/A	28C17/A	28	DIP		2.5	Site 48/40		
28C17/A	28C17/A-SOIC	28	SO		3.4	ChipSite		
28C17/A	28C17/A-SOIC	28	SO		3.4	PinSite	0302/0301	.300 SOIC
28C17/A	28C17/A-PLCC	32	PLCC		3.2	ChipSite		
28C17/A	28C17/A-PLCC	32	PLCC		3.2	PinSite	0201	
28C256	28C256	28	DIP	36	3.1	Site 48/40		
28C64/A	28C64/A	28	DIP		2.8	SetSite		
28C64/A	28C64/A	28	DIP		2.3	Site 48/40		
28C64/A	28C64/A-SOIC	28	SO		3.4	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Raytheon (continued)								
29683/A	29683	24	DIP		2.1	Site 48/40		
29683SM	29683SM	24	DIP		2.1	Site 48/40		
29771	29771	24	DIP		2.6	Site 48/40		
29771SM	29771SM	24	DIP		2.6	Site 48/40		
29773	29773	24	DIP		2.6	Site 48/40		
29773SM	29773SM	24	DIP		2.6	Site 48/40		
29791	29791	24	DIP		2.6	Site 48/40		
29791DM	29791DM	24	DIP		2.6	Site 48/40		
29793	29793	24	DIP		2.6	Site 48/40		
29793DM	29793DM	24	DIP		2.6	Site 48/40		
Ricoh Corporation								
10P8A	10P8A	20	DIP		1.0	Site 48/40		
10P8B	10P8B	20	DIP		1.0	Site 48/40		
10P8B	10P8B-SOIC	20	SO		2.6	ChipSite		
10P8B	10P8B-SOIC	20	SO		3.0	PinSite	0302/0301	.300 SOIC
12P6A	12P6A	20	DIP		1.0	Site 48/40		
12P6B	12P6B	20	DIP		1.0	Site 48/40		
14P4A	14P4A	20	DIP		1.0	Site 48/40		
14P4B	14P4B	20	DIP		1.0	Site 48/40		
16P2A	16P2A	20	DIP		1.0	Site 48/40		
16P2B	16P2B	20	DIP		1.0	Site 48/40		
16P8B	16P8B	20	DIP		1.0	Site 48/40		
16P8B	16P8B-SOIC	20	SO		2.6	ChipSite		
16P8B	16P8B-SOIC	20	SO		3.0	PinSite	0302/0301	.300 SOIC
16P8F	EPL16P8F	20	DIP		3.8	Site 48/40		
16RP4B	16RP4B	20	DIP		1.0	Site 48/40		
16RP4B	16RP4B-SOIC	20	SO		4.2	ChipSite		
16RP4B	16RP4B-SOIC	20	SO		4.2	PinSite	0302/0301	.300 SOIC
16RP4F	EPL16RP4F	20	DIP		3.8	Site 48/40		
16RP4F	EPL16RP4FJ	20	PLCC		4.0	ChipSite		
16RP4F	EPL16RP4FJ	20	PLCC		4.0	PinSite	0201	
16RP6B	16RP6B	20	DIP		1.0	Site 48/40		
16RP6F	EPL16RP6F	20	DIP		3.8	Site 48/40		
16RP8B	16RP8B	20	DIP		1.0	Site 48/40		
16RP8B	16RP8B-SOIC	20	SO		2.6	ChipSite		
16RP8B	16RP8B-SOIC	20	SO		3.0	PinSite	0302/0301	.300 SOIC
16RP8F	EPL16RP8F	20	DIP		3.8	Site 48/40		
2020	2020-JLCC	84	JLCC	94	3.4	PinSite	0201	
2020	2020-PLCC	84	PLCC	94	3.4	PinSite	0201	
204	204	20	DIP		2.6	Site 48/40		
241	241	24	DIP		2.4	Site 48/40		
241	241-PLCC	28	PLCC		2.4	ChipSite		
241	241-PLCC	28	PLCC		3.0	PinSite	0201	
242	242	24	DIP		3.8	Site 48/40		
27C256	27C256	28	DIP		2.1	SetSite		
27C256	27C256	28	DIP		2.1	Site 48/40		
27C32	27C32	24	DIP		2.0	SetSite		
27C32	27C32	24	DIP		2.0	Site 48/40		
27C64	27C64	28	DIP		2.0	SetSite		
27C64	27C64	28	DIP		2.0	Site 48/40		
5H32	5H32	24	DIP		2.0	SetSite		
5H32	5H32	24	DIP		2.0	Site 48/40		
687C64	687C64	24	DIP		1.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Rockwell International								
87C64	87C64	28	DIP		2.8	SetSite		
87C64	87C64	28	DIP		1.0	Site 48/40		
SEEQ Technology, Inc.								
20RA10Z	20RA10Z	24	DIP		2.3	Site 48/40		
20RA10Z	20RA10Z-PLCC	28	PLCC		2.7	ChipSite		
20RA10Z	20RA10Z-PLCC	28	PLCC		3.0	PinSite	0201	
26V12	26V12	28	DIP		2.7	Site 48		
27128	27128	28	DIP		2.2	SetSite		
27128	27128	28	DIP		2.2	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		
27C256	27C256	28	DIP		2.1	SetSite		
27C256	27C256	28	DIP		2.1	Site 48/40		
2816A	2816A	24	DIP		2.1	SetSite		
2816A	2816A	24	DIP		2.1	Site 48/40		
2816AH	2816AH	24	DIP		2.0	SetSite		
2816AH	2816AH	24	DIP		2.0	Site 48/40		
2817A	2817A	28	DIP		2.5	SetSite		
2817A	2817A	28	DIP		2.5	Site 48/40		
2817AH	2817AH	28	DIP		2.5	SetSite		
2817AH	2817AH	28	DIP		2.5	Site 48/40		
2864	2864/H	28	DIP		2.8	SetSite		
2864	2864/H	28	DIP		1.5	Site 48/40		
2864H	2864/H	28	DIP		2.0	SetSite		
2864H	2864/H	28	DIP		1.5	Site 48/40		
28C010	28C010	32	DIP		4.0	Site 48/40		
28C256	28C256	28	DIP		2.0	SetSite		
28C256	28C256	28	DIP		2.0	Site 48/40		
28C256	28C256-PLCC	32	PLCC		3.8	ChipSite		
28C256	28C256-PLCC	32	PLCC		3.8	PinSite	0201	
28C256A	28C256A	28	DIP	36	3.5	SetSite		
28C256A	28C256A	28	DIP	36	3.5	Site 48/40		
28C256A	28C256A-PLCC	32	PLCC		3.8	ChipSite		
28C256A	28C256A-PLCC	32	PLCC		3.8	PinSite	0201	
28C64	28C64	28	DIP		2.0	SetSite		
28C64	28C64	28	DIP		2.0	Site 48/40		
28C64	28C64-PLCC	32	PLCC		2.4	ChipSite		
28C64	28C64-PLCC	32	PLCC		3.0	PinSite	0201	
28C65	28C65	28	DIP		3.6	SetSite		
28C65	28C65	28	DIP		3.6	Site 48/40		
28C65	28C65-PLCC	32	PLCC		4.0	ChipSite		
28C65	28C65-PLCC	32	PLCC		4.0	PinSite	0201	
28HC256	28HC256	28	DIP		4.1	Site 48/40		
28HC256	28HC256-LCC	32	LCC		4.1	ChipSite		
28HC256	28HC256-LCC	32	LCC		4.1	PinSite	0202	
28HC256	28HC256-PLCC	32	PLCC		4.1	ChipSite		
28HC256	28HC256-PLCC	32	PLCC		4.1	PinSite	0201	
36C16	36C16	24	DIP		2.3	Site 48/40		
36C32	36C32	24	DIP		2.6	SetSite		
36C32	36C32	24	DIP		2.6	Site 48/40		
38C32	38C32	28	DIP		2.6	SetSite		
38C32	38C32	28	DIP		2.6	Site 48/40		
47F010	47F010	32	DIP		3.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SEEQ Technology, Inc. (continued)								
47F512	47F512	32	DIP		2.8	Site 48/40		
48128	48128	28	DIP		1.7	Site 48/40		
48F010	48F010	32	DIP		3.4	Site 48/40		
48F010	48F010-PLCC	32	PLCC		3.4	ChipSite		
48F010	48F010-PLCC	32	PLCC		3.4	PinSite	0201	
48F512	48F512	32	DIP		3.4	Site 48/40		
48F512	48F512-PLCC	32	PLCC		3.4	ChipSite		
48F512	48F512-PLCC	32	PLCC		3.4	PinSite	0201	
52B13	52B13	24	DIP		2.0	SetSite		
52B13	52B13	24	DIP		2.0	Site 48/40		
52B13H	52B13H	24	DIP		2.0	SetSite		
52B13H	52B13H	24	DIP		2.0	Site 48/40		
52B33	52B33	28	DIP		2.2	SetSite		
52B33	52B33	28	DIP		2.2	Site 48/40		
52B33H	52B33H	28	DIP		2.0	SetSite		
52B33H	52B33H	28	DIP		2.0	Site 48/40		
52B33H	52B33H-LCC	32	LCC	44	1.4	ChipSite		
52B33H	52B33H-LCC	32	LCC	44	3.0	PinSite	0202	
5516A	5516A	24	DIP		2.1	SetSite		
5516A	5516A	24	DIP		2.1	Site 48/40		
SGS-Thomson Microelectronics								
16V8	16V8/AS	20	DIP	22,49	2.8	Site 48/40		
16V8	16V8/AS-PLCC	20	PLCC	22,49	2.8	ChipSite		
16V8	16V8/AS-PLCC	20	PLCC	22,49	3.0	PinSite	0201	
20V8	20V8/AS	24	DIP	22,49	2.8	Site 48/40		
20V8	20V8/AS-PLCC	28	PLCC	22,49	3.2	ChipSite		
20V8	20V8/AS-PLCC	28	PLCC	22,49	3.2	PinSite	0201	
20V8/AS-J	20V8/AS-J-FN	28	PLCC	22,49	3.1	ChipSite		
20V8/AS-J	20V8/AS-J-FN	28	PLCC	22,49	3.1	PinSite	0201	
24C01B	24C01	8	DIP		3.6	Site 48/40		
24C02	24C02	8	DIP		3.5	Site 48		
24C02A	24C02A	8	DIP		3.6	Site 48/40		
24C04	24C04-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
24C04B	24C04	8	DIP		3.6	Site 48/40		
24C08B	24C08	8	DIP		3.6	Site 48/40		
2532	2532	24	DIP		2.0	SetSite		
2532	2532	24	DIP		2.0	Site 48/40		
25C02A	25C02A	8	DIP		3.7	Site 48/40		
25C02A	25C02A-SOIC	8	SO		3.9	PinSite	0302/0301	.150 SOIC
25C04	25C04	8	DIP		3.7	Site 48/40		
25C04	25C04-SOIC	14	SO		3.9	PinSite	0302/0301	.150 SOIC
27128A	27128A	28	DIP		2.1	SetSite		
27128A	27128A	28	DIP		2.1	Site 48/40		
2716	2716	24	DIP		2.0	SetSite		
2716	2716	24	DIP		2.0	Site 48/40		
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
27512	27512	28	DIP		2.8	SetSite		
27512	27512	28	DIP		1.6	Site 48/40		
2764	2764	28	DIP		2.2	SetSite		
2764	2764	28	DIP		2.2	Site 48/40		
2764A	2764A	28	DIP		3.5	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SGS-Thomson Microelectronics (continued)								
2764A	2764A	28	DIP		3.5	Site 48/40		
27C1000	27C1000	32	DIP		4.2	SetSite		
27C1000	27C1000	32	DIP		4.2	Site 48/40		
27C1001	27C1001	32	DIP		4.2	SetSite		
27C1001	27C1001	32	DIP		4.2	Site 48/40		
27C1001	27C1001-PLCC	32	PLCC		4.2	ChipSite		
27C1001	27C1001-PLCC	32	PLCC		4.2	PinSite	0201	
27C1024	27C1024	40	DIP		4.2	SetSite		
27C1024	27C1024	40	DIP		4.2	Site 48/40		
27C1024	27C1024-PLCC	44	PLCC		4.2	ChipSite		
27C1024	27C1024-PLCC	44	PLCC		4.2	PinSite	0201	
27C16	27C16	24	DIP		2.0	SetSite		
27C16	27C16	24	DIP		2.0	Site 48/40		
27C2001	27C2001	32	DIP		4.2	SetSite		
27C2001	27C2001	32	DIP		4.2	Site 48/40		
27C2001	27C2001-PLCC	32	PLCC		4.2	ChipSite		
27C2001	27C2001-PLCC	32	PLCC		4.2	PinSite	0201	
27C256	27C256	28	DIP		2.1	SetSite		
27C256	27C256	28	DIP		2.1	Site 48/40		
27C256	27C256-PLCC	32	PLCC		3.0	ChipSite		
27C256	27C256-PLCC	32	PLCC		3.0	PinSite	0201	
27C256B	27C256B	28	DIP		4.2	SetSite		
27C256B	27C256B	28	DIP		4.2	Site 48/40		
27C256B	27C256B-PLCC	32	PLCC		4.2	ChipSite		
27C256B	27C256B-PLCC	32	PLCC		4.2	PinSite	0201	
27C32	27C32	24	DIP		2.8	SetSite		
27C32	27C32	24	DIP		2.0	Site 48/40		
27C4001	27C4001	32	DIP		4.2	SetSite		
27C4001	27C4001	32	DIP		4.2	Site 48/40		
27C4002	27C4002	40	DIP		4.2	SetSite		
27C4002	27C4002	40	DIP		4.2	Site 48/40		
27C4002	27C4002-PLCC	44	PLCC		4.2	ChipSite		
27C4002	27C4002-PLCC	44	PLCC		4.2	PinSite	0201	
27C512	27C512	28	DIP		4.2	SetSite		
27C512	27C512	28	DIP		4.2	Site 48/40		
27C512	27C512-PLCC	32	PLCC		4.2	ChipSite		
27C512	27C512-PLCC	32	PLCC		4.2	PinSite	0201	
27C516	27C516	40	DIP		3.8	SetSite		
27C516	27C516	40	DIP		3.8	Site 48/40		
27C516	27C516-PLCC	44	PLCC		3.8	ChipSite		
27C516	27C516-PLCC	44	PLCC		3.8	PinSite	0201	
27C64	27C64	28	DIP		2.1	SetSite		
27C64	27C64	28	DIP		2.1	Site 48/40		
27C64	27C64-PLCC	32	PLCC		2.1	ChipSite		
27C64	27C64-PLCC	32	PLCC		3.0	PinSite	0201	
27C64A	27C64A	28	DIP		4.2	Site 48/40		
28F101	28F101	32	DIP		4.2	Site 48/40		
28F101	28F101-PLCC	32	PLCC		4.2	ChipSite		
28F101	28F101-PLCC	32	PLCC		4.2	PinSite	0201	
28F102	28F102	40	DIP		4.2	Site 48/40		
28F102	28F102-PLCC	44	PLCC		4.1	PinSite	0201	
28F256	28F256	32	DIP		4.0	Site 48/40		
28F256	28F256-PLCC	32	PLCC		4.1	ChipSite		
28F256	28F256-PLCC	32	PLCC		4.1	PinSite	0201	
28F512	28F512	32	DIP		4.2	Site 48/40		
28F512	28F512-PLCC	32	PLCC		4.2	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SGS-Thomson Microelectronics (continued)								
28F512	28F512-PLCC	32	PLCC		4.2	PinSite	0201	
59C11	59C11	8	DIP		3.2	Site 48/40		
6001/AS	6001/AS	24	DIP	49	4.0	Site 48/40		
6001/AS	6001/AS-PLCC	28	PLCC	49	4.0	ChipSite		
6001/AS	6001/AS-PLCC	28	PLCC	49	4.0	PinSite	0201	
62E10	62E10	20	DIP	2,140,21,170	4.0	Site 48/40		
62E15	62E15	28	DIP	2,140,21,170	4.0	Site 48/40		
62E20F1	62E20F1	20	DIP	2,140,21,189	4.0	Site 48/40		
62E25F1	62E25F1	28	DIP	2,140,21,189	4.0	Site 48/40		
71180	71180	24	DIP		2.2	Site 48/40		
71181	71181	24	DIP		2.2	Site 48/40		
71190	71190	24	DIP		2.2	Site 48/40		
71191	71191	24	DIP	2	2.2	Site 48/40		
71280	71280	24	DIP		2.2	Site 48/40		
71281	71281	24	DIP		2.2	Site 48/40		
71290	71290	24	DIP		2.2	Site 48/40		
71291	71291	24	DIP		2.2	Site 48/40		
71320	71320	24	DIP		2.2	Site 48/40		
71321	71321	24	DIP		2.2	Site 48/40		
71640	71640	24	DIP		2.2	Site 48/40		
71641	71641	24	DIP		2.2	Site 48/40		
87C257	87C257	28	DIP		4.2	SetSite		
87C257	87C257	28	DIP		4.2	Site 48/40		
87C257	87C257-PLCC	32	PLCC		4.2	ChipSite		
87C257	87C257-PLCC	32	PLCC		4.2	PinSite	0201	
9346	9346	8	DIP		3.2	Site 48/40		
93C06	93C06/B	8	DIP		3.6	Site 48/40		
93C06B	93C06/B	8	DIP		3.6	Site 48/40		
93C46	93C46/AB	8	DIP		3.6	Site 48/40		
93C46AB	93C46/AB	8	DIP		3.6	Site 48/40		
93CS46	93CS46/B	8	DIP		3.6	Site 48/40		
93CS46B	93CS46/B	8	DIP		3.6	Site 48/40		
93CS56	93CS56/B	8	DIP		3.6	Site 48/40		
93CS56B	93CS56/B	8	DIP		3.6	Site 48/40		
T2716	2716	24	DIP		2.0	SetSite		
T2716	2716	24	DIP		2.0	Site 48/40		
T2764	T2764	28	DIP		2.0	SetSite		
T2764	T2764	28	DIP		1.0	Site 48/40		
Z86E11	Z86E11	40	DIP		2.2	Site 48/40		
Z86E21	Z86E21	40	DIP		2.2	Site 48/40		
SMOS Systems, Inc.								
27128H	27128H	28	DIP		2.0	SetSite		
27128H	27128H	28	DIP		2.0	Site 48/40		
27C256H	27C256H	28	DIP		2.1	SetSite		
27C256H	27C256H	28	DIP		2.1	Site 48/40		
27C64H	27C64H	28	DIP		2.0	SetSite		
27C64H	27C64H	28	DIP		2.0	Site 48/40		
Samsung Semiconductor, Inc.								
16L8	16L8	20	DIP		3.0	Site 48/40		
16L8	16L8-PLCC	20	PLCC		3.0	ChipSite		
16L8	16L8-PLCC	20	PLCC		3.0	PinSite	0201	
16R4	16R4	20	DIP		3.0	Site 48/40		
16R4	16R4-PLCC	20	PLCC		3.0	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Samsung Semiconductor, Inc. (continued)								
16R4	16R4-PLCC	20	PLCC		3.0	PinSite	0201	
16R6	16R6	20	DIP		3.0	Site 48/40		
16R6	16R6-PLCC	20	PLCC		3.0	ChipSite		
16R6	16R6-PLCC	20	PLCC		3.0	PinSite	0201	
16R8	16R8	20	DIP		3.0	Site 48/40		
16R8	16R8-PLCC	20	PLCC		3.0	ChipSite		
16R8	16R8-PLCC	20	PLCC		3.0	PinSite	0201	
20L10	20L10	24	DIP		3.0	Site 48/40		
20L10	20L10-NL	28	PLCC		3.0	ChipSite		
20L10	20L10-NL	28	PLCC		3.0	PinSite	0201	
20L8	20L8	24	DIP		3.0	Site 48/40		
20L8	20L8-NL	28	PLCC		3.0	ChipSite		
20L8	20L8-NL	28	PLCC		3.0	PinSite	0201	
20R4	20R4	24	DIP		3.0	Site 48/40		
20R4	20R4-NL	28	PLCC		3.0	ChipSite		
20R4	20R4-NL	28	PLCC		3.0	PinSite	0201	
20R6	20R6	24	DIP		3.0	Site 48/40		
20R6	20R6-NL	28	PLCC		3.0	ChipSite		
20R6	20R6-NL	28	PLCC		3.0	PinSite	0201	
20R8	20R8	24	DIP		3.0	Site 48/40		
20R8	20R8-NL	28	PLCC		3.0	ChipSite		
20R8	20R8-NL	28	PLCC		3.0	PinSite	0201	
22V10	22V10	24	DIP		3.0	Site 48/40		
2816A	2816A	24	DIP		2.1	SetSite		
2816A	2816A	24	DIP		2.1	Site 48/40		
2817A	2817A	28	DIP		2.5	SetSite		
2817A	2817A	28	DIP		2.5	Site 48/40		
2864A	2864A/AH	28	DIP		2.0	SetSite		
2864A	2864A/AH	28	DIP		2.0	Site 48/40		
2864AH	2864A/AH	28	DIP		2.0	SetSite		
2864AH	2864A/AH	28	DIP		1.5	Site 48/40		
2865A	2865A/AH	28	DIP		2.0	SetSite		
2865A	2865A/AH	28	DIP		1.5	Site 48/40		
2865AH	2865A/AH	28	DIP		2.0	SetSite		
2865AH	2865A/AH	28	DIP		1.5	Site 48/40		
28C16	28C16	24	DIP		2.8	Site 48/40		
28C17	28C17	28	DIP		2.8	Site 48/40		
28C256	28C256	28	DIP		2.8	Site 48/40		
28C256	28C256-PLCC	32	PLCC		3.8	ChipSite		
28C256	28C256-PLCC	32	PLCC		3.8	PinSite	0201	
28C64	28C64	28	DIP		2.8	Site 48/40		
28C65	28C65	28	DIP		2.8	Site 48/40		
Seiko Epson								
BWB065	YO	BWB065SDY0	68	CARD		4.2	PinSite	9901
BWB129SDX	BWB129SDY0	68	CARD		4.2	PinSite	9901	0801
BWB513-XO	BWB513*	68	CARD	154	3.8	Site 48/40		
HWB513-XO	HWB513*	68	CARD	154	4.2	Site 48/40		
Seiko Instruments Inc.								
2100R/RF	2100	8	DIP		3.7	Site 48/40		
22H10	22H10	18	DIP		3.9	Site 48		
22H12R/I	22H12	18	DIP		3.8	Site 48		
22S10R/I	22S10	18	DIP		3.9	Site 48		
22S12R/I	22S12	18	DIP		3.8	Site 48		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Seiko Instruments Inc. (continued)								
24H45R/I	24H45	8	DIP		3.8	Site 48/40		
24S30R/I	24S30	8	DIP		3.9	Site 48/40		
24S45R/I	24S45	8	DIP		3.8	Site 48/40		
2840A(R)	2840	24	DIP		3.7	Site 48/40		
2911R/I	2911	8	DIP		3.7	Site 48/40		
2913AR/I	2913A	8	DIP		3.7	Site 48/40		
2913AR/I	2913A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2913CR/I	2913C	8	DIP		3.7	Site 48/40		
2913CR/I	2913C-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2914AID	2914AID-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2914AR/I	2914A	8	DIP		3.8	Site 48/40		
2914AR/I	2914A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2914R/RF	2914	8	DIP		3.7	Site 48/40		
2917R/I	2917	8	DIP		3.7	Site 48/40		
2918R/I	2918	8	DIP		3.7	Site 48/40		
2919AR/I	2919A	8	DIP		3.7	Site 48/40		
2919AR/I	2919A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2919CR/I	2919C	8	DIP		3.7	Site 48/40		
2919CR/I	2919C-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2919GR/I	2919G	8	DIP		3.7	Site 48/40		
2919GR/I	2919G-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2922AR/I	2922A	8	DIP		3.8	Site 48/40		
2922AR/I	2922A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2923CR/I	2923C	8	DIP		3.7	Site 48/40		
2923CR/I	2923C-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2924AR/I	2924A	8	DIP		3.7	Site 48/40		
2924AR/I	2924A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2929AR/I	2929A	8	DIP		3.7	Site 48/40		
2929AR/I	2929A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2929CR/I	2929C	8	DIP		3.7	Site 48/40		
2929CR/I	2929C-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2929GR/I	2929G	8	DIP		3.7	Site 48/40		
2929GR/I	2929G-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2933CR/I	2933C	8	DIP		3.7	Site 48/40		
2933CR/I	2933C-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2934AR/I	2934A	8	DIP		3.8	Site 48/40		
2934AR/I	2934A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2939AR/I	2939A	8	DIP		3.7	Site 48/40		
2939AR/I	2939A-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2939CR/I	2939C	8	DIP		3.7	Site 48/40		
2939CR/I	2939C-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2939GR/I	2939G	8	DIP		3.7	Site 48/40		
2939GR/I	2939G-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
2940I/IF	2940	8	DIP		3.7	Site 48/40		
2961I/IF	2961	8	DIP		3.7	Site 48/40		
2980I/IF	2980	8	DIP		3.7	Site 48/40		
Sharp Corporation								
571000	571000	32	DIP		3.0	SetSite		
571000	571000	32	DIP		2.8	Site 48/40		
571001	571001	32	DIP		2.8	Site 48/40		
57126	57126	28	DIP		2.1	SetSite		
57126	57126	28	DIP		2.1	Site 48/40		
57127	57127	28	DIP		2.1	SetSite		
57127	57127	28	DIP		2.1	Site 48/40		
57128	57128	28	DIP		2.8	SetSite		
57128	57128	28	DIP		2.0	Site 48/40		
57191	57191	24	DIP		2.8	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Sharp Corporation (continued)								
57191	57191	24	DIP		2.0	Site 48/40		
57254	57254	28	DIP		2.3	SetSite		
57254	57254	28	DIP		2.3	Site 48/40		
57255	57255	28	DIP		2.3	SetSite		
57255	57255	28	DIP		2.3	Site 48/40		
57256	57256	28	DIP		2.5	SetSite		
57256	57256	28	DIP		2.5	Site 48/40		
57257J-12	57257	28	DIP		3.8	SetSite		
57257J-12	57257	28	DIP		3.8	Site 48/40		
5749	5749	24	DIP		2.0	SetSite		
5749	5749	24	DIP		2.0	Site 48/40		
57512	57512	28	DIP		3.0	SetSite		
57512	57512	28	DIP		2.8	Site 48/40		
5762	5762	28	DIP		2.1	SetSite		
5762	5762	28	DIP		2.1	Site 48/40		
5763	5763	28	DIP		2.1	SetSite		
5763	5763	28	DIP		2.1	Site 48/40		
5764	5764	28	DIP		2.0	SetSite		
5764	5764	28	DIP		2.0	Site 48/40		
CE-776S	CE776S	45	CARD	209	4.2	Site 48/40		
Simtek Corporation								
10C68	10C68	28	DIP		3.5	Site 48/40		
11C68	11C68	28	DIP		3.5	Site 48/40		
11C68	11C68-LCC*	28	LCC		3.9	Site 48/40		
Sony Corporation								
27C1000	27C1000	32	DIP		3.0	SetSite		
27C1000	27C1000	32	DIP		3.0	Site 48/40		
27C1001	27C1001	32	DIP		3.0	SetSite		
27C1001	27C1001	32	DIP		3.0	Site 48/40		
27C2001	27C2001	32	DIP		3.9	Site 48/40		
27C256	27C256	28	DIP		3.0	SetSite		
27C256	27C256	28	DIP		3.0	Site 48/40		
27C4001	27C4001	32	DIP		3.9	Site 48/40		
27C4002	27C4002	40	DIP		3.9	Site 48/40		
27C512	27C512	28	DIP		3.0	SetSite		
27C512	27C512	28	DIP		3.0	Site 48/40		
Texas Instruments								
10H16ET6	10H16ET6	24	DIP		2.7	Site 48		
10H16P8-3	10H16P8-3	24	DIP		2.6	Site 48/40		
10H16P8-3	10H16P8-3-FN	28	PLCC		2.6	ChipSite		
10H16P8-3	10H16P8-3-FN	28	PLCC		3.0	PinSite	0201	
10H16P8-6	10H16P8-6	24	DIP	19	2.2	Site 48/40		
10H16P8-6	10H16P8-6-FN	28	PLCC		2.2	ChipSite		
10H16P8-6	10H16P8-6-FN	28	PLCC		3.0	PinSite	0201	
1602	1602	20	DIP		3.4	Site 48/40		
1602	1602-PLCC	20	PLCC		3.4	ChipSite		
1602	1602-PLCC	20	PLCC		3.4	PinSite	0201	
16L8-10	16L8-10	20	DIP		2.3	Site 48/40		
16L8-10	16L8-10-PLCC	20	PLCC		2.3	ChipSite		
16L8-10	16L8-10-PLCC	20	PLCC		3.0	PinSite	0201	
16L8-12	16L8-12-PLCC	20	PLCC		1.7	ChipSite		
16L8-12	16L8-12-PLCC	20	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
16L8-12/15/25	16L812/15/25	20	DIP		1.7	Site 48/40		
16L8-15	16L8-15-PLCC	20	PLCC		1.7	ChipSite		
16L8-15	16L8-15-PLCC	20	PLCC		3.0	PinSite	0201	
16L8-25	16L8-25-PLCC	20	PLCC		1.7	ChipSite		
16L8-25	16L8-25-PLCC	20	PLCC		3.0	PinSite	0201	
16L8-5	16L8-5	20	DIP		3.8	Site 48/40		
16L8-5	16L8-5-LCC	20	LCC	44	3.8	ChipSite		
16L8-5	16L8-5-LCC	20	LCC	44	3.8	PinSite	0202	
16L8-5	16L8-5-PLCC	20	PLCC		3.8	ChipSite		
16L8-5	16L8-5-PLCC	20	PLCC		3.8	PinSite	0201	
16L8-7	16L8-7	20	DIP		3.8	Site 48/40		
16L8-7	16L8-7-PLCC	20	PLCC		3.8	ChipSite		
16L8-7	16L8-7-PLCC	20	PLCC		3.8	PinSite	0201	
16L8A	16L8A-LCC	20	LCC		1.7	ChipSite		
16L8A	16L8A-LCC	20	LCC		3.0	PinSite	0202	
16L8A-2	16L8A-2-LCC	20	LCC		1.7	ChipSite		
16L8A-2	16L8A-2-LCC	20	LCC		3.0	PinSite	0202	
16L8A/A-2	16L8A/A-2	20	DIP		1.7	Site 48/40		
16N8	16N8	20	DIP		2.1	Site 48/40		
16N8	16N8-PLCC	20	PLCC		2.3	ChipSite		
16N8	16N8-PLCC	20	PLCC		3.0	PinSite	0201	
16R4-10	16R4-10	20	DIP		2.3	Site 48/40		
16R4-10	16R4-10-PLCC	20	PLCC		2.3	ChipSite		
16R4-10	16R4-10-PLCC	20	PLCC		3.0	PinSite	0201	
16R4-12	16R4-12-PLCC	20	PLCC		1.7	ChipSite		
16R4-12	16R4-12-PLCC	20	PLCC		3.0	PinSite	0201	
16R4-12/15/25	16R412/15/25	20	DIP		1.7	Site 48/40		
16R4-15	16R4-15-PLCC	20	PLCC		1.7	ChipSite		
16R4-15	16R4-15-PLCC	20	PLCC		3.0	PinSite	0201	
16R4-25	16R4-25-PLCC	20	PLCC		1.7	ChipSite		
16R4-25	16R4-25-PLCC	20	PLCC		3.0	PinSite	0201	
16R4-5	16R4-5	20	DIP		3.8	Site 48/40		
16R4-5	16R4-5-LCC	20	LCC	44	3.8	ChipSite		
16R4-5	16R4-5-LCC	20	LCC	44	3.8	PinSite	0202	
16R4-5	16R4-5-PLCC	20	PLCC		3.8	ChipSite		
16R4-5	16R4-5-PLCC	20	PLCC		3.8	PinSite	0201	
16R4-7	16R4-7	20	DIP		3.8	Site 48/40		
16R4-7	16R4-7-PLCC	20	PLCC		3.8	ChipSite		
16R4-7	16R4-7-PLCC	20	PLCC		3.8	PinSite	0201	
16R4A	16R4A-LCC	20	LCC		1.7	ChipSite		
16R4A	16R4A-LCC	20	LCC		3.0	PinSite	0202	
16R4A-2	16R4A-2-LCC	20	LCC		1.7	ChipSite		
16R4A-2	16R4A-2-LCC	20	LCC		3.0	PinSite	0202	
16R4A/A-2	16R4A/A-2	20	DIP		1.7	Site 48/40		
16R6-10	16R6-10	20	DIP		2.3	Site 48/40		
16R6-10	16R6-10-PLCC	20	PLCC		2.3	ChipSite		
16R6-10	16R6-10-PLCC	20	PLCC		3.0	PinSite	0201	
16R6-12	16R6-12-PLCC	20	PLCC		1.7	ChipSite		
16R6-12	16R6-12-PLCC	20	PLCC		3.0	PinSite	0201	
16R6-12/15/25	16R612/15/25	20	DIP		1.7	Site 48/40		
16R6-15	16R6-15-PLCC	20	PLCC		1.7	ChipSite		
16R6-15	16R6-15-PLCC	20	PLCC		3.0	PinSite	0201	
16R6-25	16R6-25-PLCC	20	PLCC		1.7	ChipSite		
16R6-25	16R6-25-PLCC	20	PLCC		3.0	PinSite	0201	
16R6-5	16R6-5	20	DIP		3.8	Site 48/40		
16R6-5	16R6-5-LCC	20	LCC	44	3.8	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
16R6-5	16R6-5-LCC	20	LCC	44	3.8	PinSite	0202	
16R6-5	16R6-5-PLCC	20	PLCC		3.1	ChipSite		
16R6-5	16R6-5-PLCC	20	PLCC		3.1	PinSite	0201	
16R6-7	16R6-7	20	DIP		3.8	Site 48/40		
16R6-7	16R6-7-PLCC	20	PLCC		3.8	ChipSite		
16R6-7	16R6-7-PLCC	20	PLCC		3.8	PinSite	0201	
16R6A	16R6A-LCC	20	LCC		1.7	ChipSite		
16R6A	16R6A-LCC	20	LCC		3.0	PinSite	0202	
16R6A-2	16R6A-2-LCC	20	LCC		1.7	ChipSite		
16R6A-2	16R6A-2-LCC	20	LCC		3.0	PinSite	0202	
16R6A/A-2	16R6A/A-2	20	DIP		1.7	Site 48/40		
16R8-10	16R8-10	20	DIP		2.3	Site 48/40		
16R8-10	16R8-10-PLCC	20	PLCC		2.3	ChipSite		
16R8-10	16R8-10-PLCC	20	PLCC		3.0	PinSite	0201	
16R8-12	16R8-12-PLCC	20	PLCC		1.7	ChipSite		
16R8-12	16R8-12-PLCC	20	PLCC		3.0	PinSite	0201	
16R8-12/15/25	16R812/15/25	20	DIP		1.7	Site 48/40		
16R8-15	16R8-15-PLCC	20	PLCC		1.7	ChipSite		
16R8-15	16R8-15-PLCC	20	PLCC		3.0	PinSite	0201	
16R8-25	16R8-25-PLCC	20	PLCC		1.7	ChipSite		
16R8-25	16R8-25-PLCC	20	PLCC		3.0	PinSite	0201	
16R8-5	16R8-5	20	DIP		3.8	Site 48/40		
16R8-5	16R8-5-LCC	20	LCC	44	3.8	ChipSite		
16R8-5	16R8-5-LCC	20	LCC	44	3.8	PinSite	0202	
16R8-5	16R8-5-PLCC	20	PLCC		3.8	ChipSite		
16R8-5	16R8-5-PLCC	20	PLCC		3.8	PinSite	0201	
16R8-7	16R8-7	20	DIP		3.8	Site 48/40		
16R8-7	16R8-7-PLCC	20	PLCC		3.8	ChipSite		
16R8-7	16R8-7-PLCC	20	PLCC		3.8	PinSite	0201	
16R8A	16R8A-LCC	20	LCC		1.7	ChipSite		
16R8A	16R8A-LCC	20	LCC		3.0	PinSite	0202	
16R8A-2	16R8A-2-LCC	20	LCC		1.7	ChipSite		
16R8A-2	16R8A-2-LCC	20	LCC		3.0	PinSite	0202	
16R8A/A-2	16R8A/A-2	20	DIP		1.7	Site 48/40		
1810-45	1810-45-JLCC	68	JLCC		3.2	ChipSite		
1810-45	1810-45-JLCC	68	JLCC		3.2	PinSite	0201	
1810-45	1810-45-PLCC	68	PLCC		2.7	ChipSite		
1810-45	1810-45-PLCC	68	PLCC		3.0	PinSite	0201	
1830	1830-JLCC	68	JLCC		4.2	ChipSite		
1830	1830-JLCC	68	JLCC		4.2	PinSite	0201	
1830	1830-PLCC	68	PLCC		4.2	ChipSite		
1830	1830-PLCC	68	PLCC		4.2	PinSite	0201	
18N8	18N8	20	DIP		2.3	Site 48/40		
18N8	18N8-PLCC	20	PLCC		2.3	ChipSite		
18N8	18N8-PLCC	20	PLCC		3.0	PinSite	0201	
18S030	18S030	16	DIP		2.2	Site 48/40		
18SA030	18SA030	16	DIP		2.2	Site 48/40		
20L10	20L10	24	DIP		3.0	Site 48/40		
20L10-FN	20L10-FN	28	PLCC		3.0	ChipSite		
20L10-FN	20L10-FN	28	PLCC		3.0	PinSite	0201	
20L10-NL	20L10-NL	28	PLCC		3.0	ChipSite		
20L10-NL	20L10-NL	28	PLCC		3.0	PinSite	0201	
20L8-10	20L8-10	24	DIP		3.8	Site 48/40		
20L8-10	20L8-10-PLCC	28	PLCC		3.8	ChipSite		
20L8-10	20L8-10-PLCC	28	PLCC		3.8	PinSite	0201	
20L8-15	20L8-15	24	DIP		2.3	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
20L8-15-FN	20L8-15-FN	28	PLCC		2.3	ChipSite		
20L8-15-FN	20L8-15-FN	28	PLCC		3.0	PinSite	0201	
20L8-15-NL	20L8-15-NL	28	PLCC		2.3	ChipSite		
20L8-15-NL	20L8-15-NL	28	PLCC		3.0	PinSite	0201	
20L8-25	20L8-25	24	DIP		2.3	Site 48/40		
20L8-25-FN	20L8-25-FN	28	PLCC		2.3	ChipSite		
20L8-25-FN	20L8-25-FN	28	PLCC		3.0	PinSite	0201	
20L8-25-NL	20L8-25-NL	28	PLCC		2.3	ChipSite		
20L8-25-NL	20L8-25-NL	28	PLCC		3.0	PinSite	0201	
20L8-5	20L8-5	24	DIP		4.2	PinSite	9901	5102
20L8-5	20L8-5	24	DIP		3.8	Site 48/40		
20L8-5	20L8-5-LCC	28	LCC	44	3.8	ChipSite		
20L8-5	20L8-5-LCC	28	LCC	44	3.8	PinSite	0202	
20L8-5	20L8-5-PLCC	28	PLCC		3.8	ChipSite		
20L8-5	20L8-5-PLCC	28	PLCC		3.8	PinSite	0201	
20L8-7	20L8-7	24	DIP		3.8	Site 48/40		
20L8-7	20L8-7-PLCC	28	PLCC		3.8	ChipSite		
20L8-7	20L8-7-PLCC	28	PLCC		3.8	PinSite	0201	
20L8A	20L8A	24	DIP		1.7	Site 48/40		
20L8A	20L8A-FN	28	PLCC		1.7	ChipSite		
20L8A	20L8A-FN	28	PLCC		3.0	PinSite	0201	
20R4-10	20R4-10	24	DIP		3.8	Site 48/40		
20R4-10	20R4-10-FN	28	PLCC		3.8	ChipSite		
20R4-10	20R4-10-FN	28	PLCC		3.8	PinSite	0201	
20R4-15	20R4-15	24	DIP		2.3	Site 48/40		
20R4-15-FN	20R4-15-FN	28	PLCC		2.3	ChipSite		
20R4-15-FN	20R4-15-FN	28	PLCC		3.0	PinSite	0201	
20R4-15-NL	20R4-15-NL	28	PLCC		2.3	ChipSite		
20R4-15-NL	20R4-15-NL	28	PLCC		3.0	PinSite	0201	
20R4-25	20R4-25	24	DIP		2.3	Site 48/40		
20R4-25-FN	20R4-25-FN	28	PLCC		2.3	ChipSite		
20R4-25-FN	20R4-25-FN	28	PLCC		3.0	PinSite	0201	
20R4-25-NL	20R4-25-NL	28	PLCC		2.3	ChipSite		
20R4-25-NL	20R4-25-NL	28	PLCC		3.0	PinSite	0201	
20R4-5	20R4-5	24	DIP		3.8	Site 48/40		
20R4-5	20R4-5-LCC	28	LCC	44	3.8	ChipSite		
20R4-5	20R4-5-LCC	28	LCC	44	3.8	PinSite	0202	
20R4-5	20R4-5-PLCC	28	PLCC		3.8	ChipSite		
20R4-5	20R4-5-PLCC	28	PLCC		3.8	PinSite	0201	
20R4-7	20R4-7	24	DIP		3.8	Site 48/40		
20R4-7	20R4-7-FN	28	PLCC		3.8	ChipSite		
20R4-7	20R4-7-FN	28	PLCC		3.8	PinSite	0201	
20R4A	20R4A	24	DIP		1.7	Site 48/40		
20R4A	20R4A-FN	28	PLCC		1.7	ChipSite		
20R4A	20R4A-FN	28	PLCC		3.0	PinSite	0201	
20R6-10	20R6-10	24	DIP		3.8	Site 48/40		
20R6-10	20R6-10-FN	28	PLCC		3.8	ChipSite		
20R6-10	20R6-10-FN	28	PLCC		3.8	PinSite	0201	
20R6-15	20R6-15	24	DIP		2.3	Site 48/40		
20R6-15-FN	20R6-15-FN	28	PLCC		2.3	ChipSite		
20R6-15-FN	20R6-15-FN	28	PLCC		3.0	PinSite	0201	
20R6-15-NL	20R6-15-NL	28	PLCC		2.3	ChipSite		
20R6-15-NL	20R6-15-NL	28	PLCC		3.0	PinSite	0201	
20R6-25	20R6-25	24	DIP		2.3	Site 48/40		
20R6-25-FN	20R6-25-FN	28	PLCC		2.3	ChipSite		
20R6-25-FN	20R6-25-FN	28	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
20R6-25-NL	20R6-25-NL	28	PLCC		2.3	ChipSite		
20R6-25-NL	20R6-25-NL	28	PLCC		3.0	PinSite	0201	
20R6-5	20R6-5	24	DIP		3.8	Site 48/40		
20R6-5	20R6-5-LCC	28	LCC	44	3.8	ChipSite		
20R6-5	20R6-5-LCC	28	LCC	44	3.8	PinSite	0202	
20R6-5	20R6-5-PLCC	28	PLCC		3.8	ChipSite		
20R6-5	20R6-5-PLCC	28	PLCC		3.8	PinSite	0201	
20R6-7	20R6-7	24	DIP		3.8	Site 48/40		
20R6-7	20R6-7-FN	28	PLCC		3.8	ChipSite		
20R6-7	20R6-7-FN	28	PLCC		3.8	PinSite	0201	
20R6A	20R6A	24	DIP		1.7	Site 48/40		
20R6A	20R6A-FN	28	PLCC		1.7	ChipSite		
20R6A	20R6A-FN	28	PLCC		3.0	PinSite	0201	
20R8-10	20R8-10	24	DIP		3.8	Site 48/40		
20R8-10/12/20	20R8-10-FN	28	PLCC		3.8	ChipSite		
20R8-10/12/20	20R8-10-FN	28	PLCC		3.8	PinSite	0201	
20R8-15	20R8-15	24	DIP		2.3	Site 48/40		
20R8-15-FN	20R8-15-FN	28	PLCC		2.3	ChipSite		
20R8-15-FN	20R8-15-FN	28	PLCC		3.0	PinSite	0201	
20R8-15-NL	20R8-15-NL	28	PLCC		2.3	ChipSite		
20R8-15-NL	20R8-15-NL	28	PLCC		3.0	PinSite	0201	
20R8-25	20R8-25	24	DIP		2.3	Site 48/40		
20R8-25-FN	20R8-25-FN	28	PLCC		2.3	ChipSite		
20R8-25-FN	20R8-25-FN	28	PLCC		3.0	PinSite	0201	
20R8-25-NL	20R8-25-NL	28	PLCC		2.3	ChipSite		
20R8-25-NL	20R8-25-NL	28	PLCC		3.0	PinSite	0201	
20R8-5	20R8-5	24	DIP		4.2	PinSite	9901	5102
20R8-5	20R8-5	24	DIP		3.8	Site 48/40		
20R8-5	20R8-5-LCC	28	LCC	44	3.8	ChipSite		
20R8-5	20R8-5-LCC	28	LCC	44	3.8	PinSite	0202	
20R8-5	20R8-5-PLCC	28	PLCC		3.8	ChipSite		
20R8-5	20R8-5-PLCC	28	PLCC		3.8	PinSite	0201	
20R8-7	20R8-7	24	DIP		3.8	Site 48/40		
20R8-7	20R8-7-FN	28	PLCC		3.8	ChipSite		
20R8-7	20R8-7-FN	28	PLCC		3.8	PinSite	0201	
20R8A	20R8A	24	DIP		1.7	Site 48/40		
20R8A	20R8A-FN	28	PLCC		1.7	ChipSite		
20R8A	20R8A-FN	28	PLCC		3.0	PinSite	0201	
20X10	20X10	24	DIP		3.0	Site 48/40		
20X10-FN	20X10-FN	28	PLCC		3.0	ChipSite		
20X10-FN	20X10-FN	28	PLCC		3.0	PinSite	0201	
20X10-NL	20X10-NL	28	PLCC		3.0	ChipSite		
20X10-NL	20X10-NL	28	PLCC		3.0	PinSite	0201	
20X4	20X4	24	DIP		3.0	Site 48/40		
20X4-FN	20X4-FN	28	PLCC		3.0	ChipSite		
20X4-FN	20X4-FN	28	PLCC		3.0	PinSite	0201	
20X4-NL	20X4-NL	28	PLCC		3.0	ChipSite		
20X4-NL	20X4-NL	28	PLCC		3.0	PinSite	0201	
20X8	20X8	24	DIP		3.0	Site 48/40		
20X8-FN	20X8-FN	28	PLCC		3.0	ChipSite		
20X8-FN	20X8-FN	28	PLCC		3.0	PinSite	0201	
20X8-NL	20X8-NL	28	PLCC		3.0	ChipSite		
20X8-NL	20X8-NL	28	PLCC		3.0	PinSite	0201	
22V10-10	22V10-10	24	DIP		4.1	Site 48/40		
22V10-10	22V10-10PLCC	28	PLCC		4.2	ChipSite		
22V10-10	22V10-10PLCC	28	PLCC		4.2	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
22V10-5	22V10-5-PLCC	28	PLCC		4.0	PinSite	0201	
22V10-7	22V10-7	24	DIP		3.7	Site 48/40		
22V10-7	22V10-7-FN	28	PLCC		3.7	ChipSite		
22V10-7	22V10-7-FN	28	PLCC		3.7	PinSite	0201	
22V10/A-FN	22V10/A-FN	28	PLCC		3.6	ChipSite		
22V10/A-FN	22V10/A-FN	28	PLCC		3.6	PinSite	0201	
22V10/A/B-15	22V10/A/-15B	24	DIP		3.6	Site 48/40		
22V10B-15-FN	22V10-15B-FN	28	PLCC		3.6	ChipSite		
22V10B-15-FN	22V10-15B-FN	28	PLCC		3.6	PinSite	0201	
22VP10	22VP10	24	DIP		3.6	Site 48/40		
22VP10-FN	22VP10-FN	28	PLCC		3.6	ChipSite		
22VP10-FN	22VP10-FN	28	PLCC		3.6	PinSite	0201	
24S10	24S10	16	DIP		1.0	Site 48/40		
24S41	24S41	18	DIP		1.0	Site 48/40		
24S81	24S81	18	DIP		1.0	Site 48/40		
24SA10	24SA10	16	DIP		1.0	Site 48/40		
24SA41	24SA41	18	DIP		1.0	Site 48/40		
24SA81	24SA81	18	DIP		1.0	Site 48/40		
2508	2508	24	DIP		2.8	SetSite		
2508	2508	24	DIP		2.0	Site 48/40		
2516	2516	24	DIP		2.0	SetSite		
2516	2516	24	DIP		2.0	Site 48/40		
2532	2532	24	DIP		2.0	SetSite		
2532	2532	24	DIP		1.1	Site 48/40		
2532A	2532A	24	DIP		2.0	SetSite		
2532A	2532A	24	DIP		1.5	Site 48/40		
2564	2564	28	DIP		2.0	SetSite		
2564	2564	28	DIP		1.1	Site 48/40		
2708	2708	24	DIP		2.0	SetSite		
2708	2708	24	DIP		2.0	Site 48/40		
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		2.0	Site 48/40		
27128A	27128A	28	DIP		2.1	SetSite		
27128A	27128A	28	DIP		2.1	Site 48/40		
27256	27256	28	DIP		2.1	SetSite		
27256	27256	28	DIP		2.1	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		1.2	Site 48/40		
2732A-HS	2732A	24	DIP		2.0	SetSite		
2732A-HS	2732A	24	DIP		1.6	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		
27C010	27C010	32	DIP		2.5	SetSite		
27C010	27C010	32	DIP		2.5	Site 48/40		
27C010A	27C010A	32	DIP		4.1	SetSite		
27C010A	27C010A	32	DIP		4.1	Site 48/40		
27C010A	27PC010A-PLC	32	PLCC		3.6	ChipSite		
27C010A	27PC010A-PLC	32	PLCC		3.6	PinSite	0201	
27C020	27C020	32	DIP		3.9	SetSite		
27C020	27C020	32	DIP		3.9	Site 48/40		
27C040	27C040	32	DIP		3.6	SetSite		
27C040	27C040	32	DIP		3.4	Site 48/40		
27C128	27C128	28	DIP		2.2	SetSite		
27C128	27C128	28	DIP		2.2	Site 48/40		
27C210	27C210	40	DIP		2.7	SetSite		
27C210	27C210	40	DIP		2.7	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
27C210A	27C210A	40	DIP		3.7	SetSite		
27C210A	27C210A	40	DIP		3.4	Site 48/40		
27C210A	27PC210A-PLC	44	PLCC		3.6	ChipSite		
27C210A	27PC210A-PLC	44	PLCC		3.6	PinSite	0201	
27C240	27C240	40	DIP		3.7	SetSite		
27C240	27C240	40	DIP		3.6	Site 48/40		
27C256	27C256	28	DIP		4.2	SetSite		
27C256	27C256	28	DIP		4.2	Site 48/40		
27C291	27C291	24	DIP		1.7	Site 48/40		
27C291	27C291-PLCC	28	PLCC		1.6	ChipSite		
27C291	27C291-PLCC	28	PLCC		3.0	PinSite	0201	
27C292	27C292	24	DIP		1.7	Site 48/40		
27C32	27C32	24	DIP		2.3	SetSite		
27C32	27C32	24	DIP		2.3	Site 48/40		
27C400	27C400	40	DIP		4.1	Site 48/40		
27C49	27C49	24	DIP		3.0	Site 48/40		
27C510	27C510	32	DIP		3.5	Site 48/40		
27C512	27C512	28	DIP		4.0	SetSite		
27C512	27C512	28	DIP		4.0	Site 48/40		
27C64	27C64	28	DIP		2.8	SetSite		
27C64	27C64	28	DIP		2.2	Site 48/40		
27L08	27L08	24	DIP		2.0	SetSite		
27L08	27L08	24	DIP		2.0	Site 48/40		
27P32A	27P32A	24	DIP		2.0	SetSite		
27P32A	27P32A	24	DIP		1.5	Site 48/40		
27P64	27P64	28	DIP		2.0	SetSite		
27P64	27P64	28	DIP		2.0	Site 48/40		
27PC040	27PC040-PLCC	32	PLCC		3.7	ChipSite		
27PC040	27PC040-PLCC	32	PLCC		3.7	PinSite	0201	
27PC128	27PC128	28	DIP		2.2	SetSite		
27PC128	27PC128	28	DIP		2.2	Site 48/40		
27PC128	27PC128-PLCC	32	PLCC		2.2	ChipSite		
27PC128	27PC128-PLCC	32	PLCC		3.0	PinSite	0201	
27PC240	27PC240-PLCC	44	PLCC		3.7	ChipSite		
27PC240	27PC240-PLCC	44	PLCC		3.7	PinSite	0201	
27PC256	27PC256	28	DIP		4.2	SetSite		
27PC256	27PC256	28	DIP		4.2	Site 48/40		
27PC256	27PC256-PLCC	32	PLCC		4.2	ChipSite		
27PC256	27PC256-PLCC	32	PLCC		4.2	PinSite	0201	
27PC32	27PC32	24	DIP		2.3	SetSite		
27PC32	27PC32	24	DIP		2.3	Site 48/40		
27PC512	27PC512	28	DIP		4.0	SetSite		
27PC512	27PC512	28	DIP		4.0	Site 48/40		
27PC512	27PC512-PLCC	32	PLCC		4.0	ChipSite		
27PC512	27PC512-PLCC	32	PLCC		4.0	PinSite	0201	
27PC64	27PC64	28	DIP		2.2	SetSite		
27PC64	27PC64	28	DIP		2.2	Site 48/40		
28F010	28F010	32	DIP		4.2	Site 48/40		
28F010	28F010-PLCC	32	PLCC		4.2	ChipSite		
28F010	28F010-PLCC	32	PLCC		4.2	PinSite	0201	
28F210	28F210	40	DIP		4.2	Site 48/40		
28F512	28F512	32	DIP		4.2	Site 48/40		
28F512	28F512-PLCC	32	PLCC		4.2	ChipSite		
28F512	28F512-PLCC	32	PLCC		4.2	PinSite	0201	
28L22	28L22	20	DIP		1.0	Site 48/40		
28L42	28L42	20	DIP		1.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
28L45	28L45	24	DIP		1.0	Site 48/40		
28L85	28L85	24	DIP		1.0	Site 48/40		
28L86	28L86	24	DIP		1.0	Site 48/40		
28LA22	28LA22	20	DIP		1.0	Site 48/40		
28P42	28P42	20	DIP		1.3	Site 48/40		
28S166	28S166	24	DIP		1.0	Site 48/40		
28S2708	28S2708	24	DIP		2.0	Site 48/40		
28S42	28S42	20	DIP		1.0	Site 48/40		
28S45	28S45	24	DIP		1.0	Site 48/40		
28S46	28S46	24	DIP		1.0	Site 48/40		
28S85	28S85	24	DIP		1.0	Site 48/40		
28S86	28S86	24	DIP		1.0	Site 48/40		
28SA166	28SA166	24	DIP		1.0	Site 48/40		
28SA42	28SA42	20	DIP		1.0	Site 48/40		
28SA46	28SA46	24	DIP		1.0	Site 48/40		
28SA86	28SA86	24	DIP		1.0	Site 48/40		
29F256	29F256	28	DIP		4.0	Site 48/40		
29F256	29F256-PLCC	32	PLCC		4.0	ChipSite		
29F256	29F256-PLCC	32	PLCC		4.0	PinSite	0201	
29F259	29F259	32	DIP		4.0	Site 48/40		
29F259	29F259-PLCC	32	PLCC		4.0	ChipSite		
29F259	29F259-PLCC	32	PLCC		4.0	PinSite	0201	
320E14	320E14-JLCC	68	JLCC	2	3.8	PinSite	0201	
320E15	320E15	40	DIP		2.7	Site 48/40		
320E15	320E15-JLCC	44	JLCC		2.8	ChipSite		
320E15	320E15-JLCC	44	JLCC		3.0	PinSite	0201	
320E17	320E17	40	DIP	2	2.7	Site 48/40		
320E17	320E17-JLCC	44	JLCC	2	4.2	PinSite	0201	
320E25	320E25-JLCC	68	JLCC	2	3.8	PinSite	0201	
320P14	320P14-PLCC	68	PLCC	2	4.2	ChipSite		
320P14	320P14-PLCC	68	PLCC	2	4.2	PinSite	0201	
320P15	320P15	40	DIP	2	4.2	Site 48/40		
320P15	320P15-PLCC	44	PLCC	2	4.2	PinSite	0201	
320P17	320P17	40	DIP	2	4.2	Site 48/40		
320P17	320P17-PLCC	44	PLCC	2	3.8	PinSite	0201	
330	330	20	DIP	194	3.3	Site 48/40		
330	330-PLCC	20	PLCC	194	3.3	ChipSite		
330	330-PLCC	20	PLCC	194	3.3	PinSite	0201	
34L10	34L10	16	DIP		2.2	Site 48/40		
34L12	34L12-PLCC	20	PLCC		2.2	ChipSite		
34L12	34L12-PLCC	20	PLCC		3.0	PinSite	0201	
34L162	34L162	20	DIP		2.2	Site 48/40		
34L162	34L162-PLCC	20	PLCC		2.2	ChipSite		
34L162	34L162-PLCC	20	PLCC		3.0	PinSite	0201	
34L41	34L41	18	DIP		2.2	Site 48/40		
34R162	34R162	20	DIP		2.2	Site 48/40		
34R42	34R42-PLCC	20	PLCC		3.0	ChipSite		
34R42	34R42-PLCC	20	PLCC		3.0	PinSite	0201	
34S10	34S10	16	DIP		2.2	Site 48/40		
34S12	34S12-PLCC	20	PLCC		2.2	ChipSite		
34S12	34S12-PLCC	20	PLCC		3.0	PinSite	0201	
34S162	34S162	20	DIP		2.2	Site 48/40		
34S162	34S162-PLCC	20	PLCC		2.2	ChipSite		
34S162	34S162-PLCC	20	PLCC		3.0	PinSite	0201	
34S41	34S41	18	DIP		2.2	Site 48/40		
34SA10	34SA10	16	DIP		2.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
34SA12	34SA12-PLCC	20	PLCC		2.2	ChipSite		
34SA12	34SA12-PLCC	20	PLCC		3.0	PinSite	0201	
34SA162	34SA162	20	DIP		2.2	Site 48/40		
34SA162	34SA162-PLCC	20	PLCC		2.2	ChipSite		
34SA162	34SA162-PLCC	20	PLCC		3.0	PinSite	0201	
34SA41	34SA41	18	DIP		2.2	Site 48/40		
34SR165	34SR165	24	DIP		2.2	Site 48/40		
34SR167	34SR167-PLCC	28	PLCC		2.2	ChipSite		
34SR167	34SR167-PLCC	28	PLCC		3.0	PinSite	0201	
38L165	38L165	24	DIP		2.2	Site 48/40		
38L166	38L166	24	DIP		2.2	Site 48/40		
38L167	38L167-PLCC	28	PLCC		2.2	ChipSite		
38L167	38L167-PLCC	28	PLCC		3.0	PinSite	0201	
38L22	38L22	20	DIP		2.2	Site 48/40		
38L22	38L22-PLCC	20	PLCC		2.2	ChipSite		
38L22	38L22-PLCC	20	PLCC		3.0	PinSite	0201	
38R165	38R165	24	DIP	1	2.2	Site 48/40		
38S030	38S030	16	DIP		2.2	Site 48/40		
38S165	38S165	24	DIP		2.2	Site 48/40		
38S22	38S22	20	DIP		2.2	Site 48/40		
38S22	38S22-PLCC	20	PLCC		2.2	ChipSite		
38S22	38S22-PLCC	20	PLCC		3.0	PinSite	0201	
38SA030	38SA030	16	DIP		2.2	Site 48/40		
38SA165	38SA165	24	DIP		2.2	Site 48/40		
38SA22	38SA22	20	DIP		2.2	Site 48/40		
38SA22	38SA22-PLCC	20	PLCC		2.2	ChipSite		
38SA22	38SA22-PLCC	20	PLCC		3.0	PinSite	0201	
506/A	FPLS506	24	DIP		3.6	Site 48/40		
506/A	FPLS506-PLCC	28	PLCC		2.7	ChipSite		
506/A	FPLS506-PLCC	28	PLCC		3.0	PinSite	0201	
507/A	FPLS507	24	DIP		3.6	Site 48/40		
507/A	FPLS507-PLCC	28	PLCC		2.7	ChipSite		
507/A	FPLS507-PLCC	28	PLCC		3.0	PinSite	0201	
529	FPGA529	20	DIP		2.2	Site 48/40		
54ALS526	54ALS526	20	DIP		2.5	Site 48/40		
54ALS527	54ALS527	20	DIP		2.5	Site 48/40		
54ALS528	54ALS528	16	DIP		2.5	Site 48/40		
54ALS812	54ALS812	24	DIP		2.5	Site 48/40		
610	610	24	DIP	37	2.7	Site 48/40		
610	610-JLCC	28	JLCC	37	3.2	ChipSite		
610	610-JLCC	28	JLCC	37	3.2	PinSite	0201	
610	610-PLCC	28	PLCC	37	2.7	ChipSite		
610	610-PLCC	28	PLCC	37	3.0	PinSite	0201	
630	630	24	DIP		3.3	Site 48/40		
630	630-PLCC	28	PLCC		3.3	ChipSite		
630	630-PLCC	28	PLCC		3.3	PinSite	0201	
74ALS526	74ALS526	20	DIP		2.5	Site 48/40		
74ALS527	74ALS527	20	DIP		3.0	Site 48/40		
74ALS528	74ALS528	16	DIP		2.5	Site 48/40		
74ALS812	74ALS812	24	DIP		2.5	Site 48/40		
7742	7742	40	DIP		1.1	Site 48/40		
77C82	77C82-PLCC	44	PLCC		3.4	PinSite	0201	
77C82NL	77C82	40	DIP		3.4	Site 48/40		
82S105A/B	82S105A/B	28	DIP		2.6	Site 48/40		
82S105A/B	82S105-PLCC	28	PLCC		2.8	ChipSite		
82S105A/B	82S105-PLCC	28	PLCC		3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
82S167	82S167B	24	DIP		2.5	Site 48/40		
82S191B	82S191B	24	DIP		2.2	Site 48/40		
839	FPLA839	24	DIP		1.3	Site 48/40		
839	FPLA839-PLCC	28	PLCC		1.3	ChipSite		
839	FPLA839-PLCC	28	PLCC		3.0	PinSite	0201	
840	FPLA840	24	DIP		1.3	Site 48/40		
840	FPLA840-PLCC	28	PLCC		1.3	ChipSite		
840	FPLA840-PLCC	28	PLCC		3.0	PinSite	0201	
87C257	87C257	28	DIP		2.8	Site 48/40		
910	910	40	DIP		2.7	Site 48/40		
910	910-JLCC	44	JLCC		3.2	ChipSite		
910	910-JLCC	44	JLCC		3.2	PinSite	0201	
910	910-PLCC	44	PLCC		2.7	ChipSite		
910	910-PLCC	44	PLCC		3.0	PinSite	0201	
C16L8	C16L8	20	DIP		2.2	Site 48/40		
C16R4	C16R4	20	DIP		2.2	Site 48/40		
C16R6	C16R6	20	DIP		2.2	Site 48/40		
C16R8	C16R8	20	DIP		2.2	Site 48/40		
C22V10T	C22V10-T	24	DIP		3.0	Site 48/40		
C22V10T	C22V10-T-FN	28	PLCC		3.0	ChipSite		
C22V10T	C22V10-T-FN	28	PLCC		3.0	PinSite	0201	
C22V10ZP	C22V10-ZP	24	DIP		3.0	Site 48/40		
C22V10ZP	C22V10-ZP-FN	28	PLCC		3.0	ChipSite		
C22V10ZP	C22V10-ZP-FN	28	PLCC		3.0	PinSite	0201	
R19L8	R19L8	24	DIP		2.5	Site 48/40		
R19L8	R19L8-PLCC	28	PLCC		2.5	ChipSite		
R19L8	R19L8-PLCC	28	PLCC		3.0	PinSite	0201	
R19R4	R19R4	24	DIP		2.5	Site 48/40		
R19R4	R19R4-PLCC	28	PLCC		2.5	ChipSite		
R19R4	R19R4-PLCC	28	PLCC		3.0	PinSite	0201	
R19R6	R19R6	24	DIP		2.5	Site 48/40		
R19R6	R19R6-PLCC	28	PLCC		2.5	ChipSite		
R19R6	R19R6-PLCC	28	PLCC		3.0	PinSite	0201	
R19R8	R19R8	24	DIP		2.5	Site 48/40		
R19R8	R19R8-PLCC	28	PLCC		2.5	ChipSite		
R19R8	R19R8-PLCC	28	PLCC		3.0	PinSite	0201	
SE370C710FZ	SE370C710FZ	28	JLCC	140,131,188,132	4.0	PinSite	0201	
SE370C710JD	SE370C710JD	28	DIP	140,131,188,132	4.0	Site 48		
SE370C742FZ	SE370C742FZ	44	JLCC	140,131,188,132	4.0	PinSite	0201	
SE370C742JD	SE370C742JD	40	DIP	140,131,188,132	4.0	Site 48		
SE370C756FZ	SE370C756FZ	68	JLCC	140,131,188,132	4.0	PinSite	0201	
T19L8	T19L8	24	DIP		2.5	Site 48/40		
T19L8	T19L8-PLCC	28	PLCC		2.5	ChipSite		
T19L8	T19L8-PLCC	28	PLCC		3.0	PinSite	0201	
T19R4	T19R4	24	DIP		2.5	Site 48/40		
T19R4	T19R4-PLCC	28	PLCC		2.5	ChipSite		
T19R4	T19R4-PLCC	28	PLCC		3.0	PinSite	0201	
T19R6	T19R6	24	DIP		2.5	Site 48/40		
T19R6	T19R6-PLCC	28	PLCC		2.5	ChipSite		
T19R6	T19R6-PLCC	28	PLCC		3.0	PinSite	0201	
T19R8	T19R8	24	DIP		2.5	Site 48/40		
T19R8	T19R8-PLCC	28	PLCC		2.5	ChipSite		
T19R8	T19R8-PLCC	28	PLCC		3.0	PinSite	0201	
TMS2716	TMS2716	24	DIP		2.6	SetSite		
TMS2716	TMS2716	24	DIP		2.5	Site 48/40		
TMS370C610FN	TMS370C610FN	28	PLCC	140,131,188,132	4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Texas Instruments (continued)								
TMS370C610N	TMS370C610N	28	DIP	140,131,188,132	4.0	Site 48		
TMS370C642N	TMS370C642N	40	DIP	140,131,188,132	4.0	Site 48		
TMS370C710FN	TMS370C710FN	28	PLCC	140,131,188,132	4.0	PinSite	0201	
TMS370C710N	TMS370C710N	28	DIP	140,131,188,132	4.0	Site 48		
TMS370C742FN	TMS370C742FN	44	PLCC	140,131,188,132	4.0	PinSite	0201	
TMS370C742N	TMS370C742N	40	DIP	140,131,188,132	4.0	Site 48		
TMS370C742N2	TMS370C742N2	40	SDIP	140,131,188,132	4.0	PinSite	9901	0602
TMS370C756FN	TMS370C756FN	68	PLCC	140,131,188,132	4.0	PinSite	0201	
TPC1010AFN-044	1010A-44GANG	44	PLCC	39,216	4.2	PinSite	0201	
TPC1010AFN-044	1010A-44GANG	44	PLCC	39	4.2	USM-340-002		
TPC1010AFN-068	1010AFN-068	68	PLCC	39,216	4.2	PinSite	0201	
TPC1010AFN-068	1010AFN-068	68	PLCC	39	3.4	USM-340-001		
TPC1010AMGB84	1010AMGB84	85	PGA	39,216	4.2	PinSite	0402/0401	
TPC1010AVE-100	1010AVE-100	100	QFP	39,216	4.2	PinSite	9901	0522
TPC1010BFN-044	1010B-44GANG	44	PLCC	39,216	4.2	PinSite	0201	
TPC1010BFN-044	1010B-44GANG	44	PLCC	39	4.2	USM-340-002		
TPC1010BFN-068	1010B-68GANG	68	PLCC	39,216	4.2	PinSite	0201	
TPC1010BFN-068	1010B-68GANG	68	PLCC	39	4.2	USM-340-001		
TPC1010BVE-100	1010BVE-100	100	QFP	39,216	4.2	PinSite	9901	0522
TPC1020AFN-044	1020A-44GANG	44	PLCC	39,216	4.2	PinSite	0201	
TPC1020AFN-044	1020A-44GANG	44	PLCC	39	4.2	USM-340-002		
TPC1020AFN-068	1020AFN-068	68	PLCC	39,216	4.2	PinSite	0201	
TPC1020AFN-068	1020AFN-068	68	PLCC	39	3.4	USM-340-001		
TPC1020AFN-084	1020AFN-084	84	PLCC	39,216	4.2	PinSite	0201	
TPC1020AFN-084	1020AFN-084	84	PLCC	39	4.0	USM-340-002		
TPC1020AMGB84	1020AMGB84	85	PGA	39,216	4.2	PinSite	0402/0401	
TPC1020AMHT84	1020AMHT84	84	QFPCAR	39,216	4.2	PinSite	9901	0529
TPC1225AVE-100	1225AVE-100	100	QFP	39,192,216	4.2	PinSite	9901	0522
TPC1240GB-133	1240GB-133	133	PGA	39,192,216	4.2	PinSite	9901	0402
TPC1240VE-144	1240VE-144	144	QFP	39,192,216	4.2	PinSite	9901	0523
TPC1280GB-176	1280GB-176	176	PGA	39,192,216	4.2	PinSite	9901	0402
TPC1280VB-160	1280VB-160	160	QFP	39,192,216	4.2	PinSite	9901	0524
Toshiba America								
24128	24128	28	DIP		2.0	SetSite		
24128	24128	28	DIP		2.0	Site 48/40		
24128A	24128A	28	DIP		2.0	SetSite		
24128A	24128A	28	DIP		2.0	Site 48/40		
24128A	24128A-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
24256	24256	28	DIP		2.0	SetSite		
24256	24256	28	DIP		2.0	Site 48/40		
24256A	24256A	28	DIP		2.0	SetSite		
24256A	24256A	28	DIP		2.0	Site 48/40		
24256A	24256A-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
24512	24512	28	DIP		2.2	SetSite		
24512	24512	28	DIP		2.2	Site 48/40		
2464	2464	28	DIP		2.0	SetSite		
2464	2464	28	DIP		2.0	Site 48/40		
2464A	2464A	28	DIP		2.0	SetSite		
2464A	2464A	28	DIP		2.0	Site 48/40		
2464A	2464A-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
27128	27128	28	DIP		2.0	SetSite		
27128	27128	28	DIP		2.0	Site 48/40		
27128A	27128A	28	DIP		2.0	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Toshiba America (continued)								
27128A	27128A	28	DIP		2.0	Site 48/40		
27256	27256	28	DIP		2.0	SetSite		
27256	27256	28	DIP		2.0	Site 48/40		
27256A	27256A	28	DIP		2.0	SetSite		
27256A	27256A	28	DIP		2.0	Site 48/40		
27256B	27256B	28	DIP		2.2	SetSite		
27256B	27256B	28	DIP		2.2	Site 48/40		
2732	2732	24	DIP		2.0	SetSite		
2732	2732	24	DIP		2.0	Site 48/40		
2732A	2732A	24	DIP		2.0	SetSite		
2732A	2732A	24	DIP		2.0	Site 48/40		
27512	27512	28	DIP		2.2	SetSite		
27512	27512	28	DIP		2.2	Site 48/40		
27512A	27512A	28	DIP		2.2	SetSite		
27512A	27512A	28	DIP		2.2	Site 48/40		
2764	2764	28	DIP		2.0	SetSite		
2764	2764	28	DIP		2.0	Site 48/40		
2764A	2764A	28	DIP		2.0	SetSite		
2764A	2764A	28	DIP		2.0	Site 48/40		
541001A	541001A	32	DIP		4.2	Site 48/40		
541001A	541001A-SOIC	32	SO		4.2	PinSite	0302	.420 SOIC
541001F	541001F-SOIC	32	SO		3.9	PinSite	0302	.420 SOIC
54256A	54256A	28	DIP		2.0	SetSite		
54256A	54256A	28	DIP		2.0	Site 48/40		
54256A	54256A-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
544000	544000-SOIC	32	SO		4.2	PinSite	0302	.420 SOIC
544200	544200-SOIC	40	SO		3.9	PinSite	0302	.420 SOIC
54512A	54512A-SOIC	28	SO		3.9	PinSite	0302/0301	.350 SOIC
571000	571000	32	DIP		2.0	SetSite		
571000	571000	32	DIP		2.0	Site 48/40		
571000A	571000A	32	DIP		3.1	Site 48/40		
571001	571001	32	DIP		2.0	SetSite		
571001	571001	32	DIP		2.0	Site 48/40		
571001A	571001A	32	DIP		3.3	Site 48/40		
571024	571024	40	DIP		2.8	SetSite		
571024	571024	40	DIP		2.1	Site 48/40		
5716200	5716200	42	DIP		3.8	Site 48		
57256	57256	28	DIP		2.0	SetSite		
57256	57256	28	DIP		2.0	Site 48/40		
57256A	57256A	28	DIP		3.0	SetSite		
57256A	57256A	28	DIP		3.0	Site 48/40		
574000	574000	32	DIP		2.7	SetSite		
574000	574000	32	DIP		2.5	Site 48/40		
574096	574096	40	DIP		3.6	SetSite		
574096	574096	40	DIP		3.4	Site 48/40		
574200	574200	40	DIP		3.1	Site 48/40		
57512A	57512A	28	DIP		2.8	SetSite		
57512A	57512A	28	DIP		2.3	Site 48/40		
578200D-150	578200	42	DIP		3.8	Site 48		
578200D-200	578200	42	DIP		3.8	Site 48		
57H1000A	57H1000A	32	DIP		3.3	SetSite		
57H1000A	57H1000A	32	DIP		3.3	Site 48/40		
57H1001A	57H1001A	32	DIP		3.6	Site 48/40		
57H1024	57H1024	40	DIP		2.8	SetSite		
57H1024	57H1024	40	DIP		2.5	Site 48/40		
57H1024A	57H1024A	40	DIP		3.5	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Toshiba America (continued)								
57H1025A	57H1025A	40	DIP		3.2	Site 48/40		
57H1026	57H1026	40	DIP		3.6	Site 48/40		
57H256	57H256	28	DIP		2.5	Site 48/40		
58257A	58257A	28	DIP		4.0	Site 48/40		
58257A	58257A-SOIC	28	SO		4.0	PinSite	0302/0301	.350 SOIC
58257A-LV	58257A-LV	28	DIP		2.8	Site 48/40		
58F010	58F010	32	DIP		4.2	Site 48/40		
58F1001	58F1001	32	DIP		4.0	Site 48/40		
8755A	8755A	40	DIP		1.5	Site 48/40		
89101P	89101	8	DIP		4.0	Site 48/40		
89102P	89102	8	DIP		4.0	Site 48/40		
89112P	89112	8	DIP		4.0	Site 48/40		
89113P	89113	8	DIP		4.0	Site 48/40		
89121AM	89121A-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
89121AP	89121A	8	DIP		4.0	Site 48/40		
89121M	89121-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
89121P	89121	8	DIP		4.0	Site 48/40		
89122AM	89122A-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
89122AP	89122A	8	DIP		4.0	Site 48/40		
89122M	89122-SOIC	8	SO		4.0	PinSite	0302/0301	.150 SOIC
89122P	89122	8	DIP		4.0	Site 48/40		
972010	972010-PLCC	44	PLCC		4.0	ChipSite		
972010	972010-PLCC	44	PLCC		4.0	PinSite	0201	
97208	97208	32	DIP		4.0	Site 48/40		
97208A	97208A	32	DIP		4.0	Site 48/40		
97209	97209	32	DIP		4.0	Site 48/40		
97209	97209-PLCC	32	PLCC		4.0	ChipSite		
97209	97209-PLCC	32	PLCC		4.0	PinSite	0201	
97218	97218	32	DIP		4.0	Site 48/40		
97218A	97218A	32	DIP		4.0	Site 48/40		
9800P	9800	20	DIP		2.8	Site 48/40		
9800P	9800-SOIC	20	SO		4.2	PinSite	0302/0301	.300 SOIC
9801P	9801	20	DIP		2.8	Site 48/40		
9806P	9806	20	DIP		4.2	Site 48/40		
9808P	9808	20	DIP		3.9	Site 48/40		
VLSI Technology, Inc.								
16V8	16V8	20	DIP	22,49	1.7	Site 48/40		
16V8	16V8-PLCC	20	PLCC	22,49	1.7	ChipSite		
16V8	16V8-PLCC	20	PLCC	22,49	3.0	PinSite	0201	
16V8	16V8-SOIC	20	SO	22,49	1.7	ChipSite		
16V8	16V8-SOIC	20	SO	22,49	3.0	PinSite	0302/0301	.300 SOIC
20V8	20V8	24	DIP	22,49	1.5	Site 48/40		
20V8	20V8-SOIC	24	SO	22,49	1.5	ChipSite		
20V8	20V8-SOIC	24	SO	22,49	3.0	PinSite	0302/0301	.300 SOIC
20V8	20V8-PLCC	28	PLCC	22,49	1.5	ChipSite		
20V8	20V8-PLCC	28	PLCC	22,49	3.0	PinSite	0201	
27C128	27C128	28	DIP		2.1	SetSite		
27C128	27C128	28	DIP		2.1	Site 48/40		
27C256	27C256	28	DIP		2.1	SetSite		
27C256	27C256	28	DIP		2.1	Site 48/40		
27C512	27C512	28	DIP		2.0	SetSite		
27C512	27C512	28	DIP		2.0	Site 48/40		
27C64	27C64	28	DIP		2.0	SetSite		
27C64	27C64	28	DIP		1.7	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Waferscale Integration, Inc.								
27C010L	27C010L	32	DIP		4.1	SetSite		
27C010L	27C010L	32	DIP		4.1	Site 48/40		
27C010L	27C010L-LCC	32	LCC	44	4.1	ChipSite		
27C010L	27C010L-LCC	32	LCC	44	4.1	PinSite	0202	
27C010L	27C010L-PLCC	32	PLCC		4.1	ChipSite		
27C010L	27C010L-PLCC	32	PLCC		4.1	PinSite	0201	
27C010R	27C010R	32	DIP		4.1	SetSite		
27C010R	27C010R	32	DIP		4.1	Site 48/40		
27C128F	27C128F	28	DIP		2.0	SetSite		
27C128F	27C128F	28	DIP		2.0	Site 48/40		
27C128F	27C128F-LCC	32	LCC	44	2.4	ChipSite		
27C128F	27C128F-LCC	32	LCC	44	3.0	PinSite	0202	
27C128L	27C128L	28	DIP		4.1	SetSite		
27C128L	27C128L	28	DIP		4.1	Site 48/40		
27C128L	27C128L-JLCC	32	JLCC		4.1	ChipSite		
27C128L	27C128L-JLCC	32	JLCC		4.1	PinSite	0201	
27C128L	27C128L-PLCC	32	PLCC		4.1	ChipSite		
27C128L	27C128L-PLCC	32	PLCC		4.1	PinSite	0201	
27C191	27C191	28	DIP		2.8	SetSite		
27C191	27C191	28	DIP		2.0	Site 48/40		
27C210L	27C210L	40	DIP		4.1	Site 48/40		
27C210L	27C210L-JLCC	44	JLCC		4.1	ChipSite		
27C210L	27C210L-JLCC	44	JLCC		4.1	PinSite	0201	
27C210L	27C210L-PLCC	44	PLCC		4.1	ChipSite		
27C210L	27C210L-PLCC	44	PLCC		4.1	PinSite	0201	
27C256F	27C256F	28	DIP		3.0	SetSite		
27C256F	27C256F	28	DIP		2.4	Site 48/40		
27C256F	27C256F-LCC	32	LCC	44	2.4	ChipSite		
27C256F	27C256F-LCC	32	LCC	44	3.0	PinSite	0202	
27C256L	27C256L	28	DIP		4.1	SetSite		
27C256L	27C256L	28	DIP		4.1	Site 48/40		
27C256L	27C256L-LCC	32	LCC	44	4.1	ChipSite		
27C256L	27C256L-LCC	32	LCC	44	4.1	PinSite	0202	
27C256L	27C256L-PLCC	32	PLCC		4.1	ChipSite		
27C256L	27C256L-PLCC	32	PLCC		4.1	PinSite	0201	
27C291	27C291	24	DIP		2.0	SetSite		
27C291	27C291	24	DIP		2.0	Site 48/40		
27C43	27C43	24	DIP		2.0	SetSite		
27C43	27C43	24	DIP		2.0	Site 48/40		
27C49	27C49	24	DIP		2.0	SetSite		
27C49	27C49	24	DIP		2.0	Site 48/40		
27C51	27C51	28	DIP		2.0	SetSite		
27C51	27C51	28	DIP		2.0	Site 48/40		
27C512F	27C512F	28	DIP		2.5	Site 48/40		
27C512L	27C512L	28	DIP		4.1	Site 48/40		
27C512L	27C512L-LCC	32	LCC	44	4.1	ChipSite		
27C512L	27C512L-LCC	32	LCC	44	4.1	PinSite	0202	
27C512L	27C512L-PLCC	32	PLCC		4.1	ChipSite		
27C512L	27C512L-PLCC	32	PLCC		4.1	PinSite	0201	
27C64F	27C64F	28	DIP		2.0	SetSite		
27C64F	27C64F	28	DIP		2.0	Site 48/40		
27C64L	27C64L	28	DIP		4.1	Site 48/40		
27C64L	27C64L-JLCC	32	JLCC		4.1	ChipSite		
27C64L	27C64L-JLCC	32	JLCC		4.1	PinSite	0201	
27C64L	27C64L-PLCC	32	PLCC		4.1	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Waferscale Integration, Inc. (continued)								
27C64L	27C64L-PLCC	32	PLCC		4.1	PinSite	0201	
27C65	27C65	40	DIP		2.0	Site 48/40		
448	448	28	DIP	49,86	2.6	Site 48/40		
448	448-JLCC	28	JLCC	49,86	2.6	ChipSite		
448	448-JLCC	28	JLCC	49,86	3.0	PinSite	0201	
448	448-PLCC	28	PLCC	49,86	4.1	ChipSite		
448	448-PLCC	28	PLCC	49,86	4.1	PinSite	0201	
57C128F	57C128F	28	DIP		2.8	SetSite		
57C128F	57C128F	28	DIP		2.5	Site 48/40		
57C128F	57C128F-JLCC	32	JLCC		3.8	ChipSite		
57C128F	57C128F-JLCC	32	JLCC		3.8	PinSite	0201	
57C128F	57C128F-LCC	32	LCC	44	2.4	ChipSite		
57C128F	57C128F-LCC	32	LCC	44	3.0	PinSite	0202	
57C128FB	57C128FB	28	DIP		3.9	SetSite		
57C128FB	57C128FB	28	DIP		3.9	Site 48/40		
57C128FB	57C128FB-PLC	32	PLCC		3.9	ChipSite		
57C128FB	57C128FB-PLC	32	PLCC		3.9	PinSite	0201	
57C191B	57C191B	24	DIP	19	2.8	SetSite		
57C191B	57C191B	24	DIP	19	2.5	Site 48/40		
57C191B	57C191B-PLCC	28	PLCC		2.5	ChipSite		
57C191B	57C191B-PLCC	28	PLCC		3.0	PinSite	0201	
57C191C	57C191C	24	DIP		2.5	Site 48/40		
57C191C	57C191C-LCC	28	LCC		4.2	PinSite	0202	
57C191C	57C191C-PLCC	28	PLCC		4.2	ChipSite		
57C191C	57C191C-PLCC	28	PLCC		4.2	PinSite	0201	
57C256F	57C256F	28	DIP		2.4	Site 48/40		
57C256F	57C256F-LCC	32	LCC	44	2.4	ChipSite		
57C256F	57C256F-LCC	32	LCC	44	3.0	PinSite	0202	
57C256FB	57C256FB-PLC	32	PLCC		3.9	ChipSite		
57C256FB	57C256FB-PLC	32	PLCC		3.9	PinSite	0201	
57C256FB-T	57C256FB	28	DIP		3.9	Site 48/40		
57C257	57C257	40	DIP		2.4	Site 48/40		
57C257	57C257-LCC	44	LCC	44	2.4	ChipSite		
57C257	57C257-LCC	44	LCC	44	3.0	PinSite	0202	
57C257	57C257-PLCC	44	PLCC		2.5	ChipSite		
57C257	57C257-PLCC	44	PLCC		3.0	PinSite	0201	
57C291	57C291	24	DIP		2.8	SetSite		
57C291	57C291	24	DIP		2.5	Site 48/40		
57C291BT	57C291BT	24	DIP		2.5	Site 48/40		
57C291CT	57C291CT	24	DIP		2.5	Site 48/40		
57C43	57C43	24	DIP		2.0	SetSite		
57C43	57C43	24	DIP		2.0	Site 48/40		
57C43B	57C43B	24	DIP	19	2.5	SetSite		
57C43B	57C43B	24	DIP	19	2.5	Site 48/40		
57C43B	57C43B-PLCC	28	PLCC	19	2.5	ChipSite		
57C43B	57C43B-PLCC	28	PLCC	19	3.0	PinSite	0201	
57C43BT	57C43BT	24	DIP	19	2.5	Site 48/40		
57C43C	57C43C	24	DIP		3.8	Site 48/40		
57C43C	57C43C-PLCC	28	PLCC		3.8	ChipSite		
57C43C	57C43C-PLCC	28	PLCC		3.8	PinSite	0201	
57C45	57C45	24	DIP	3	2.7	Site 48/40		
57C45	57C45-LCC	28	LCC	3,44	3.7	ChipSite		
57C45	57C45-LCC	28	LCC	3,44	3.7	PinSite	0202	
57C45BT	57C45BT	24	DIP		3.6	Site 48/40		
57C45T	57C45T	24	DIP		3.6	Site 48/40		
57C49	57C49	24	DIP		2.0	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Waferscale Integration, Inc. (continued)								
57C49	57C49	24	DIP		2.0	Site 48/40		
57C49	57C49-LCC	28	LCC	44	2.5	ChipSite		
57C49	57C49-LCC	28	LCC	44	3.0	PinSite	0202	
57C49B	57C49B-LCC	28	LCC	19,44	2.5	ChipSite		
57C49B	57C49B-LCC	28	LCC	19,44	3.0	PinSite	0202	
57C49B	57C49B-PLCC	28	PLCC	19	2.5	ChipSite		
57C49B	57C49B-PLCC	28	PLCC	19	3.0	PinSite	0201	
57C49BD	57C49B	24	DIP	19	2.8	SetSite		
57C49BD	57C49B	24	DIP	19	2.5	Site 48/40		
57C49BT	57C49BT	24	DIP	19	2.5	Site 48/40		
57C49C	57C49C	24	DIP		3.7	Site 48/40		
57C49C	57C49C-PLCC	28	PLCC		3.8	ChipSite		
57C49C	57C49C-PLCC	28	PLCC		3.8	PinSite	0201	
57C51	57C51	28	DIP		2.0	SetSite		
57C51	57C51	28	DIP		2.0	Site 48/40		
57C51B	57C51B	28	DIP		3.0	SetSite		
57C51B	57C51B	28	DIP		2.5	Site 48/40		
57C51B	57C51B-LCC	32	LCC	44	2.5	ChipSite		
57C51B	57C51B-LCC	32	LCC	44	3.0	PinSite	0202	
57C51BT	57C51BT	28	DIP		2.5	SetSite		
57C51BT	57C51BT	28	DIP		2.5	Site 48/40		
57C51C	57C51C	28	DIP		3.9	SetSite		
57C51C	57C51C	28	DIP		3.4	Site 48/40		
57C51C	57C51C-JLCC	32	JLCC		3.8	ChipSite		
57C51C	57C51C-JLCC	32	JLCC		3.8	PinSite	0201	
57C51C	57C51C-PLCC	32	PLCC		3.8	ChipSite		
57C51C	57C51C-PLCC	32	PLCC		3.8	PinSite	0201	
57C64F	57C64F	28	DIP		2.0	SetSite		
57C64F	57C64F	28	DIP		2.0	Site 48/40		
57C64F	57C64F-LCC	32	LCC	44	2.4	ChipSite		
57C64F	57C64F-LCC	32	LCC	44	3.0	PinSite	0202	
57C65	57C65	40	DIP		2.0	Site 48/40		
57C65	57C65-LCC	44	LCC	44	2.5	ChipSite		
57C65	57C65-LCC	44	LCC	44	3.0	PinSite	0202	
57C71C	57C71C	28	DIP		3.0	Site 48/40		
MAP168	MAP168-LCC	44	LCC	44,47	4.0	ChipSite		
MAP168	MAP168-LCC	44	LCC	44,47	4.0	PinSite	0202	
MAP168	MAP168-PGA	44	PGA	47	4.0	PinSite	0402/0401	
PAC1000	PAC1000-PGA	88	PGA	2	4.2	PinSite	0402/0401	
PSD100	PSD100-LCC	44	LCC	44,47	4.0	ChipSite		
PSD100	PSD100-LCC	44	LCC	44,47	4.0	PinSite	0202	
PSD100	PSD100-PGA	44	PGA	47	4.0	PinSite	0402/0401	
PSD301	PSD301-JLCC	44	JLCC	57	4.2	ChipSite		
PSD301	PSD301-JLCC	44	JLCC	57	4.2	PinSite	0201	
PSD302	PSD302-JLCC	44	PLCC	57	3.8	ChipSite		
PSD302	PSD302-JLCC	44	PLCC	57	3.8	PinSite	0201	
PSD303	PSD303-JLCC	44	JLCC	57	3.8	ChipSite		
PSD303	PSD303-JLCC	44	JLCC	57	3.8	PinSite	0201	
PSD311	PSD311-JLCC	44	JLCC	57	4.2	ChipSite		
PSD311	PSD311-JLCC	44	JLCC	57	4.2	PinSite	0201	
PSD311C1	PSD311C1-PLC	44	PLCC	57	4.2	PinSite	0201	
PSD312	PSD312-JLCC	44	JLCC	57	3.8	ChipSite		
PSD312	PSD312-JLCC	44	JLCC	57	3.8	PinSite	0201	
PSD312C1	PSD312C1-PLC	44	PLCC	57	3.8	PinSite	0201	
PSD313	PSD313-JLCC	44	JLCC	57	3.8	ChipSite		
PSD313	PSD313-JLCC	44	JLCC	57	3.8	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Waferscale Integration, Inc. (continued)								
PSD313C1	PSD313C1-PLC	44	PLCC	57	3.8	PinSite	0201	
Xicor, Inc.								
2001	2001	24	DIP		3.2	Site 48/40		
2004	2004	28	DIP		3.2	Site 48/40		
2004	2004-LCC	32	LCC		3.2	ChipSite		
2004	2004-LCC	32	LCC		3.2	PinSite	0202	
2004	2004-PLCC	32	PLCC		3.2	ChipSite		
2004	2004-PLCC	32	PLCC		3.2	PinSite	0201	
2201A	2201A	18	DIP		3.3	Site 48/40		
2210	2210	18	DIP		3.2	Site 48		
2212	2212	18	DIP		3.2	Site 48		
22C10	22C10	18	DIP		3.3	Site 48		
2402	2402	8	DIP		2.8	Site 48/40		
2404	2404	8	DIP		2.8	Site 48/40		
2444	2444	8	DIP		3.2	Site 48/40		
24C01	24C01	8	DIP		3.2	Site 48/40		
24C01-3	24C01-3	8	DIP	118	3.4	Site 48/40		
24C02	24C02	8	DIP		3.8	Site 48/40		
24C04	24C04	8	DIP		2.8	Site 48/40		
24C04-3	24C04-3	8	DIP	118	3.4	Site 48/40		
24C08-3	24C08-3	8	DIP	118	3.6	Site 48/40		
24C16	24C16	8	DIP		2.8	Site 48/40		
24C16	24C16-SOIC	8	SO		4.1	PinSite	0302/0301	.150 SOIC
24C16-3	24C16-3	8	DIP	118	3.4	Site 48/40		
24LC01	24LC01	8	DIP		3.3	Site 48/40		
24LC04	24LC04	8	DIP		3.3	Site 48/40		
24LC16	24LC16	8	DIP		3.3	Site 48/40		
2804A	2804A	24	DIP		2.1	SetSite		
2804A	2804A	24	DIP		2.1	Site 48/40		
2816A	2816A	24	DIP		2.1	SetSite		
2816A	2816A	24	DIP		2.1	Site 48/40		
2816A	2816A-LCC	32	LCC	44	2.8	ChipSite		
2816A	2816A-LCC	32	LCC	44	3.0	PinSite	0202	
2816A	2816A-PLCC	32	PLCC		2.8	ChipSite		
2816A	2816A-PLCC	32	PLCC		3.0	PinSite	0201	
2816B	2816B	24	DIP		2.8	SetSite		
2816B	2816B	24	DIP		2.5	Site 48/40		
2816B	2816B-LCC	32	LCC	44	2.8	ChipSite		
2816B	2816B-LCC	32	LCC	44	3.0	PinSite	0202	
2816B	2816B-PLCC	32	PLCC		2.5	ChipSite		
2816B	2816B-PLCC	32	PLCC		3.0	PinSite	0201	
2816C	2816C	24	DIP		3.2	SetSite		
2816C	2816C	24	DIP		3.2	Site 48/40		
2816C	2816C-PLCC	32	PLCC		3.3	ChipSite		
2816C	2816C-PLCC	32	PLCC		3.3	PinSite	0201	
28256	28256	28	DIP	36	2.4	SetSite		
28256	28256	28	DIP	36	2.4	Site 48/40		
28256	28256-LCC	32	LCC	36,44	2.8	ChipSite		
28256	28256-LCC	32	LCC	36,44	3.0	PinSite	0202	
28256	28256-PLCC	32	PLCC	36	2.5	ChipSite		
28256	28256-PLCC	32	PLCC	36	3.0	PinSite	0201	
2864A	2864A	28	DIP		2.5	SetSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Xicor, Inc. (continued)								
2864A	2864A	28	DIP		2.5	Site 48/40		
2864A	2864A-LCC	32	LCC	44	2.5	ChipSite		
2864A	2864A-LCC	32	LCC	44	3.0	PinSite	0202	
2864A	2864A-PLCC	32	PLCC		2.5	ChipSite		
2864A	2864A-PLCC	32	PLCC		3.0	PinSite	0201	
2864B	2864B	28	DIP		2.5	SetSite		
2864B	2864B	28	DIP		2.5	Site 48/40		
2864B	2864B-LCC	32	LCC		3.2	ChipSite		
2864B	2864B-LCC	32	LCC		3.2	PinSite	0202	
2864B	2864B-PLCC	32	PLCC		2.8	ChipSite		
2864B	2864B-PLCC	32	PLCC		3.0	PinSite	0201	
2864H	2864H	28	DIP		2.5	SetSite		
2864H	2864H	28	DIP		2.5	Site 48/40		
2864H	2864H-LCC	32	LCC	44	2.8	ChipSite		
2864H	2864H-LCC	32	LCC	44	3.0	PinSite	0202	
2864H	2864H-PLCC	32	PLCC		3.3	ChipSite		
2864H	2864H-PLCC	32	PLCC		3.3	PinSite	0201	
28C010	28C010	32	DIP	36	4.0	Site 48/40		
28C010	28C010-PLCC	32	PLCC	36	4.2	ChipSite		
28C010	28C010-PLCC	32	PLCC	36	4.2	PinSite	0201	
28C256	28C256	28	DIP	36	2.5	SetSite		
28C256	28C256	28	DIP	36	2.5	Site 48/40		
28C256	28C256-PGA	28	PGA	36	3.5	PinSite	0402	
28C256	28C256-LCC	32	LCC	36,44	3.2	ChipSite		
28C256	28C256-LCC	32	LCC	36,44	3.2	PinSite	0202	
28C256	28C256-PLCC	32	PLCC	36	3.2	ChipSite		
28C256	28C256-PLCC	32	PLCC	36	3.2	PinSite	0201	
28C256B	28C256B	28	DIP	36	3.2	SetSite		
28C256B	28C256B	28	DIP	36	3.2	Site 48/40		
28C512	28C512	32	DIP	36	3.6	Site 48/40		
28C512	28C512-LCC	32	LCC	36,44	3.6	ChipSite		
28C512	28C512-LCC	32	LCC	36,44	3.6	PinSite	0202	
28C512	28C512-PLCC	32	PLCC	36	3.6	ChipSite		
28C512	28C512-PLCC	32	PLCC	36	3.6	PinSite	0201	
28C513	28C513-LCC	32	LCC	36,44	3.6	ChipSite		
28C513	28C513-LCC	32	LCC	36,44	3.6	PinSite	0202	
28C513	28C513-PLCC	32	PLCC	36	3.6	ChipSite		
28C513	28C513-PLCC	32	PLCC	36	3.6	PinSite	0201	
28C64	28C64	28	DIP	36	2.5	SetSite		
28C64	28C64	28	DIP	36	2.5	Site 48/40		
28C64	28C64-LCC	32	LCC	36,44	3.3	ChipSite		
28C64	28C64-LCC	32	LCC	36,44	3.3	PinSite	0202	
28C64	28C64-PLCC	32	PLCC	36	3.3	ChipSite		
28C64	28C64-PLCC	32	PLCC	36	3.3	PinSite	0201	
28C64B	28C64B	28	DIP	36	3.2	SetSite		
28C64B	28C64B	28	DIP	36	3.2	Site 48/40		
28HC16	28HC16	24	DIP	36	4.2	Site 48/40		
28HC16	28HC16-SOIC	24	SO	36	4.2	PinSite	0302/0301	.300 SOIC
28HC256	28HC256	28	DIP	36	4.2	Site 48/40		
28HC256	28HC256-PLCC	32	PLCC	36	4.2	ChipSite		
28HC256	28HC256-PLCC	32	PLCC	36	4.2	PinSite	0201	
28HC64	28HC64	28	DIP	36	4.2	Site 48/40		
28HC64	28HC64-SOIC	28	SO	36	4.2	PinSite	0302/0301	.300 SOIC
28HC64	28HC64-LCC	32	LCC	36	4.2	PinSite	0202	
28HC64	28HC64-PLCC	32	PLCC	36	4.2	ChipSite		
28HC64	28HC64-PLCC	32	PLCC	36	4.2	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Xicor, Inc. (continued)								
68C64	68C64	24	DIP		4.0	Site 48/40		
86C64	86C64	24	DIP		4.0	Site 48/40		
88C64	88C64	24	DIP		4.0	Site 48/40		
M28C010	M28C010	32	DIP	147,36	4.0	SetSite		
M28C010	M28C010	32	DIP	147,36	4.0	Site 48/40		
Xilinx								
1736	1736	8	DIP	46	3.0	Site 48/40		
1736A	1736A	8	DIP	46	3.0	Site 48/40		
1736A	1736A-PLCC	20	PLCC	46	3.4	ChipSite		
1736A	1736A-PLCC	20	PLCC	46	3.4	PinSite	0201	
1765	1765	8	DIP	46,99	4.2	Site 48/40		
1765	1765-PLCC	20	PLCC	46,99	4.2	ChipSite		
1765	1765-PLCC	20	PLCC	46,99	4.2	PinSite	0201	
XC17128	XC17128	8	DIP	46,202	4.2	Site 48/40		
XC17128	XC17128-PLCC	20	PLCC	46,202	4.2	ChipSite		
XC17128	XC17128-PLCC	20	PLCC	46,202	4.2	PinSite	0201	
XC1718D	XC1718D	8	DIP	46,210	4.2	Site 48/40		
XC1718D	XC1718D-SOIC	8	SO	46,210	4.2	PinSite	0302/0301	.150 SOIC
XC1718D	XC1718D-PLCC	20	PLCC	46,210	4.2	ChipSite		
XC1718D	XC1718D-PLCC	20	PLCC	46,210	4.2	PinSite	0201	
XC1736D	XC1736D	8	DIP	46,206	4.2	Site 48/40		
XC1736D	XC1736D-SOIC	8	SO	46,206	4.2	PinSite	0302/0301	.150 SOIC
XC1736D	XC1736D-PLCC	20	PLCC	46,206	4.2	ChipSite		
XC1736D	XC1736D-PLCC	20	PLCC	46,206	4.2	PinSite	0201	
XC1765D	XC1765D	8	DIP	46,99	4.2	Site 48/40		
XC1765D	XC1765D-SOIC	8	SO	46,99	4.2	PinSite	0302/0301	.150 SOIC
XC1765D	XC1765D-PLCC	20	PLCC	46,99	4.2	ChipSite		
XC1765D	XC1765D-PLCC	20	PLCC	46,99	4.2	PinSite	0201	
Zilog								
86E08	86E08	18	DIP	201	4.1	Site 48		
86E21	86E21	40	DIP	2,153	2.6	Site 48/40		
86E21	86E21-PLCC	44	PLCC	2,153	3.8	ChipSite		
86E21	86E21-PLCC	44	PLCC	2,153	3.8	PinSite	0201	
86E22	86E22	40	DIP	2,153	3.7	Site 48/40		
86E40	86E40	40	DIP	53	3.9	Site 48/40		
86E40	86E40-PLCC	44	PLCC	53	3.9	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Advanced Micro Devices/MMI CE16V8H-25/4 DIP as:								
CE16L8		20	DIP	49	3.9	Site 48/40		
CE16R4		20	DIP	49	3.9	Site 48/40		
CE16R6		20	DIP	49	3.9	Site 48/40		
CE16R8		20	DIP	49	3.9	Site 48/40		
Advanced Micro Devices/MMI CE16V8H-25/4 PLCC as:								
CE16L8		20	PLCC	49	3.9	ChipSite		
CE16L8		20	PLCC	49	3.9	PinSite	0201	
CE16R4		20	PLCC	49	3.9	ChipSite		
CE16R4		20	PLCC	49	3.9	PinSite	0201	
CE16R6		20	PLCC	49	3.9	ChipSite		
CE16R6		20	PLCC	49	3.9	PinSite	0201	
CE16R8		20	PLCC	49	3.9	ChipSite		
CE16R8		20	PLCC	49	3.9	PinSite	0201	
Advanced Micro Devices/MMI CE20V8H-15/4 DIP as:								
CE20L8		24	DIP	49	3.9	Site 48/40		
CE20R4		24	DIP	49	3.9	Site 48/40		
CE20R6		24	DIP	49	3.9	Site 48/40		
CE20R8		24	DIP	49	3.9	Site 48/40		
Advanced Micro Devices/MMI CE20V8H-15/4 PLCC as:								
CE20L8		28	PLCC	49	3.9	ChipSite		
CE20L8		28	PLCC	49	3.9	PinSite	0201	
CE20R4		28	PLCC	49	3.9	ChipSite		
CE20R4		28	PLCC	49	3.9	PinSite	0201	
CE20R6		28	PLCC	49	3.9	ChipSite		
CE20R6		28	PLCC	49	3.9	PinSite	0201	
CE20R8		28	PLCC	49	3.9	ChipSite		
CE20R8		28	PLCC	49	3.9	PinSite	0201	
Intel Corporation 85C220 DIP as:								
16V8		20	DIP		3.8	Site 48/40		
Intel Corporation 85C220 PLCC as:								
16V8		20	PLCC		3.8	ChipSite		
16V8		20	PLCC		3.8	PinSite	0201	
Intel Corporation 85C224 DIP as:								
20V8		24	DIP		3.8	Site 48/40		
Intel Corporation 85C224 PLCC as:								
20V8		28	PLCC		3.8	ChipSite		
20V8		28	PLCC		3.8	PinSite	0201	
Intel Corporation 85C22V10 DIP as:								
22V10		24	DIP		3.7	Site 48/40		
22V10UES		24	DIP		3.7	Site 48/40		
22VP10		24	DIP		3.7	Site 48/40		
Intel Corporation 85C22V10 PLCC as:								
22V10		28	PLCC		3.7	ChipSite		
22V10		28	PLCC		3.7	PinSite	0201	
22V10UES		28	PLCC		3.7	ChipSite		
22V10UES		28	PLCC		3.7	PinSite	0201	
22VP10		28	PLCC		3.7	ChipSite		
22VP10		28	PLCC		3.7	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Intel Corporation IPLD16V8XP DIP as:								
16V8		20	DIP		3.8	Site 48/40		
Intel Corporation IPLD16V8XP PLCC as:								
16V8		20	PLCC		3.8	ChipSite		
16V8		20	PLCC		3.8	PinSite	0201	
Intel Corporation IPLD20V8XP DIP as:								
20V8		24	DIP		3.8	Site 48/40		
Intel Corporation IPLD20V8XP PLCC as:								
20V8		28	PLCC		3.8	ChipSite		
20V8		28	PLCC		3.8	PinSite	0201	
Lattice Semiconductor 16V8 DIP as:								
10H8		20	DIP	33,49	4.0	Site 48/40		
10L8		20	DIP	33,49	4.0	Site 48/40		
10P8		20	DIP	33,49	4.0	Site 48/40		
12H6		20	DIP	33,49	4.0	Site 48/40		
12L6		20	DIP	33,49	4.0	Site 48/40		
12P6		20	DIP	33,49	4.0	Site 48/40		
14H4		20	DIP	33,49	4.0	Site 48/40		
14L4		20	DIP	33,49	4.0	Site 48/40		
14P4		20	DIP	33,49	4.0	Site 48/40		
16H2		20	DIP	33,49	4.0	Site 48/40		
16H8		20	DIP	33,49	4.0	Site 48/40		
16L2		20	DIP	33,49	4.0	Site 48/40		
16L8		20	DIP	33,49	4.0	Site 48/40		
16P2		20	DIP	33,49	4.0	Site 48/40		
16P8		20	DIP	33,49	4.0	Site 48/40		
16R4		20	DIP	33,49	4.0	Site 48/40		
16R6		20	DIP	33,49	4.0	Site 48/40		
16R8		20	DIP	33,49	4.0	Site 48/40		
16RP4		20	DIP	33,49	4.0	Site 48/40		
16RP6		20	DIP	33,49	4.0	Site 48/40		
16RP8		20	DIP	33,49	4.0	Site 48/40		
Lattice Semiconductor 16V8 PLCC as:								
10H8		20	PLCC	33,49	4.0	ChipSite		
10H8		20	PLCC	33,49	4.0	PinSite	0201	
10L8		20	PLCC	33,49	4.0	ChipSite		
10L8		20	PLCC	33,49	4.0	PinSite	0201	
10P8		20	PLCC	33,49	4.0	ChipSite		
10P8		20	PLCC	33,49	4.0	PinSite	0201	
12H6		20	PLCC	33,49	4.0	ChipSite		
12H6		20	PLCC	33,49	4.0	PinSite	0201	
12L6		20	PLCC	33,49	4.0	ChipSite		
12L6		20	PLCC	33,49	4.0	PinSite	0201	
12P6		20	PLCC	33,49	4.0	ChipSite		
12P6		20	PLCC	33,49	4.0	PinSite	0201	
14H4		20	PLCC	33,49	4.0	ChipSite		
14H4		20	PLCC	33,49	4.0	PinSite	0201	
14L4		20	PLCC	33,49	4.0	ChipSite		
14L4		20	PLCC	33,49	4.0	PinSite	0201	
14P4		20	PLCC	33,49	4.0	ChipSite		
14P4		20	PLCC	33,49	4.0	PinSite	0201	
16H2		20	PLCC	33,49	4.0	ChipSite		
16H2		20	PLCC	33,49	4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor 16V8 PLCC as: (continued)								
16H8		20	PLCC	33,49	4.0	ChipSite		
16H8		20	PLCC	33,49	4.0	PinSite	0201	
16L2		20	PLCC	33,49	4.0	ChipSite		
16L2		20	PLCC	33,49	4.0	PinSite	0201	
16L8		20	PLCC	33,49	4.0	ChipSite		
16L8		20	PLCC	33,49	4.0	PinSite	0201	
16P2		20	PLCC	33,49	4.0	ChipSite		
16P2		20	PLCC	33,49	4.0	PinSite	0201	
16P8		20	PLCC	33,49	4.0	ChipSite		
16P8		20	PLCC	33,49	4.0	PinSite	0201	
16R4		20	PLCC	33,49	4.0	ChipSite		
16R4		20	PLCC	33,49	4.0	PinSite	0201	
16R6		20	PLCC	33,49	4.0	ChipSite		
16R6		20	PLCC	33,49	4.0	PinSite	0201	
16R8		20	PLCC	33,49	4.0	ChipSite		
16R8		20	PLCC	33,49	4.0	PinSite	0201	
16RP4		20	PLCC	33,49	4.0	ChipSite		
16RP4		20	PLCC	33,49	4.0	PinSite	0201	
16RP6		20	PLCC	33,49	4.0	ChipSite		
16RP6		20	PLCC	33,49	4.0	PinSite	0201	
16RP8		20	PLCC	33,49	4.0	ChipSite		
16RP8		20	PLCC	33,49	4.0	PinSite	0201	
Lattice Semiconductor 16V8A DIP as:								
10H8A		20	DIP	33,49	4.0	Site 48/40		
10L8A		20	DIP	33,49	4.0	Site 48/40		
10P8A		20	DIP	33,49	4.0	Site 48/40		
12H6A		20	DIP	33,49	4.0	Site 48/40		
12L6A		20	DIP	33,49	4.0	Site 48/40		
12P6A		20	DIP	33,49	4.0	Site 48/40		
14H4A		20	DIP	33,49	4.0	Site 48/40		
14L4A		20	DIP	33,49	4.0	Site 48/40		
14P4A		20	DIP	33,49	4.0	Site 48/40		
16H2A		20	DIP	33,49	4.0	Site 48/40		
16H8A		20	DIP	33,49	4.0	Site 48/40		
16L2A		20	DIP	33,49	4.0	Site 48/40		
16L8A		20	DIP	33,49	4.0	Site 48/40		
16P2A		20	DIP	33,49	4.0	Site 48/40		
16P8A		20	DIP	33,49	4.0	Site 48/40		
16R4A		20	DIP	33,49	4.0	Site 48/40		
16R6A		20	DIP	33,49	4.0	Site 48/40		
16R8A		20	DIP	33,49	4.0	Site 48/40		
16RP4A		20	DIP	33,49	4.0	Site 48/40		
16RP6A		20	DIP	33,49	4.0	Site 48/40		
16RP8A		20	DIP	33,49	4.0	Site 48/40		
Lattice Semiconductor 16V8A PLCC as:								
10H8A		20	PLCC	33,49	4.0	ChipSite		
10H8A		20	PLCC	33,49	4.0	PinSite	0201	
10L8A		20	PLCC	33,49	4.0	ChipSite		
10L8A		20	PLCC	33,49	4.0	PinSite	0201	
10P8A		20	PLCC	33,49	4.0	ChipSite		
10P8A		20	PLCC	33,49	4.0	PinSite	0201	
12H6A		20	PLCC	33,49	4.0	ChipSite		
12H6A		20	PLCC	33,49	4.0	PinSite	0201	
12L6A		20	PLCC	33,49	4.0	ChipSite		
12L6A		20	PLCC	33,49	4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor 16V8A PLCC as: (continued)								
12P6A		20	PLCC	33,49	4.0	ChipSite		
12P6A		20	PLCC	33,49	4.0	PinSite	0201	
14H4A		20	PLCC	33,49	4.0	ChipSite		
14H4A		20	PLCC	33,49	4.0	PinSite	0201	
14L4A		20	PLCC	33,49	4.0	ChipSite		
14L4A		20	PLCC	33,49	4.0	PinSite	0201	
14P4A		20	PLCC	33,49	4.0	ChipSite		
14P4A		20	PLCC	33,49	4.0	PinSite	0201	
16H2A		20	PLCC	33,49	4.0	ChipSite		
16H2A		20	PLCC	33,49	4.0	PinSite	0201	
16H8A		20	PLCC	33,49	4.0	ChipSite		
16H8A		20	PLCC	33,49	4.0	PinSite	0201	
16L2A		20	PLCC	33,49	4.0	ChipSite		
16L2A		20	PLCC	33,49	4.0	PinSite	0201	
16L8A		20	PLCC	33,49	4.0	ChipSite		
16L8A		20	PLCC	33,49	4.0	PinSite	0201	
16P2A		20	PLCC	33,49	4.0	ChipSite		
16P2A		20	PLCC	33,49	4.0	PinSite	0201	
16P8A		20	PLCC	33,49	4.0	ChipSite		
16P8A		20	PLCC	33,49	4.0	PinSite	0201	
16R4A		20	PLCC	33,49	4.0	ChipSite		
16R4A		20	PLCC	33,49	4.0	PinSite	0201	
16R6A		20	PLCC	33,49	4.0	ChipSite		
16R6A		20	PLCC	33,49	4.0	PinSite	0201	
16R8A		20	PLCC	33,49	4.0	ChipSite		
16R8A		20	PLCC	33,49	4.0	PinSite	0201	
16RP4A		20	PLCC	33,49	4.0	ChipSite		
16RP4A		20	PLCC	33,49	4.0	PinSite	0201	
16RP6A		20	PLCC	33,49	4.0	ChipSite		
16RP6A		20	PLCC	33,49	4.0	PinSite	0201	
16RP8A		20	PLCC	33,49	4.0	ChipSite		
16RP8A		20	PLCC	33,49	4.0	PinSite	0201	
Lattice Semiconductor 16V8B DIP as:								
10H8B		20	DIP	33,49	4.0	Site 48/40		
10L8B		20	DIP	33,49	4.0	Site 48/40		
10P8B		20	DIP	33,49	4.0	Site 48/40		
12H6B		20	DIP	33,49	4.0	Site 48/40		
12L6B		20	DIP	33,49	4.0	Site 48/40		
12P6B		20	DIP	33,49	4.0	Site 48/40		
14H4B		20	DIP	33,49	4.0	Site 48/40		
14L4B		20	DIP	33,49	4.0	Site 48/40		
14P4B		20	DIP	33,49	4.0	Site 48/40		
16H2B		20	DIP	33,49	4.0	Site 48/40		
16H8B		20	DIP	33,49	4.0	Site 48/40		
16L2B		20	DIP	33,49	4.0	Site 48/40		
16L8B		20	DIP	33,49	4.0	Site 48/40		
16P2B		20	DIP	33,49	4.0	Site 48/40		
16P8B		20	DIP	33,49	4.0	Site 48/40		
16R4B		20	DIP	33,49	4.0	Site 48/40		
16R6B		20	DIP	33,49	4.0	Site 48/40		
16R8B		20	DIP	33,49	4.0	Site 48/40		
16RP4B		20	DIP	33,49	4.0	Site 48/40		
16RP6B		20	DIP	33,49	4.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor 16V8B DIP as: (continued)								
16RP8B		20	DIP	33,49	4.0	Site 48/40		
Lattice Semiconductor 16V8B PLCC as:								
10H8B		20	PLCC	33,49	4.0	ChipSite		
10H8B		20	PLCC	33,49	4.0	PinSite	0201	
10L8B		20	PLCC	33,49	4.0	ChipSite		
10L8B		20	PLCC	33,49	4.0	PinSite	0201	
10P8B		20	PLCC	33,49	4.0	ChipSite		
10P8B		20	PLCC	33,49	4.0	PinSite	0201	
12H6B		20	PLCC	33,49	4.0	ChipSite		
12H6B		20	PLCC	33,49	4.0	PinSite	0201	
12L6B		20	PLCC	33,49	4.0	ChipSite		
12L6B		20	PLCC	33,49	4.0	PinSite	0201	
12P6B		20	PLCC	33,49	4.0	ChipSite		
12P6B		20	PLCC	33,49	4.0	PinSite	0201	
14H4B		20	PLCC	33,49	4.0	ChipSite		
14H4B		20	PLCC	33,49	4.0	PinSite	0201	
14L4B		20	PLCC	33,49	4.0	ChipSite		
14L4B		20	PLCC	33,49	4.0	PinSite	0201	
14P4B		20	PLCC	33,49	4.0	ChipSite		
14P4B		20	PLCC	33,49	4.0	PinSite	0201	
16H2B		20	PLCC	33,49	4.0	ChipSite		
16H2B		20	PLCC	33,49	4.0	PinSite	0201	
16H8B		20	PLCC	33,49	4.0	ChipSite		
16H8B		20	PLCC	33,49	4.0	PinSite	0201	
16L2B		20	PLCC	33,49	4.0	ChipSite		
16L2B		20	PLCC	33,49	4.0	PinSite	0201	
16L8B		20	PLCC	33,49	4.0	ChipSite		
16L8B		20	PLCC	33,49	4.0	PinSite	0201	
16P2B		20	PLCC	33,49	4.0	ChipSite		
16P2B		20	PLCC	33,49	4.0	PinSite	0201	
16P8B		20	PLCC	33,49	4.0	ChipSite		
16P8B		20	PLCC	33,49	4.0	PinSite	0201	
16R4B		20	PLCC	33,49	4.0	ChipSite		
16R4B		20	PLCC	33,49	4.0	PinSite	0201	
16R6B		20	PLCC	33,49	4.0	ChipSite		
16R6B		20	PLCC	33,49	4.0	PinSite	0201	
16R8B		20	PLCC	33,49	4.0	ChipSite		
16R8B		20	PLCC	33,49	4.0	PinSite	0201	
16RP4B		20	PLCC	33,49	4.0	ChipSite		
16RP4B		20	PLCC	33,49	4.0	PinSite	0201	
16RP6B		20	PLCC	33,49	4.0	ChipSite		
16RP6B		20	PLCC	33,49	4.0	PinSite	0201	
16RP8B		20	PLCC	33,49	4.0	ChipSite		
16RP8B		20	PLCC	33,49	4.0	PinSite	0201	
Lattice Semiconductor 20V8 DIP as:								
14H8		24	DIP	33,49	4.0	Site 48/40		
14L8		24	DIP	33,49	4.0	Site 48/40		
14P8		24	DIP	33,49	4.0	Site 48/40		
16H6		24	DIP	33,49	4.0	Site 48/40		
16L6		24	DIP	33,49	4.0	Site 48/40		
16P6		24	DIP	33,49	4.0	Site 48/40		
18H4		24	DIP	33,49	4.0	Site 48/40		
18L4		24	DIP	33,49	4.0	Site 48/40		
18P4		24	DIP	33,49	4.0	Site 48/40		
20H2		24	DIP	33,49	4.0	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor 20V8 DIP as: (continued)								
20H8		24	DIP	33,49	4.0	Site 48/40		
20L2		24	DIP	33,49	4.0	Site 48/40		
20L8		24	DIP	33,49	4.0	Site 48/40		
20P2		24	DIP	33,49	4.0	Site 48/40		
20P8		24	DIP	33,49	4.0	Site 48/40		
20R4		24	DIP	33,49	4.0	Site 48/40		
20R6		24	DIP	33,49	4.0	Site 48/40		
20R8		24	DIP	33,49	4.0	Site 48/40		
20RP4		24	DIP	33,49	4.0	Site 48/40		
20RP6		24	DIP	33,49	4.0	Site 48/40		
20RP8		24	DIP	33,49	4.0	Site 48/40		
Lattice Semiconductor 20V8 PLCC as:								
14H8		28	PLCC	33,49	4.0	ChipSite		
14H8		28	PLCC	33,49	4.0	PinSite	0201	
14L8		28	PLCC	33,49	4.0	ChipSite		
14L8		28	PLCC	33,49	4.0	PinSite	0201	
14P8		28	PLCC	33,49	4.0	ChipSite		
14P8		28	PLCC	33,49	4.0	PinSite	0201	
16H6		28	PLCC	33,49	4.0	ChipSite		
16H6		28	PLCC	33,49	4.0	PinSite	0201	
16L6		28	PLCC	33,49	4.0	ChipSite		
16L6		28	PLCC	33,49	4.0	PinSite	0201	
16P6		28	PLCC	33,49	4.0	ChipSite		
16P6		28	PLCC	33,49	4.0	PinSite	0201	
18H4		28	PLCC	33,49	4.0	ChipSite		
18H4		28	PLCC	33,49	4.0	PinSite	0201	
18L4		28	PLCC	33,49	4.0	ChipSite		
18L4		28	PLCC	33,49	4.0	PinSite	0201	
18P4		28	PLCC	33,49	4.0	ChipSite		
18P4		28	PLCC	33,49	4.0	PinSite	0201	
20H2		28	PLCC	33,49	4.0	ChipSite		
20H2		28	PLCC	33,49	4.0	PinSite	0201	
20H8		28	PLCC	33,49	4.0	ChipSite		
20H8		28	PLCC	33,49	4.0	PinSite	0201	
20L2		28	PLCC	33,49	4.0	ChipSite		
20L2		28	PLCC	33,49	4.0	PinSite	0201	
20L8		28	PLCC	33,49	4.0	ChipSite		
20L8		28	PLCC	33,49	4.0	PinSite	0201	
20P2		28	PLCC	33,49	4.0	ChipSite		
20P2		28	PLCC	33,49	4.0	PinSite	0201	
20P8		28	PLCC	33,49	4.0	ChipSite		
20P8		28	PLCC	33,49	4.0	PinSite	0201	
20R4		28	PLCC	33,49	4.0	ChipSite		
20R4		28	PLCC	33,49	4.0	PinSite	0201	
20R6		28	PLCC	33,49	4.0	ChipSite		
20R6		28	PLCC	33,49	4.0	PinSite	0201	
20R8		28	PLCC	33,49	4.0	ChipSite		
20R8		28	PLCC	33,49	4.0	PinSite	0201	
20RP4		28	PLCC	33,49	4.0	ChipSite		
20RP4		28	PLCC	33,49	4.0	PinSite	0201	
20RP6		28	PLCC	33,49	4.0	ChipSite		
20RP6		28	PLCC	33,49	4.0	PinSite	0201	
20RP8		28	PLCC	33,49	4.0	ChipSite		
20RP8		28	PLCC	33,49	4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor 20V8A DIP as:								
14H8A		24	DIP	33,49	4.0	Site 48/40		
14L8A		24	DIP	33,49	4.0	Site 48/40		
14P8A		24	DIP	33,49	4.0	Site 48/40		
16H6A		24	DIP	33,49	4.0	Site 48/40		
16L6A		24	DIP	33,49	4.0	Site 48/40		
16P6A		24	DIP	33,49	4.0	Site 48/40		
18H4A		24	DIP	33,49	4.0	Site 48/40		
18L4A		24	DIP	33,49	4.0	Site 48/40		
18P4A		24	DIP	33,49	4.0	Site 48/40		
20H2A		24	DIP	33,49	4.0	Site 48/40		
20H8A		24	DIP	33,49	4.0	Site 48/40		
20L2A		24	DIP	33,49	4.0	Site 48/40		
20L8A		24	DIP	33,49	4.0	Site 48/40		
20P2A		24	DIP	33,49	4.0	Site 48/40		
20P8A		24	DIP	33,49	4.0	Site 48/40		
20R4A		24	DIP	33,49	4.0	Site 48/40		
20R6A		24	DIP	33,49	4.0	Site 48/40		
20R8A		24	DIP	33,49	4.0	Site 48/40		
20RP4A		24	DIP	33,49	4.0	Site 48/40		
20RP6A		24	DIP	33,49	4.0	Site 48/40		
20RP8A		24	DIP	33,49	4.0	Site 48/40		
Lattice Semiconductor 20V8A PLCC as:								
14H8A		28	PLCC	33,49	4.0	ChipSite		
14H8A		28	PLCC	33,49	4.0	PinSite	0201	
14L8A		28	PLCC	33,49	4.0	ChipSite		
14L8A		28	PLCC	33,49	4.0	PinSite	0201	
14P8A		28	PLCC	33,49	4.0	ChipSite		
14P8A		28	PLCC	33,49	4.0	PinSite	0201	
16H6A		28	PLCC	33,49	4.0	ChipSite		
16H6A		28	PLCC	33,49	4.0	PinSite	0201	
16L6A		28	PLCC	33,49	4.0	ChipSite		
16L6A		28	PLCC	33,49	4.0	PinSite	0201	
16P6A		28	PLCC	33,49	4.0	ChipSite		
16P6A		28	PLCC	33,49	4.0	PinSite	0201	
18H4A		28	PLCC	33,49	4.0	ChipSite		
18H4A		28	PLCC	33,49	4.0	PinSite	0201	
18L4A		28	PLCC	33,49	4.0	ChipSite		
18L4A		28	PLCC	33,49	4.0	PinSite	0201	
18P4A		28	PLCC	33,49	4.0	ChipSite		
18P4A		28	PLCC	33,49	4.0	PinSite	0201	
20H2A		28	PLCC	33,49	4.0	ChipSite		
20H2A		28	PLCC	33,49	4.0	PinSite	0201	
20H8A		28	PLCC	33,49	4.0	ChipSite		
20H8A		28	PLCC	33,49	4.0	PinSite	0201	
20L2A		28	PLCC	33,49	4.0	ChipSite		
20L2A		28	PLCC	33,49	4.0	PinSite	0201	
20L8A		28	PLCC	33,49	4.0	ChipSite		
20L8A		28	PLCC	33,49	4.0	PinSite	0201	
20P2A		28	PLCC	33,49	4.0	ChipSite		
20P2A		28	PLCC	33,49	4.0	PinSite	0201	
20P8A		28	PLCC	33,49	4.0	ChipSite		
20P8A		28	PLCC	33,49	4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor 20V8A PLCC as: (continued)								
20R4A		28	PLCC	33,49	4.0	ChipSite		
20R4A		28	PLCC	33,49	4.0	PinSite	0201	
20R6A		28	PLCC	33,49	4.0	ChipSite		
20R6A		28	PLCC	33,49	4.0	PinSite	0201	
20R8A		28	PLCC	33,49	4.0	ChipSite		
20R8A		28	PLCC	33,49	4.0	PinSite	0201	
20RP4A		28	PLCC	33,49	4.0	ChipSite		
20RP4A		28	PLCC	33,49	4.0	PinSite	0201	
20RP6A		28	PLCC	33,49	4.0	ChipSite		
20RP6A		28	PLCC	33,49	4.0	PinSite	0201	
20RP8A		28	PLCC	33,49	4.0	ChipSite		
20RP8A		28	PLCC	33,49	4.0	PinSite	0201	
Lattice Semiconductor 20V8B DIP as:								
14H8B		24	DIP	33,49	4.0	Site 48/40		
14L8B		24	DIP	33,49	4.0	Site 48/40		
14P8B		24	DIP	33,49	4.0	Site 48/40		
16H6B		24	DIP	33,49	4.0	Site 48/40		
16L6B		24	DIP	33,49	4.0	Site 48/40		
16P6B		24	DIP	33,49	4.0	Site 48/40		
18H4B		24	DIP	33,49	4.0	Site 48/40		
18L4B		24	DIP	33,49	4.0	Site 48/40		
18P4B		24	DIP	33,49	4.0	Site 48/40		
20H2B		24	DIP	33,49	4.0	Site 48/40		
20H8B		24	DIP	33,49	4.0	Site 48/40		
20L2B		24	DIP	33,49	4.0	Site 48/40		
20L8B		24	DIP	33,49	4.0	Site 48/40		
20P2B		24	DIP	33,49	4.0	Site 48/40		
20P8B		24	DIP	33,49	4.0	Site 48/40		
20R4B		24	DIP	33,49	4.0	Site 48/40		
20R6B		24	DIP	33,49	4.0	Site 48/40		
20R8B		24	DIP	33,49	4.0	Site 48/40		
20RP4B		24	DIP	33,49	4.0	Site 48/40		
20RP6B		24	DIP	33,49	4.0	Site 48/40		
20RP8B		24	DIP	33,49	4.0	Site 48/40		
Lattice Semiconductor 20V8B PLCC as:								
14H8B		28	PLCC	33,49	4.0	ChipSite		
14H8B		28	PLCC	33,49	4.0	PinSite	0201	
14L8B		28	PLCC	33,49	4.0	ChipSite		
14L8B		28	PLCC	33,49	4.0	PinSite	0201	
14P8B		28	PLCC	33,49	4.0	ChipSite		
14P8B		28	PLCC	33,49	4.0	PinSite	0201	
16H6B		28	PLCC	33,49	4.0	ChipSite		
16H6B		28	PLCC	33,49	4.0	PinSite	0201	
16L6B		28	PLCC	33,49	4.0	ChipSite		
16L6B		28	PLCC	33,49	4.0	PinSite	0201	
16P6B		28	PLCC	33,49	4.0	ChipSite		
16P6B		28	PLCC	33,49	4.0	PinSite	0201	
18H4B		28	PLCC	33,49	4.0	ChipSite		
18H4B		28	PLCC	33,49	4.0	PinSite	0201	
18L4B		28	PLCC	33,49	4.0	ChipSite		
18L4B		28	PLCC	33,49	4.0	PinSite	0201	
18P4B		28	PLCC	33,49	4.0	ChipSite		
18P4B		28	PLCC	33,49	4.0	PinSite	0201	
20H2B		28	PLCC	33,49	4.0	ChipSite		
20H2B		28	PLCC	33,49	4.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
Lattice Semiconductor 20V8B PLCC as: (continued)								
20H8B		28	PLCC	33,49	4.0	ChipSite		
20H8B		28	PLCC	33,49	4.0	PinSite	0201	
20L2B		28	PLCC	33,49	4.0	ChipSite		
20L2B		28	PLCC	33,49	4.0	PinSite	0201	
20L8B		28	PLCC	33,49	4.0	ChipSite		
20L8B		28	PLCC	33,49	4.0	PinSite	0201	
20P2B		28	PLCC	33,49	4.0	ChipSite		
20P2B		28	PLCC	33,49	4.0	PinSite	0201	
20P8B		28	PLCC	33,49	4.0	ChipSite		
20P8B		28	PLCC	33,49	4.0	PinSite	0201	
20R4B		28	PLCC	33,49	4.0	ChipSite		
20R4B		28	PLCC	33,49	4.0	PinSite	0201	
20R6B		28	PLCC	33,49	4.0	ChipSite		
20R6B		28	PLCC	33,49	4.0	PinSite	0201	
20R8B		28	PLCC	33,49	4.0	ChipSite		
20R8B		28	PLCC	33,49	4.0	PinSite	0201	
20RP4B		28	PLCC	33,49	4.0	ChipSite		
20RP4B		28	PLCC	33,49	4.0	PinSite	0201	
20RP6B		28	PLCC	33,49	4.0	ChipSite		
20RP6B		28	PLCC	33,49	4.0	PinSite	0201	
20RP8B		28	PLCC	33,49	4.0	ChipSite		
20RP8B		28	PLCC	33,49	4.0	PinSite	0201	
National Semiconductor Corp. 16V8 DIP as:								
10H8		20	DIP	33,49	2.2	Site 48/40		
10L8		20	DIP	33,49	2.2	Site 48/40		
10P8		20	DIP	33,49	2.2	Site 48/40		
12H6		20	DIP	33,49	2.2	Site 48/40		
12L6		20	DIP	33,49	2.2	Site 48/40		
12P6		20	DIP	33,49	2.2	Site 48/40		
14H4		20	DIP	33,49	2.2	Site 48/40		
14L4		20	DIP	33,49	2.2	Site 48/40		
14P4		20	DIP	33,49	2.2	Site 48/40		
16H2		20	DIP	33,49	2.2	Site 48/40		
16H8		20	DIP	33,49	2.2	Site 48/40		
16L2		20	DIP	33,49	2.2	Site 48/40		
16L8		20	DIP	33,49	2.2	Site 48/40		
16P2		20	DIP	33,49	2.2	Site 48/40		
16P8		20	DIP	33,49	2.2	Site 48/40		
16R4		20	DIP	33,49	2.2	Site 48/40		
16R6		20	DIP	33,49	2.2	Site 48/40		
16R8		20	DIP	33,49	2.2	Site 48/40		
16RP4		20	DIP	33,49	2.2	Site 48/40		
16RP6		20	DIP	33,49	2.2	Site 48/40		
16RP8		20	DIP	33,49	2.2	Site 48/40		
National Semiconductor Corp. 16V8 PLCC as:								
10H8		20	PLCC	33,49	2.2	ChipSite		
10H8		20	PLCC	33,49	3.0	PinSite	0201	
10L8		20	PLCC	33,49	2.2	ChipSite		
10L8		20	PLCC	33,49	3.0	PinSite	0201	
10P8		20	PLCC	33,49	2.2	ChipSite		
10P8		20	PLCC	33,49	3.0	PinSite	0201	
12H6		20	PLCC	33,49	2.2	ChipSite		
12H6		20	PLCC	33,49	3.0	PinSite	0201	
12L6		20	PLCC	33,49	2.2	ChipSite		
12L6		20	PLCC	33,49	3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. 16V8 PLCC as: (continued)								
12P6		20	PLCC	33,49	2.2	ChipSite		
12P6		20	PLCC	33,49	3.0	PinSite	0201	
14H4		20	PLCC	33,49	2.2	ChipSite		
14H4		20	PLCC	33,49	3.0	PinSite	0201	
14L4		20	PLCC	33,49	2.2	ChipSite		
14L4		20	PLCC	33,49	3.0	PinSite	0201	
14P4		20	PLCC	33,49	2.2	ChipSite		
14P4		20	PLCC	33,49	3.0	PinSite	0201	
16H2		20	PLCC	33,49	2.2	ChipSite		
16H2		20	PLCC	33,49	3.0	PinSite	0201	
16H8		20	PLCC	33,49	2.3	ChipSite		
16H8		20	PLCC	33,49	3.0	PinSite	0201	
16L2		20	PLCC	33,49	2.2	ChipSite		
16L2		20	PLCC	33,49	3.0	PinSite	0201	
16L8		20	PLCC	33,49	2.2	ChipSite		
16L8		20	PLCC	33,49	3.0	PinSite	0201	
16P2		20	PLCC	33,49	2.2	ChipSite		
16P2		20	PLCC	33,49	3.0	PinSite	0201	
16P8		20	PLCC	33,49	2.2	ChipSite		
16P8		20	PLCC	33,49	3.0	PinSite	0201	
16R4		20	PLCC	33,49	2.2	ChipSite		
16R4		20	PLCC	33,49	3.0	PinSite	0201	
16R6		20	PLCC	33,49	2.2	ChipSite		
16R6		20	PLCC	33,49	3.0	PinSite	0201	
16R8		20	PLCC	33,49	2.2	ChipSite		
16R8		20	PLCC	33,49	3.0	PinSite	0201	
16RP4		20	PLCC	33,49	2.2	ChipSite		
16RP4		20	PLCC	33,49	3.0	PinSite	0201	
16RP6		20	PLCC	33,49	2.2	ChipSite		
16RP6		20	PLCC	33,49	3.0	PinSite	0201	
16RP8		20	PLCC	33,49	2.2	ChipSite		
16RP8		20	PLCC	33,49	3.0	PinSite	0201	
National Semiconductor Corp. 16V8A DIP as:								
10H8A		20	DIP	33,49	2.5	Site 48/40		
10L8A		20	DIP	33,49	2.5	Site 48/40		
10P8A		20	DIP	33,49	2.5	Site 48/40		
12H6A		20	DIP	33,49	2.5	Site 48/40		
12L6A		20	DIP	33,49	2.5	Site 48/40		
12P6A		20	DIP	33,49	2.5	Site 48/40		
14H4A		20	DIP	33,49	2.5	Site 48/40		
14L4A		20	DIP	33,49	2.5	Site 48/40		
14P4A		20	DIP	33,49	2.5	Site 48/40		
16H2A		20	DIP	33,49	2.5	Site 48/40		
16H8A		20	DIP	33,49	2.5	Site 48/40		
16L2A		20	DIP	33,49	2.5	Site 48/40		
16L8A		20	DIP	33,49	2.5	Site 48/40		
16P2A		20	DIP	33,49	2.5	Site 48/40		
16P8A		20	DIP	33,49	2.5	Site 48/40		
16R4A		20	DIP	33,49	2.5	Site 48/40		
16R6A		20	DIP	33,49	2.5	Site 48/40		
16R8A		20	DIP	33,49	2.5	Site 48/40		
16RP4A		20	DIP	33,49	2.5	Site 48/40		
16RP6A		20	DIP	33,49	2.5	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. 16V8A DIP as: (continued)								
16RP8A		20	DIP	33,49	2.5	Site 48/40		
National Semiconductor Corp. 20V8 DIP as:								
14H8		24	DIP	33,49	2.2	Site 48/40		
14L8		24	DIP	33,49	2.2	Site 48/40		
14P8		24	DIP	33,49	2.2	Site 48/40		
16H6		24	DIP	33,49	2.2	Site 48/40		
16L6		24	DIP	33,49	2.2	Site 48/40		
16P6		24	DIP	33,49	2.2	Site 48/40		
18H4		24	DIP	33,49	2.2	Site 48/40		
18L4		24	DIP	33,49	2.2	Site 48/40		
18P4		24	DIP	33,49	2.2	Site 48/40		
20H2		24	DIP	33,49	2.2	Site 48/40		
20H8		24	DIP	33,49	2.2	Site 48/40		
20L2		24	DIP	33,49	2.2	Site 48/40		
20L8		24	DIP	33,49	2.2	Site 48/40		
20P2		24	DIP	33,49	2.2	Site 48/40		
20P8		24	DIP	33,49	2.2	Site 48/40		
20R4		24	DIP	33,49	2.2	Site 48/40		
20R6		24	DIP	33,49	2.2	Site 48/40		
20R8		24	DIP	33,49	2.2	Site 48/40		
20RP4		24	DIP	33,49	2.2	Site 48/40		
20RP6		24	DIP	33,49	2.2	Site 48/40		
20RP8		24	DIP	33,49	2.2	Site 48/40		
National Semiconductor Corp. 20V8 PLCC as:								
14H8		28	PLCC	33,49	2.2	ChipSite		
14H8		28	PLCC	33,49	3.0	PinSite	0201	
14L8		28	PLCC	33,49	2.2	ChipSite		
14L8		28	PLCC	33,49	3.0	PinSite	0201	
14P8		28	PLCC	33,49	2.2	ChipSite		
14P8		28	PLCC	33,49	3.0	PinSite	0201	
16H6		28	PLCC	33,49	2.2	ChipSite		
16H6		28	PLCC	33,49	3.0	PinSite	0201	
16L6		28	PLCC	33,49	2.2	ChipSite		
16L6		28	PLCC	33,49	3.0	PinSite	0201	
16P6		28	PLCC	33,49	2.2	ChipSite		
16P6		28	PLCC	33,49	3.0	PinSite	0201	
18H4		28	PLCC	33,49	2.2	ChipSite		
18H4		28	PLCC	33,49	3.0	PinSite	0201	
18L4		28	PLCC	33,49	2.2	ChipSite		
18L4		28	PLCC	33,49	3.0	PinSite	0201	
18P4		28	PLCC	33,49	2.2	ChipSite		
18P4		28	PLCC	33,49	3.0	PinSite	0201	
20H2		28	PLCC	33,49	2.2	ChipSite		
20H2		28	PLCC	33,49	3.0	PinSite	0201	
20H8		28	PLCC	33,49	2.2	ChipSite		
20H8		28	PLCC	33,49	3.0	PinSite	0201	
20L2		28	PLCC	33,49	2.2	ChipSite		
20L2		28	PLCC	33,49	3.0	PinSite	0201	
20L8		28	PLCC	33,49	2.2	ChipSite		
20L8		28	PLCC	33,49	3.0	PinSite	0201	
20P2		28	PLCC	33,49	2.2	ChipSite		
20P2		28	PLCC	33,49	3.0	PinSite	0201	
20P8		28	PLCC	33,49	2.2	ChipSite		
20P8		28	PLCC	33,49	3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
National Semiconductor Corp. 20V8 PLCC as: (continued)								
20R4		28	PLCC	33,49	2.2	ChipSite		
20R4		28	PLCC	33,49	3.0	PinSite	0201	
20R6		28	PLCC	33,49	2.2	ChipSite		
20R6		28	PLCC	33,49	3.0	PinSite	0201	
20R8		28	PLCC	33,49	2.2	ChipSite		
20R8		28	PLCC	33,49	3.0	PinSite	0201	
20RP4		28	PLCC	33,49	2.2	ChipSite		
20RP4		28	PLCC	33,49	3.0	PinSite	0201	
20RP6		28	PLCC	33,49	2.2	ChipSite		
20RP6		28	PLCC	33,49	3.0	PinSite	0201	
20RP8		28	PLCC	33,49	2.2	ChipSite		
20RP8		28	PLCC	33,49	3.0	PinSite	0201	
National Semiconductor Corp. 20V8/A/QS DIP as:								
14H8A		24	DIP	33,49	2.5	Site 48/40		
14L8A		24	DIP	33,49	2.5	Site 48/40		
14P8A		24	DIP	33,49	2.5	Site 48/40		
16H6A		24	DIP	33,49	2.5	Site 48/40		
16L6A		24	DIP	33,49	2.5	Site 48/40		
16P6A		24	DIP	33,49	2.5	Site 48/40		
18H4A		24	DIP	33,49	2.5	Site 48/40		
18L4A		24	DIP	33,49	2.5	Site 48/40		
18P4A		24	DIP	33,49	2.5	Site 48/40		
20H2A		24	DIP	33,49	2.5	Site 48/40		
20H8A		24	DIP	33,49	2.5	Site 48/40		
20L2A		24	DIP	33,49	2.5	Site 48/40		
20L8A		24	DIP	33,49	2.5	Site 48/40		
20P2A		24	DIP	33,49	2.5	Site 48/40		
20P8A		24	DIP	33,49	2.5	Site 48/40		
20R4A		24	DIP	33,49	2.5	Site 48/40		
20R6A		24	DIP	33,49	2.5	Site 48/40		
20R8A		24	DIP	33,49	2.5	Site 48/40		
20RP4A		24	DIP	33,49	2.5	Site 48/40		
20RP6A		24	DIP	33,49	2.5	Site 48/40		
20RP8A		24	DIP	33,49	2.5	Site 48/40		
SGS-Thomson Microelectronics 16V8 DIP as:								
10H8		20	DIP	33,49	2.8	Site 48/40		
10H8A		20	DIP	33,49	2.8	Site 48/40		
10L8		20	DIP	33,49	2.8	Site 48/40		
10L8A		20	DIP	33,49	2.8	Site 48/40		
10P8		20	DIP	33,49	2.8	Site 48/40		
10P8A		20	DIP	33,49	2.8	Site 48/40		
12H6		20	DIP	33,49	2.8	Site 48/40		
12H6A		20	DIP	33,49	2.8	Site 48/40		
12L6		20	DIP	33,49	2.8	Site 48/40		
12L6A		20	DIP	33,49	2.8	Site 48/40		
12P6		20	DIP	33,49	2.8	Site 48/40		
12P6A		20	DIP	33,49	2.8	Site 48/40		
14H4		20	DIP	33,49	2.8	Site 48/40		
14H4A		20	DIP	33,49	2.8	Site 48/40		
14L4		20	DIP	33,49	2.8	Site 48/40		
14L4A		20	DIP	33,49	2.8	Site 48/40		
14P4		20	DIP	33,49	2.8	Site 48/40		
14P4A		20	DIP	33,49	2.8	Site 48/40		
16H2		20	DIP	33,49	2.8	Site 48/40		
16H2A		20	DIP	33,49	2.8	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SGS-Thomson Microelectronics 16V8 DIP as: (continued)								
16H8		20	DIP	33,49	2.8	Site 48/40		
16H8A		20	DIP	33,49	2.8	Site 48/40		
16L2		20	DIP	33,49	2.8	Site 48/40		
16L2A		20	DIP	33,49	2.8	Site 48/40		
16L8		20	DIP	33,49	2.8	Site 48/40		
16L8A		20	DIP	33,49	2.8	Site 48/40		
16P2		20	DIP	33,49	2.8	Site 48/40		
16P2A		20	DIP	33,49	2.8	Site 48/40		
16P8		20	DIP	33,49	2.8	Site 48/40		
16P8A		20	DIP	33,49	2.8	Site 48/40		
16R4		20	DIP	33,49	2.8	Site 48/40		
16R4A		20	DIP	33,49	2.8	Site 48/40		
16R6		20	DIP	33,49	2.8	Site 48/40		
16R6A		20	DIP	33,49	2.8	Site 48/40		
16R8		20	DIP	33,49	2.8	Site 48/40		
16R8A		20	DIP	33,49	2.8	Site 48/40		
16RP4		20	DIP	33,49	2.8	Site 48/40		
16RP4A		20	DIP	33,49	2.8	Site 48/40		
16RP6		20	DIP	33,49	2.8	Site 48/40		
16RP6A		20	DIP	33,49	2.8	Site 48/40		
16RP8		20	DIP	33,49	2.8	Site 48/40		
16RP8A		20	DIP	33,49	2.8	Site 48/40		
SGS-Thomson Microelectronics 16V8 PLCC as:								
10H8		20	PLCC	33,49	2.8	ChipSite		
10H8		20	PLCC	33,49	3.0	PinSite	0201	
10H8A		20	PLCC	33,49	2.8	ChipSite		
10H8A		20	PLCC	33,49	3.0	PinSite	0201	
10L8		20	PLCC	33,49	2.8	ChipSite		
10L8		20	PLCC	33,49	3.0	PinSite	0201	
10L8A		20	PLCC	33,49	2.8	ChipSite		
10L8A		20	PLCC	33,49	3.0	PinSite	0201	
10P8		20	PLCC	33,49	2.8	ChipSite		
10P8		20	PLCC	33,49	3.0	PinSite	0201	
10P8A		20	PLCC	33,49	2.8	ChipSite		
10P8A		20	PLCC	33,49	3.0	PinSite	0201	
12H6		20	PLCC	33,49	2.8	ChipSite		
12H6		20	PLCC	33,49	3.0	PinSite	0201	
12H6A		20	PLCC	33,49	2.8	ChipSite		
12H6A		20	PLCC	33,49	3.0	PinSite	0201	
12L6		20	PLCC	33,49	2.8	ChipSite		
12L6		20	PLCC	33,49	3.0	PinSite	0201	
12L6A		20	PLCC	33,49	2.8	ChipSite		
12L6A		20	PLCC	33,49	3.0	PinSite	0201	
12P6		20	PLCC	33,49	2.8	ChipSite		
12P6		20	PLCC	33,49	3.0	PinSite	0201	
12P6A		20	PLCC	33,49	2.8	ChipSite		
12P6A		20	PLCC	33,49	3.0	PinSite	0201	
14H4		20	PLCC	33,49	2.8	ChipSite		
14H4		20	PLCC	33,49	3.0	PinSite	0201	
14H4A		20	PLCC	33,49	2.8	ChipSite		
14H4A		20	PLCC	33,49	3.0	PinSite	0201	
14L4		20	PLCC	33,49	2.8	ChipSite		
14L4		20	PLCC	33,49	3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SGS-Thomson Microelectronics 16V8 PLCC as: (continued)								
14L4A		20	PLCC	33,49	2.8	ChipSite		
14L4A		20	PLCC	33,49	3.0	PinSite	0201	
14P4		20	PLCC	33,49	2.8	ChipSite		
14P4		20	PLCC	33,49	3.0	PinSite	0201	
14P4A		20	PLCC	33,49	2.8	ChipSite		
14P4A		20	PLCC	33,49	3.0	PinSite	0201	
16H2		20	PLCC	33,49	2.8	ChipSite		
16H2		20	PLCC	33,49	3.0	PinSite	0201	
16H2A		20	PLCC	33,49	2.8	ChipSite		
16H2A		20	PLCC	33,49	3.0	PinSite	0201	
16H8		20	PLCC	33,49	2.8	ChipSite		
16H8		20	PLCC	33,49	3.0	PinSite	0201	
16H8A		20	PLCC	33,49	2.8	ChipSite		
16H8A		20	PLCC	33,49	3.0	PinSite	0201	
16L2		20	PLCC	33,49	2.8	ChipSite		
16L2		20	PLCC	33,49	3.0	PinSite	0201	
16L2A		20	PLCC	33,49	2.8	ChipSite		
16L2A		20	PLCC	33,49	3.0	PinSite	0201	
16L8		20	PLCC	33,49	2.8	ChipSite		
16L8		20	PLCC	33,49	3.0	PinSite	0201	
16L8A		20	PLCC	33,49	2.8	ChipSite		
16L8A		20	PLCC	33,49	3.0	PinSite	0201	
16P2		20	PLCC	33,49	2.8	ChipSite		
16P2		20	PLCC	33,49	3.0	PinSite	0201	
16P2A		20	PLCC	33,49	2.8	ChipSite		
16P2A		20	PLCC	33,49	3.0	PinSite	0201	
16P8		20	PLCC	33,49	2.8	ChipSite		
16P8		20	PLCC	33,49	3.0	PinSite	0201	
16P8A		20	PLCC	33,49	2.8	ChipSite		
16P8A		20	PLCC	33,49	3.0	PinSite	0201	
16R4		20	PLCC	33,49	2.8	ChipSite		
16R4		20	PLCC	33,49	3.0	PinSite	0201	
16R4A		20	PLCC	33,49	2.8	ChipSite		
16R4A		20	PLCC	33,49	3.0	PinSite	0201	
16R6		20	PLCC	33,49	2.8	ChipSite		
16R6		20	PLCC	33,49	3.0	PinSite	0201	
16R6A		20	PLCC	33,49	2.8	ChipSite		
16R6A		20	PLCC	33,49	3.0	PinSite	0201	
16R8		20	PLCC	33,49	2.8	ChipSite		
16R8		20	PLCC	33,49	3.0	PinSite	0201	
16R8A		20	PLCC	33,49	2.8	ChipSite		
16R8A		20	PLCC	33,49	3.0	PinSite	0201	
16RP4		20	PLCC	33,49	2.8	ChipSite		
16RP4		20	PLCC	33,49	3.0	PinSite	0201	
16RP4A		20	PLCC	33,49	2.8	ChipSite		
16RP4A		20	PLCC	33,49	3.0	PinSite	0201	
16RP6		20	PLCC	33,49	2.8	ChipSite		
16RP6		20	PLCC	33,49	3.0	PinSite	0201	
16RP6A		20	PLCC	33,49	2.8	ChipSite		
16RP6A		20	PLCC	33,49	3.0	PinSite	0201	
16RP8		20	PLCC	33,49	2.8	ChipSite		
16RP8		20	PLCC	33,49	3.0	PinSite	0201	
16RP8A		20	PLCC	33,49	2.8	ChipSite		
16RP8A		20	PLCC	33,49	3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SGS-Thomson Microelectronics 20V8 DIP as:								
14H8		24	DIP	33,49	2.8	Site 48/40		
14H8A		24	DIP	33,49	2.8	Site 48/40		
14L8		24	DIP	33,49	2.8	Site 48/40		
14L8A		24	DIP	33,49	2.8	Site 48/40		
14P8		24	DIP	33,49	2.8	Site 48/40		
14P8A		24	DIP	33,49	2.8	Site 48/40		
16H6		24	DIP	33,49	2.8	Site 48/40		
16H6A		24	DIP	33,49	2.8	Site 48/40		
16L6		24	DIP	33,49	2.8	Site 48/40		
16L6A		24	DIP	33,49	2.8	Site 48/40		
16P6		24	DIP	33,49	2.8	Site 48/40		
16P6A		24	DIP	33,49	2.8	Site 48/40		
18H4		24	DIP	33,49	2.8	Site 48/40		
18H4A		24	DIP	33,49	2.8	Site 48/40		
18L4		24	DIP	33,49	2.8	Site 48/40		
18L4A		24	DIP	33,49	2.8	Site 48/40		
18P4		24	DIP	33,49	2.8	Site 48/40		
18P4A		24	DIP	33,49	2.8	Site 48/40		
20H2		24	DIP	33,49	2.8	Site 48/40		
20H2A		24	DIP	33,49	2.8	Site 48/40		
20H8		24	DIP	33,49	2.8	Site 48/40		
20H8A		24	DIP	33,49	2.8	Site 48/40		
20L2		24	DIP	33,49	2.8	Site 48/40		
20L2A		24	DIP	33,49	2.8	Site 48/40		
20L8		24	DIP	33,49	2.8	Site 48/40		
20L8A		24	DIP	33,49	2.8	Site 48/40		
20P2		24	DIP	33,49	2.8	Site 48/40		
20P2A		24	DIP	33,49	2.8	Site 48/40		
20P8		24	DIP	33,49	2.8	Site 48/40		
20P8A		24	DIP	33,49	2.8	Site 48/40		
20R4		24	DIP	33,49	2.8	Site 48/40		
20R4A		24	DIP	33,49	2.8	Site 48/40		
20R6		24	DIP	33,49	2.8	Site 48/40		
20R6A		24	DIP	33,49	2.8	Site 48/40		
20R8		24	DIP	33,49	2.8	Site 48/40		
20R8A		24	DIP	33,49	2.8	Site 48/40		
20RP4		24	DIP	33,49	2.8	Site 48/40		
20RP4A		24	DIP	33,49	2.8	Site 48/40		
20RP6		24	DIP	33,49	2.8	Site 48/40		
20RP6A		24	DIP	33,49	2.8	Site 48/40		
20RP8		24	DIP	33,49	2.8	Site 48/40		
20RP8A		24	DIP	33,49	2.8	Site 48/40		
SGS-Thomson Microelectronics 20V8 PLCC as:								
14H8		28	PLCC	33,49	2.8	ChipSite		
14H8		28	PLCC	33,49	3.0	PinSite	0201	
14H8A		28	PLCC	33,49	2.8	ChipSite		
14H8A		28	PLCC	33,49	3.0	PinSite	0201	
14L8		28	PLCC	33,49	2.8	ChipSite		
14L8		28	PLCC	33,49	3.0	PinSite	0201	
14L8A		28	PLCC	33,49	2.8	ChipSite		
14L8A		28	PLCC	33,49	3.0	PinSite	0201	
14P8		28	PLCC	33,49	2.8	ChipSite		
14P8		28	PLCC	33,49	3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SGS-Thomson Microelectronics 20V8 PLCC as: (continued)								
14P8A		28	PLCC	33,49	2.8	ChipSite		
14P8A		28	PLCC	33,49	3.0	PinSite	0201	
16H6		28	PLCC	33,49	2.8	ChipSite		
16H6		28	PLCC	33,49	3.0	PinSite	0201	
16H6A		28	PLCC	33,49	2.8	ChipSite		
16H6A		28	PLCC	33,49	3.0	PinSite	0201	
16L6		28	PLCC	33,49	2.8	ChipSite		
16L6		28	PLCC	33,49	3.0	PinSite	0201	
16L6A		28	PLCC	33,49	2.8	ChipSite		
16L6A		28	PLCC	33,49	3.0	PinSite	0201	
16P6		28	PLCC	33,49	2.8	ChipSite		
16P6		28	PLCC	33,49	3.0	PinSite	0201	
16P6A		28	PLCC	33,49	2.8	ChipSite		
16P6A		28	PLCC	33,49	3.0	PinSite	0201	
18H4		28	PLCC	33,49	2.8	ChipSite		
18H4		28	PLCC	33,49	3.0	PinSite	0201	
18H4A		28	PLCC	33,49	2.8	ChipSite		
18H4A		28	PLCC	33,49	3.0	PinSite	0201	
18L4		28	PLCC	33,49	2.8	ChipSite		
18L4		28	PLCC	33,49	3.0	PinSite	0201	
18L4A		28	PLCC	33,49	2.8	ChipSite		
18L4A		28	PLCC	33,49	3.0	PinSite	0201	
18P4		28	PLCC	33,49	2.8	ChipSite		
18P4		28	PLCC	33,49	3.0	PinSite	0201	
18P4A		28	PLCC	33,49	2.8	ChipSite		
18P4A		28	PLCC	33,49	3.0	PinSite	0201	
20H2		28	PLCC	33,49	2.8	ChipSite		
20H2		28	PLCC	33,49	3.0	PinSite	0201	
20H2A		28	PLCC	33,49	2.8	ChipSite		
20H2A		28	PLCC	33,49	3.0	PinSite	0201	
20H8		28	PLCC	33,49	2.8	ChipSite		
20H8		28	PLCC	33,49	3.0	PinSite	0201	
20H8A		28	PLCC	33,49	2.8	ChipSite		
20H8A		28	PLCC	33,49	3.0	PinSite	0201	
20L2		28	PLCC	33,49	2.8	ChipSite		
20L2		28	PLCC	33,49	3.0	PinSite	0201	
20L2A		28	PLCC	33,49	2.8	ChipSite		
20L2A		28	PLCC	33,49	3.0	PinSite	0201	
20L8		28	PLCC	33,49	2.8	ChipSite		
20L8		28	PLCC	33,49	3.0	PinSite	0201	
20L8A		28	PLCC	33,49	2.8	ChipSite		
20L8A		28	PLCC	33,49	3.0	PinSite	0201	
20P2		28	PLCC	33,49	2.8	ChipSite		
20P2		28	PLCC	33,49	3.0	PinSite	0201	
20P2A		28	PLCC	33,49	2.8	ChipSite		
20P2A		28	PLCC	33,49	3.0	PinSite	0201	
20P8		28	PLCC	33,49	2.8	ChipSite		
20P8		28	PLCC	33,49	3.0	PinSite	0201	
20P8A		28	PLCC	33,49	2.8	ChipSite		
20P8A		28	PLCC	33,49	3.0	PinSite	0201	
20R4		28	PLCC	33,49	2.8	ChipSite		
20R4		28	PLCC	33,49	3.0	PinSite	0201	
20R4A		28	PLCC	33,49	2.8	ChipSite		
20R4A		28	PLCC	33,49	3.0	PinSite	0201	
20R6		28	PLCC	33,49	2.8	ChipSite		
20R6		28	PLCC	33,49	3.0	PinSite	0201	

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
SGS-Thomson Microelectronics 20V8 PLCC as: (continued)								
20R6A		28	PLCC	33,49	2.8	ChipSite		
20R6A		28	PLCC	33,49	3.0	PinSite	0201	
20R8		28	PLCC	33,49	2.8	ChipSite		
20R8		28	PLCC	33,49	3.0	PinSite	0201	
20R8A		28	PLCC	33,49	2.8	ChipSite		
20R8A		28	PLCC	33,49	3.0	PinSite	0201	
20RP4		28	PLCC	33,49	2.8	ChipSite		
20RP4		28	PLCC	33,49	3.0	PinSite	0201	
20RP4A		28	PLCC	33,49	2.8	ChipSite		
20RP4A		28	PLCC	33,49	3.0	PinSite	0201	
20RP6		28	PLCC	33,49	2.8	ChipSite		
20RP6		28	PLCC	33,49	3.0	PinSite	0201	
20RP6A		28	PLCC	33,49	2.8	ChipSite		
20RP6A		28	PLCC	33,49	3.0	PinSite	0201	
20RP8		28	PLCC	33,49	2.8	ChipSite		
20RP8		28	PLCC	33,49	3.0	PinSite	0201	
20RP8A		28	PLCC	33,49	2.8	ChipSite		
20RP8A		28	PLCC	33,49	3.0	PinSite	0201	
VLSI Technology, Inc. 16V8 DIP as:								
10H8		20	PLCC	33,49	2.2	ChipSite		
10H8		20	PLCC	33,49	3.0	PinSite	0201	
10L8		20	PLCC	33,49	2.2	ChipSite		
10L8		20	PLCC	33,49	3.0	PinSite	0201	
10P8		20	PLCC	33,49	2.2	ChipSite		
10P8		20	PLCC	33,49	3.0	PinSite	0201	
12H6		20	PLCC	33,49	2.2	ChipSite		
12H6		20	PLCC	33,49	3.0	PinSite	0201	
12L6		20	PLCC	33,49	2.2	ChipSite		
12L6		20	PLCC	33,49	3.0	PinSite	0201	
12P6		20	PLCC	33,49	2.2	ChipSite		
12P6		20	PLCC	33,49	3.0	PinSite	0201	
14H4		20	PLCC	33,49	2.2	ChipSite		
14H4		20	PLCC	33,49	3.0	PinSite	0201	
14L4		20	PLCC	33,49	2.2	ChipSite		
14L4		20	PLCC	33,49	3.0	PinSite	0201	
14P4		20	PLCC	33,49	2.2	ChipSite		
14P4		20	PLCC	33,49	3.0	PinSite	0201	
16H2		20	PLCC	33,49	2.2	ChipSite		
16H2		20	PLCC	33,49	3.0	PinSite	0201	
16H8		20	PLCC	33,49	2.2	ChipSite		
16H8		20	PLCC	33,49	3.0	PinSite	0201	
16L2		20	PLCC	33,49	2.2	ChipSite		
16L2		20	PLCC	33,49	3.0	PinSite	0201	
16L8		20	PLCC	33,49	2.2	ChipSite		
16L8		20	PLCC	33,49	3.0	PinSite	0201	
16P2		20	PLCC	33,49	2.2	ChipSite		
16P2		20	PLCC	33,49	3.0	PinSite	0201	
16P8		20	PLCC	33,49	2.2	ChipSite		
16P8		20	PLCC	33,49	3.0	PinSite	0201	
16R4		20	PLCC	33,49	2.2	ChipSite		
16R4		20	PLCC	33,49	3.0	PinSite	0201	
16R6		20	PLCC	33,49	2.2	ChipSite		
16R6		20	PLCC	33,49	3.0	PinSite	0201	
16R8		20	PLCC	33,49	2.2	ChipSite		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
VLSI Technology, Inc. 16V8 DIP as: (continued)								
16R8		20	PLCC	33,49	3.0	PinSite	0201	
16RP4		20	PLCC	33,49	2.2	ChipSite		
16RP4		20	PLCC	33,49	3.0	PinSite	0201	
16RP6		20	PLCC	33,49	2.2	ChipSite		
16RP6		20	PLCC	33,49	3.0	PinSite	0201	
16RP8		20	PLCC	33,49	2.2	ChipSite		
16RP8		20	PLCC	33,49	3.0	PinSite	0201	
VLSI Technology, Inc. 16V8 PLCC as:								
10H8		20	DIP	33,49	2.2	Site 48/40		
10L8		20	DIP	33,49	2.2	Site 48/40		
10P8		20	DIP	33,49	2.2	Site 48/40		
12H6		20	DIP	33,49	2.2	Site 48/40		
12L6		20	DIP	33,49	2.2	Site 48/40		
12P6		20	DIP	33,49	2.2	Site 48/40		
14H4		20	DIP	33,49	2.2	Site 48/40		
14L4		20	DIP	33,49	2.2	Site 48/40		
14P4		20	DIP	33,49	2.2	Site 48/40		
16H2		20	DIP	33,49	2.2	Site 48/40		
16H8		20	DIP	33,49	2.2	Site 48/40		
16L2		20	DIP	33,49	2.2	Site 48/40		
16L8		20	DIP	33,49	2.2	Site 48/40		
16P2		20	DIP	33,49	2.2	Site 48/40		
16P8		20	DIP	33,49	2.2	Site 48/40		
16R4		20	DIP	33,49	2.2	Site 48/40		
16R6		20	DIP	33,49	2.2	Site 48/40		
16R8		20	DIP	33,49	2.2	Site 48/40		
16RP4		20	DIP	33,49	2.2	Site 48/40		
16RP6		20	DIP	33,49	2.2	Site 48/40		
16RP8		20	DIP	33,49	2.2	Site 48/40		
VLSI Technology, Inc. 20V8 DIP as:								
14H8		24	DIP	33,49	2.2	Site 48/40		
14L8		24	DIP	33,49	2.2	Site 48/40		
14P8		24	DIP	33,49	2.2	Site 48/40		
16H6		24	DIP	33,49	2.2	Site 48/40		
16L6		24	DIP	33,49	2.2	Site 48/40		
16P6		24	DIP	33,49	2.2	Site 48/40		
18H4		24	DIP	33,49	2.2	Site 48/40		
18L4		24	DIP	33,49	2.2	Site 48/40		
18P4		24	DIP	33,49	2.2	Site 48/40		
20H2		24	DIP	33,49	2.2	Site 48/40		
20H8		24	DIP	33,49	2.2	Site 48/40		
20L2		24	DIP	33,49	2.2	Site 48/40		
20L8		24	DIP	33,49	2.2	Site 48/40		
20P2		24	DIP	33,49	2.2	Site 48/40		
20P8		24	DIP	33,49	2.2	Site 48/40		
20R4		24	DIP	33,49	2.2	Site 48/40		
20R6		24	DIP	33,49	2.2	Site 48/40		
20R8		24	DIP	33,49	2.2	Site 48/40		
20RP4		24	DIP	33,49	2.2	Site 48/40		
20RP6		24	DIP	33,49	2.2	Site 48/40		
20RP8		24	DIP	33,49	2.2	Site 48/40		

Device Part Number	Menu Name	Pin Count	Package Type	Footnote	Product Version	Module	Base	MatchBook/ PPI Adapter
VLSI Technology, Inc. 20V8 PLCC as:								
14H8		28	PLCC	33,49	2.2	ChipSite		
14H8		28	PLCC	33,49	3.0	PinSite	0201	
14L8		28	PLCC	33,49	2.2	ChipSite		
14L8		28	PLCC	33,49	3.0	PinSite	0201	
14P8		28	PLCC	33,49	2.2	ChipSite		
14P8		28	PLCC	33,49	3.0	PinSite	0201	
16H6		28	PLCC	33,49	2.2	ChipSite		
16H6		28	PLCC	33,49	3.0	PinSite	0201	
16L6		28	PLCC	33,49	2.2	ChipSite		
16L6		28	PLCC	33,49	3.0	PinSite	0201	
16P6		28	PLCC	33,49	2.2	ChipSite		
16P6		28	PLCC	33,49	3.0	PinSite	0201	
18H4		28	PLCC	33,49	2.2	ChipSite		
18H4		28	PLCC	33,49	3.0	PinSite	0201	
18L4		28	PLCC	33,49	2.2	ChipSite		
18L4		28	PLCC	33,49	3.0	PinSite	0201	
18P4		28	PLCC	33,49	2.2	ChipSite		
18P4		28	PLCC	33,49	3.0	PinSite	0201	
20H2		28	PLCC	33,49	2.2	ChipSite		
20H2		28	PLCC	33,49	3.0	PinSite	0201	
20H8		28	PLCC	33,49	2.2	ChipSite		
20H8		28	PLCC	33,49	3.0	PinSite	0201	
20L2		28	PLCC	33,49	2.2	ChipSite		
20L2		28	PLCC	33,49	3.0	PinSite	0201	
20L8		28	PLCC	33,49	2.2	ChipSite		
20L8		28	PLCC	33,49	3.0	PinSite	0201	
20P2		28	PLCC	33,49	2.2	ChipSite		
20P2		28	PLCC	33,49	3.0	PinSite	0201	
20P8		28	PLCC	33,49	2.2	ChipSite		
20P8		28	PLCC	33,49	3.0	PinSite	0201	
20R4		28	PLCC	33,49	2.2	ChipSite		
20R4		28	PLCC	33,49	3.0	PinSite	0201	
20R6		28	PLCC	33,49	2.2	ChipSite		
20R6		28	PLCC	33,49	3.0	PinSite	0201	
20R8		28	PLCC	33,49	2.2	ChipSite		
20R8		28	PLCC	33,49	3.0	PinSite	0201	
20RP4		28	PLCC	33,49	2.2	ChipSite		
20RP4		28	PLCC	33,49	3.0	PinSite	0201	
20RP6		28	PLCC	33,49	2.2	ChipSite		
20RP6		28	PLCC	33,49	3.0	PinSite	0201	
20RP8		28	PLCC	33,49	2.2	ChipSite		
20RP8		28	PLCC	33,49	3.0	PinSite	0201	

Footnotes

1. This device has initialization data which follows the Main Array data in User Memory.

2. This device is a microcontroller with security bit programming capability. Security bit programming may be enabled in the Program Memory Device Options screen.

3. This device has initialization data which follows the Main Array data in User Memory. It also has an asynchronous/synchronous output enable bit which follows the initialize word data in User Memory. Data for this bit should be set at 00 for asynchronous mode, or 01 for synchronous mode. Other data will generate a program or verify error.

4. This device has initialization data at device address 2000 hex, following the Main Array. It also has an architecture byte at device address 2001 hex. The following table shows the architecture data for the three modes of operation.

   Asynchronous operation, address 2001, value 00 hex
   Synchronous operation, address 2001, value 01 hex
   Initialize word operation, address 2001, value 02 hex

5. This device requires socket adapter PA78P322KD. It is available from the device manufacturer. Set device block size to 4000 hex.

6. This device is a microcontroller with security bit programming capability. Security bit programming may be enabled in the Program Memory Device Options screen; this overrides the Mask Option Register (MOR) security bit value in User Memory. Note that there are two menu selections for the 68705S3: mask set 1TJ6 identifies parts produced before 1987, and mask set 0A20T identifies parts produced since January 1987.

7. This device's memory map is offset to start at User Memory address 0000 hex. The EPROM memory block starts at User Memory 0000 and is translated to device address F000 hex during a program operation. A load operation will read device address F000 hex and translate address 0000 to User Memory.

8. This device's memory array begins at address 80 hex. The programmer will automatically transfer data from User Memory to the device by the required offset. If the data block begins at User Memory 0 hex, it will be translated to device address 80 hex during a program operation. Conversely a load operation will transfer the data block from device address 80 hex to User Memory address 0.

9. This device requires socket adapter PA78P322KC. It is available from the device manufacturer. Set device block size to 4000 hex.

10. The address block for this device is defined with the configuration byte at location 103F hex (low nibble only). The EEPROM is located at address B600 to B7FF hex. The two ROM blocks are at addresses BF40 to BFFF and E000 to FFFF hex.

11. This device does not support block limits; the block size is 64K. Memory locations not defined as EPROM or EEPROM are set to zero. The configuration byte, located at address 103F, specifies the starting address of the EEPROM memory and enables/disables the COP system watch dog timer.

    The upper nibble of the configuration byte defines the most significant bit of the starting address of the EEPROM memory. If the configuration byte is set to 3F hex, then the EEPROM starting address is 3800 hex (3000 hex + 800 hex). Note that the upper nibble of the configuration byte cannot be set to B hex.

    The lower nibble of the configuration byte defines the enable/disable state of the COP system watch dog timer. This nibble can only be set to F hex (disable) or B hex (enable).

12. This device requires socket adapter H31VSA01A. It is available from the device manufacturer.

13. This device requires socket adapter H67PWA01A. It is available from the device manufacturer.

14. This device requires socket adapter H31YSA01A. It is available from the device manufacturer.

15. This device requires socket adapter H35VSA01A. It is available from the device manufacturer.

16. This device requires socket adapter HS35ZESF01H. It is available from the device manufacturer.

17. This device requires socket adapter 87C452P. It is available from the device manufacturer.

18. This device is a microcontroller with Security Data and User Data features. Enable the security bit in the Program Device Options screen by using the security bit option or by programming a 1 at address 800 hex. The User Data Bytes are at address 801 and 802 hex. The Security Bit and User Data features must be enabled in the Program Device Options screen.

19. To use this device, early versions of UniSite must be modified to ensure that UniSite complies with programming specifications. Data I/O will modify UniSite model numbers 901-0058-001 through 901-0058-006 free of charge. Contact Data I/O Customer Support for further information.

20. The main array fuses for this device are 512 thru 1535. The polarity fuses are 2053 and 2054. All other fuse locations are phantom fuses. A load operation will reset the phantom locations to zero. JEDEC files that set the phantom locations in the fuse map will be calculated in the checksum, but will not affect program or verify operations.

21. The window on these devices should be covered with an opaque label during programming.

22. Cross Programming support for GAL devices are listed in the Cross Programming section of the Device List.

23. This device contains two separate EPROM areas, one for Instruction information and the other for Data. The Instruction memory space is address 0 to 7FF hex; the instruction data consists of four bytes, three information bytes followed by a null byte.

    The Data memory space is address 800 to BFF hex; data is oriented in reverse order with address BFF hex as the first byte and address 800 hex as the last address. This format is compatible with the NEC 77P20 assembler. See NEC's 77P20 databook for more information.

24. This device is a microcontroller with security bit programming capability. Security bit programming may be enabled in the Program Memory Device Options screen. This device also has address locations in the programmable array area that are reserved for special functions and are not programmable. These locations are 9-B hex, D-F hex, 18-3F hex, and the most significant byte of C hex. These locations will always load as FFFF hex or FF hex for location 00C. If data is entered at these locations, a verify error occurs, but data will not be programmed into the device.

    The least significant byte of location C hex is the Chip Configuration byte, which is programmable. The two most significant bits of this location are the lock bits which can only be programmed if the Security Bit programming is enabled from the Program Device Options screen. Consult the Manufacturer's specifications for further information. This device does not need to have the Byte Swap Option enabled (in UniSite version 2.5 or later).

25. This device is a microcontroller with two security options. Currently, only one of the two security options may be implemented per device.

    The first security option protects against in-circuit reads. This option is selected from the program screen. The second security option is activated by programming device addresses 782 hex and 783 hex with data 20 hex and FE hex respectively. This prevents the part from entering program mode.

    Addresses 782 hex and 783 hex may also be used for normal data, however, once data is programmed at these addresses, you must erase the device before attempting another program operation.

26. This device has special programmable registers that can be programmed by entering data at locations following the Main Array. The CLR register is located at device address 8000 hex. The SFR register is located at device address 8001 hex. The SFRLR register is located at device address 8002 hex. Refer to the manufacturer's spec sheet for the correct data pattern (leave all undefined bits as 1s).

    If the EPROM array and the SFR registers are programmed to overlap, the programmer will fill the overlapped section in RAM with zeros.

27. This device has a data format very similar to that described in footnote 23. The major difference is in the partitioning of the EPROM space. Instruction data memory space is at 0 to 1FFF hex. Data memory space is at 2000 to 27FF hex with the first data word at address 2000 hex.

28. This programmer does not fully support all structured test cases for this device.

    Refer to the sections in your manual which describe the "High Speed Logic Drivers" and the "Compensated Vector Test" options. These options can be used to help identify the cause and possibly eliminate a vector from failing.

29. Any of the three security options can be implemented for this device (Encryption Array data, Security Bit 1 or Security Bit 2). You can select the security options from the Program Device Options screen, or from the Main Array. Once any of the security options have been programmed into the device, no further programming is allowed.

    Illegal operations will generate one of these error messages:

    a. Encryption Array Already Programmed - A programming operation has been attempted after the Encryption Array has been programmed.

    b. Security Fuse Programmed or Bad Device - A programming operation has been attempted after security bit 1 has been programmed.

    c. Security Fuse Violation - A programming operation has been attempted after security bit 2 has been programmed. This error will also be generated for a load or verify operation.

    d. Test Fuse Programming Error - This error will be displayed if there is a programming error in the Encryption Array.

    Data in the programmer's User Memory is partitioned as follows:

    Main Array Data, 0 through 7FF hex
    Encryption Array Data, 800 through 80F hex
    Security Bit1 Data, 810 hex (bit D7)
    Security Bit2 Data, 810 hex (bit D6)

    Enter Encryption Array data by editing the appropriate address in User Memory. Enter Security Bit data via the edit screen or the PROGRAM DEVICE Options screen.

    After the Encryption Array is programmed, device data will no longer match data in User RAM. Encryption Array and Security Bit data cannot be read from the device.

30. This device is a microcontroller with security bit programming capability. Security bit programming may be enabled in the Program Memory Device Options screen.

    The device's memory map starting at address 2000 hex is offset by 2000 hex bytes to start at the User Memory address 0000 hex. Because of differences in assemblers, fill first 10000 hex bytes in User Ram with FF hex before file downloading. Partial device operation is not allowed.

This device also has address locations in the programmable array area that are reserved for special functions and are not programmable. These addresses are B, D-F, 20-3F hex, and the most significant bytes of A and C hex. These addresses will always load as FFFF hex (FF hex for addresses 00A and 00C). If data is entered at these addresses, a verify error occurs, but the data will not be programmed into the device.

The least significant byte of address A hex is the PPW byte, which is programmable. The least significant byte of address C hex is the Chip Configuration byte, which is programmable. The two most significant bits of this location are the lock bits which can only be programmed if the Security Bit programming is enabled from the Options screen. Consult the manufacturer's specifications for further information.

Starting with Unisite software version 3.7, 2900 version 1.8, and 3900 version 1.2, the most significant byte of address 000C must be filled with 20 hex.

The User Ram is showed in words as default. It may be more convenient to select Data Word Width = 8 and then follow memory map in Intel's User's Guide.

31. This device does not support Illegal Bit Test or Blank Check. However, the programmer will not indicate that the tests are not supported.

32. This device contains a User Electronic Signature (UES) array. Programming this array is optional. Two devices are available; one with the UES suffix and one without.

    The device without the UES suffix programs the device but does not program the UES array. The device with the UES suffix programs all the arrays.

    When you download a JEDEC file, you will select the device compatible with the JEDEC file. If the device is not compatible, one of the following errors will be displayed: File not initialized or Incompatible User Data.

33. This device contains extra fuses which are automatically configured by the programmer. If these extra fuses fail to program, an error occurs. However, since these fuses are not part of the fuse map, an underblow/overblow operation will not indicate their presence.

34. This device requires socket adapter PA78P322L. It is available from the device manufacturer. Set device block size to 4000 hex.

35. The memory map of this device is offset to start at User Memory address 0000 hex bytes. The location of the EPROM memory block starts at User Memory 0000 hex, and will be translated to device address 20 hex during a program operation. A load operation will read device address 20 hex and translate address 0000 to User Memory.

36. This Device has a Software Data Protection option that can be enabled or disabled on the Program Device Options screen.

    (UniSite only) This feature is only presented on the Program Device screen for single device operations. When the Data Protection option is selected in the single device screen, it also applies to the SetSite module operation for Gang programming.

37. If you attempt to re-program this device after programming the security fuse, a Device Over-Current Fault error may be generated and there is a potential that the device may be damaged.

38. This device has initialization data that follows the Main Array located at device address 800 hex. The device also has an architecture byte located at 801 hex. The following table shows the architecture data for the four modes of operation.

    Asynchronous Enable, Asynchronous Initialize 801 hex = FF hex
    Synchronous Enable, Asynchronous Initialize 801 hex = FE hex
    Asynchronous Enable, Synchronous Initialize 801 hex = FD hex
    Synchronous Enable, Synchronous Initialize 801 hex = FC hex

39. Actel's family of FPGAs are treated as memory devices for programming operations. The fuse data is represented in a binary format commonly used for memory devices. This requires a data translation program that runs on the Action Logic development system. This program will translate fuse information on the Actel programming operations and file transfers.

    Keep the following in mind when using these devices: verify passes must be set to 0 prior to programming, block limits are not supported for the Actel FPGAs, and do not change the user data size after downloading data.

    Contact Data I/O Customer Support and request the Actel Programming Application Note.

40. This device does not support Preload vectors.

41. This device requires socket adapter AS-68-40-01P-6. It is available from Emulation Technology Inc. (408-982-0660).

42. This device requires socket adapter AS-68-40-04P-6. It is available from Emulation Technology Inc. (408-982-0660).

43. Data for this device is organized into the User RAM as follows: Main Array data, four words of User I.D. (identification), information, and a configuration word.

    This device has a 12 bit data word which is represented as 16 bit data for the programmer. Data Bits 12-15 throughout the Main Array are not used. Bits 4-15 in the User I.D. and configuration words are not used. All unused bits will be loaded from the device to User RAM as zeros and are ignored during the verify operation. During programming, bits 4-11 of the User I.D. and configuration word are automatically be programmed to zeros. The Security Bit can be programmed only by setting the data to a one and enabling the one on the Programming Options screen. Oscillator selection bits cannot be reprogrammed if they were configured by the factory (OTP devices only).

When assembling your source file, use the output option that produces the merged 8 bit Intellec Hex object file (INHX8M). The object file that was created can then be downloaded to the programmer by selecting the Intel Intellec 8/MDS translator (code 83).

44. This device is thinner than most JEDEC type PLCC devices, therefore an LCC Spacer may be required to make proper contact. A device insertion error occurs when the device makes poor contact. A spacer is not necessary when using a PinSite, 2900, or 3900 MatchBook for LCC devices. Contact Data I/O Customer Support for information regarding the LCC Spacer Kit.

    This applies only to the ChipSite module.

45. This device has a differential cell array utilizing floating gate technology. Any unprogrammed location is in an undetermined state. Loading an unprogrammed device will produce inconsistent checksums. Verify operations are valid only after the device has been programmed. Some differential cell devices support a special blank check routine. If blank check is supported, attempts to reprogram a non-blank device will generate an illegal bit error. Although setting block limits is allowed, it is recommended that the entire device be programmed to avoid ambiguous states.

46. Partial device operations are not allowed on this device. If your data file is smaller than the device size, make sure that the extra locations in User RAM are filled with the blank state (FF hex).

47. The data file used to program this device contains the security option data. The Security option will not be programmed into the device unless it is enabled from the Programming Options screen.

48. This device has an asynchronous/synchronous output enable bit that follows the Main Array data in User Memory. The outputs are enabled synchronously when programmed to 1.

49. This device contains an Electronic ID. If an ID error occurs, the wrong device is selected or the version of this device is not supported. A software update may be required. Contact Data I/O Customer Support for more information.

50. This device does not support the test code/checksum and test signature features.

51. Any of the four security options can be implemented for this device (Encryption Array data, Security Bits 1, 2 or 3). The security options can be selected from the Program Device Options screen, or from the Main Array. Once any of the security options have been programmed into the device, no further programming is allowed.

    Data in the Programmer's User Memory is partitioned as follows:

    Main Array Data, 0 through 7FFF hex
    Encryption Array Data, 8000 through 803F hex
    Security Bit1 Data, 8040 hex (bit D7)
    Security Bit2 Data, 8040 hex (bit D6)
    Security Bit3 Data, 8040 hex (bit D5)

Enter Encryption Array data by editing the appropriate address in User Memory. Enter Security Bit data via the edit screen or the Program Device Options screen.

After the Encryption Array is programmed, device data will no longer match data in User RAM. Encryption Array and Security Bit data cannot be read from the device.

52. This device is a microcontroller with Security Bit programming capability. Security Bit programming may be enabled in the Program Memory Device Options screen. (No Uprom bit programming in UniSite 3.0 or 2900 1.2.)

    The device's memory map starting at address 2000 hex is offset by 2000 hex bytes to start at the User Memory address 0000 hex. Because of differences in assemblers, fill first 10000 hex bytes in User Ram with FF hex before file downloading. Partial device operation is not allowed.

    This device also has address locations in the programmable array area that are reserved for special functions and are not programmable. These addresses are B, D-F and 2F-3F hex. These locations will always load as FFFF hex. If data is entered in User RAM at these locations, a verify error occurs, but no data will be programmed at those locations.

    Address C hex is also reserved. The most significant byte of C hex is always programmed to 20 hex. If data other than 20 hex is entered in User RAM at this location, a verify error occurs, but data 20 hex will be programmed.

    The least significant byte of address C hex is the Chip Configuration byte, which is programmable. The two most significant bits of this location are the lock bits, which can be programmed only by selecting the Security Bit programming option in the PROGRAM Options screen. Consult the Manufacturer's specifications for further information.

    The User Ram is showed in words as default. It may be more convenient to select Data Word Width = 8 and then follow memory map in Intel's User's Guide.

53. This device contains a security fuse, however, the option is currently not supported. If you attempt to program the security fuse manually, the part will secure. However, reprogramming will no longer be possible.

54. This device does not support upload, output to disk, fill RAM, Edit data or Blank check. Disable the "Blank Check" option, located on the Programming Options screen, to avoid invalid non-blank and illegal-bit errors.

55. This device does not support output to disk, Fill RAM, Edit data or Blank check. Disable the "Blank Check" option, located on the Programming Options screen, to avoid invalid non-blank and illegal-bit errors.

    This programmer supports POF files generated by the MAXPLUS (TM Altera) development system software version 2.5 or later.

    Some POF files contain "don't care" data that is calculated into the data checksum. If you perform a Load operation after programming a downloaded file, the checksum may be slightly different.

56. This device has an architecture byte at address 8000 hex. Set the appropriate bits to 1 to program the desired features into the device. Set all unused bits in the architecture byte to 0.

Address	Bit	Function	Device(s) Supporting Feature
8000 (hex)	2	ALE polarity	Cypress 7C277 and 7C279
8000	1	ALE enable	Cypress 7C277 and 7C279
8000	0	SYNC enable	Cypress 7C277

57. The WSI-PSD301/302/303 Maple compiled data file may contain data at locations that are not programmable. These locations will be filled with zeros during any device related operation (program, load, verify). This may result in an incorrect checksum if you program a device immediately after downloading the PSD301/302/303 data file to the programmer.

    To get the correct checksum, perform a load operation after programming the device. Any devices programmed after the first device will display the correct checksum.

    The PSD301/302/303 contains a Security Bit (SECA) which can be enabled in the Program Memory Device Options screen.

58. This device requires one of the following socket adapters:

Adapter	Manufacturer
AS-44-28-02P-6YAM	Emulation Technology (408-982-0660)
44PL/28D6-ZL-L1016	EDI Corporation (209-892-3270)
44PL/28D6-ZAL-L1016	EDI Corporation (209-892-3270)

59. This device requires socket adapter HS538ESH01H. It is available from the device manufacturer.

60. This device requires socket adapter HS538ESG01H. It is available from the device manufacturer.

61. This device requires socket adapter HS338ESH01H. It is available from the device manufacturer. Set device block size to 4000 hex.

62. This device requires socket adapter HS18XESF01H. It is available from the device manufacturer. Set device block size to 4000 hex.

63. This device requires socket adapter HS460ESF01H. It is available from the device manufacturer. Set device block size to 4000 hex. Data bits 5-7 should be set to ones at all address locations. Refer to the manufacturer's spec sheet for the correct data pattern.

64. This device requires socket adapter HS470ESS11H. It is available from the device manufacturer. Data bits 5-7 should be set to ones at all address locations. Refer to the manufacturer's spec sheet for the correct data pattern.

65. This device requires socket adapter PCA4708. It is available from the device manufacturer. Set device begin address and device block size to 4000 hex.

66. This device requires socket adapter PCA4708. It is available from the device manufacturer.

67. This device requires socket adapter PCA4700G02. It is available from the device manufacturer. Place jumper JP1 on adapter to 64. Set device begin address to 800 hex and device block size to 1800 hex.

68. This device requires socket adapter PCA4701G02. It is available from the device manufacturer. Place jumper JP1 on adapter to 64. Set device begin address to 800 hex and device block size to 1800 hex.

69. This device requires socket adapter PCA4700G02. It is available from the device manufacturer. Place jumper JP1 on adapter to 64. Set device block size to 4000 hex.

70. This device requires socket adapter PCA4701G02. It is available from the device manufacturer. Place jumper JP1 on adapter to 64. Set device block size to 4000 hex.

71. This device requires socket adapter PCA4705. It is available from the device manufacturer. Set device begin address to 1000 hex and device block size 3000 hex.

72. This device requires socket adapter PCA4730. It is available from the device manufacturer. Set device begin address and device block size to 4000 hex.

73. This device requires socket adapter PCA4731. It is available from the device manufacturer. Set device begin address and device block size to 4000 hex.

74. This device requires socket adapter PCA4719. It is available from the device manufacturer. Set device begin address and device block size to 4000 hex.

75. This device requires socket adapter PCA4710. It is available from the device manufacturer. Set device begin address and device block size to 4000 hex.

76. This device requires socket adapter PCA4791. It is available from the device manufacturer.

77. This device requires socket adapter PCA4740. It is available from the device manufacturer. Set device block size to 1000 hex.

78. This device requires socket adapter PCA4741. It is available from the device manufacturer.

79. This device requires socket adapter HS338ESG01H. It is available from the device manufacturer. Set device block size to 4000 hex.

80. This device requires socket adapter HS328ESS01H. It is available from the device manufacturer.

81. This device requires socket adapter HS81XESG01H. It is available from the device manufacturer. Set device block size to 4000 hex.

82. This device requires socket adapter HS528ESS01H. It is available from the device manufacturer. Set device block size to 4000 hex.

83. This device requires socket adapter HS409ESS11H. It is available from the device manufacturer. Data bits 5-7 should be set to ones at all address locations. Refer to the manufacturer's spec sheet for the correct data pattern.

84. This device requires socket adapter PA-78CP14CW. It is available from the device manufacturer. Set device block size to 4000 hex.

85. This device requires socket adapter PA-78P214CW. It is available from the device manufacturer. Set device block size to 4000 hex.

86. This device has phantom fuses in the JEDEC fuse map which are ignored during program and verify operations. These fuses will load as ones. This device must be erased before re-programming. An error will occur if the device is not erased before re-programming.

87. This device requires socket adapter AD-3. It is available from the device manufacturer.

88. This device requires socket adapter AD-4. It is available from the device manufacturer.

89. This device requires socket adapter AD-10. It is available from the device manufacturer.

90. This device requires socket adapter AD-12. It is available from the device manufacturer.

91. This device requires socket adapter 98A-EAC-68. It is available from the device manufacturer.

92. This device requires socket adapter MFT2A02-001. It is available from the device manufacturer.

    There are switches on the socket adapter which allow the individual devices on the card to be programmed. The programmer's block size will default to the size of an individual device. Refer to the documentation supplied with the socket adapter for information on how to configure the switches on the adapter.

93. This device requires socket adapter MFT2A02-002. It is available from the device manufacturer.

94. This device does not support Illegal Bit Test. However, the programmer will not indicate that the test is not supported.

95. This device has one or more architecture bits contained in one byte at address 10000 hex. Set the appropriate bits to 1 to program the desired features into the device:

Address	Bit	Function	Device Supporting Feature
8000 (hex)	7 msb	CS2 polarity	Cypress 7C289
8000	6	CS1 polarity	Cypress 7C289
8000	5	WAIT polarity	Cypress 7C289
8000	4	WAIT timing	Cypress 7C289
8000	3	ALE polarity	Cypress 7C289
8000	2	ALE enable	Cypress 7C289
8000	1	Address setup	Cypress 7C289
8000	0 lsb	SYNC enable	Cypress 7C289

96. This device requires a socket adapter that interchanges pins 1 and 4 between the device and ZIF socket.

97. This device requires one of the following socket adapters:

Adapter	Manufacturer
AS-68-28-03P-6YAM	Emulation Technology (408-982-0660)
68PL/28D6-ZL-L1024	EDI Corporation (209-892-3270)
68PL/28D6-ZAL-L1024	EDI Corporation (209-892-3270)

98. This device requires a socket adapter and additional operating instructions. Please contact Data I/O Customer Support for further information.

99. This device has programmable reset polarity. To set polarity active low, set addresses 2000-2003 hex to zero's. For active high polarity, set to ff hex.

100. This device requires socket adapter PA-CP14GF. It is available from the device manufacturer. Set device size to 4000 hex.

101. This device requires one of the following socket adapters:

Adapter	Manufacturer
AS-120-28-01Q-6YAM	Emulation Technology (408-982-0660)
120QF/28D6-ZL-L1048	EDI Corporation (209-892-3270)
120QF/28D6-ZAL-L1048	EDI Corporation (209-892-3270)

102. This device requires socket adapter AD14. It is available from the device manufacturer.

103. This device requires socket adapter HS470ESS11H. It is available from the device manufacturer. Data bits 5-7 should be set to ones at all address locations. Refer to the manufacturer's spec sheet for the correct data pattern.

104. This device requires socket adapter HS460ESH01H. It is available from the device manufacturer. Set device size to 4000 hex. Data bits 5-7 should be set to ones at all address locations. Refer to the manufacturer's spec sheet for the correct data pattern.

105. This device requires socket adapter HS328ESS01H. It is available from the device manufacturer.

106. This device requires socket adapter HS528ESS01H. It is available from the device manufacturer. Set device size to 4000 hex.

107. Any of the four security options can be implemented for this device (Encryption Array data, Security Bits 1, 2 or 3). The security options can be selected from the Program Device Options screen, or from the Main Array. Once any of the security options have been programmed into the device, no further programming is allowed.

    Data in the programmer's User Memory is partitioned as follows:

Main Array Data	0 through 1FFF hex
Encryption Array Data	2000 through 203F hex
Security Bit1 Data	2040 hex (bit D7)
Security Bit2 Data	2040 hex (bit D6)
Security Bit3 Data	2040 hex (bit D5)

    Enter Encryption Array data by editing the appropriate address in User Memory. Enter Security Bit Data via the Edit Screen or the Program Device Options screen.

    After the Encryption Array is programmed, device data will no longer match data in User RAM. Encryption Array and Security Bit data cannot be read from the device.

108. Block limits are not supported for this device. The entire memory array will be programmed or erased automatically.

109. At address locations 0 to FFF hex, data bits 4-7 should be set to ones. At address locations 1000 to 1FFF hex, data bits 5-7 should be set to ones. Refer to the manufacturer's spec sheet for the correct data pattern.

110. This device requires socket adapter PCA4710. It is available from the device manufacturer.

111. This device requires socket adapter PCA4711. It is available from the device manufacturer.

112. This device requires socket adapter PCA4709. It is available from the device manufacturer.

Device	**JP1 Jumper Position**
37701E2SDIP	all to 01
37703E2SDIP	all to 01
37705E2SDIP	all to 05

    Set device begin address and block size to 4000 hex.

113. This device requires socket adapter PCA4709. It is available from the device manufacturer.

114. This device requires socket adapter MFT2A02-001. It is available from the device manufacturer. To program the first 128K, select bank 0. Maximum device size is 20000 hex. To program the last 64K, select bank 1. The maximum device size is 10000 hex.

115. This device requires socket adapter PA-78P214GC. It is available from the device manufacturer. Set device block size to 4000 hex.

116. (2900 only) To insert the socket adapter, push down on the ZIF socket handle.

117. This device requires socket adapter MB98A-0AC-68. It is available from the device manufacturer.

118. This device uses 3.0 volts on VCC for load, program, and verify operations. The VCC voltages applied during a two-pass verify operation are 3.0 volts and 3.5 volts.

119. Structured testing is not supported for this device on the ChipSite module.

120. This device's memory map starting at address 2000 hex is offset by 2000 hex bytes to start at the User Memory address 0000 hex. Because of differences in assemblers, fill first 10000 hex bytes in User Ram with FF hex before file downloading. Partial device operation is not allowed.

    The device has address locations in the programmable array area that are reserved for special functions and are not programmable. These addresses are A, B, 2F-3F hex, and the least significant bytes of E hex and F hex. Fill these locations in User RAM with FF hex.

    Fill the most significant bytes of C, D, E and F hex in User RAM with 20 hex.

    The least significant byte of C hex (CCB byte) is programmable. The two most significant bits of this location are programmable lock bits, which can be programmed only by selecting the Security Bit programming option in the Program Options screen.

    To program the CCB1 and Security Key bytes (the least significant byte of D hex and all bytes of address 10-17 hex) consult the manufacturer's specifications.

    The User Ram is showed in words as default. It may be more convenient to select Data Word Width = 8 and then follow memory map in Intel's User's Guide.

121. **Caution: use only for FX-core devices.** FX core devices can be distinguish from older 87C51/87C51FA/87C51FB devices via the topside tracking number (FPO number) marked on the part. The topside tracking number on FX core devices will end with a letter 'A'. For more information call Intel.

Any of the four security options can be implemented for this device (Encryption Array data, Security Bits 1, 2 or 3). The security options can be selected from the Program Device Options screen. Data in the Programmer's User Memory is partitioned as follows:

Device	87C51(FX)	87C51FA(FX)	87C51FB(FX)
Main Array	0 - 0FFFh	0 - 1FFFh	0 - 3FFFh
Encrypt. Array	1000 - 103F	2000 - 203Fh	4000 - 403Fh
Security Bit 1	1040 (bit 7)	2040 (bit 7)	4040 (bit 7)
Security Bit 2	1040 (bit 6)	2040 (bit 6)	4040 (bit 6)
Security Bit 3	1040 (bit 5)	2040 (bit 5)	4040 (bit 5)

Enter Encryption Array data by editing the appropriate address in User Memory. Enter Security Bit data via the edit screen or the Program Device Options screen.

After the Encryption Array is programmed, device data will no longer match data in User RAM. Encryption Array and Security Bit data cannot be read from the device.

122. This device requires an adapter that converts the TSOP pinout to a standard DIP socket, for use with Site40 or Site48. The adapter is available from the following vendors:
    - Emulation Technology, (408) 982-0660 or
    - California Integration Coordinators, (916) 626-6168
123. This device requires socket adapter PA78P328GF. It is available from the device manufacturer. Set device block size to 4000 hex.
124. This device requires socket adapter PA78P328CW. It is available from the device manufacturer. Set device block size to 4000 hex.
125. This device must have the Device Begin Address set to zero, for partial programming to function properly
126. This device must have the Device Begin Address set to zero, and the Device Block Size is set to an even number, for partial programming to function properly
127. This device requires the Fujitsu MB98A-EAC-68 card adapter. The least significant address line on the card is controlled by a dip switch on the adapter. Please use the following procedure to program adjacent bytes as the least significant and most significant byte of a word:
    1. Set data word width to 16.
    2. Set auto increment to Y.
    3. Program even bytes. When the operation is complete, the next device field in the programming menu will change from 1 to 2.
    4. Toggle dip switch 1 and program odd bytes.
128. This device requires socket adapter AS-84-40-01P-6YAM. It is available from Emulation Technology Inc. (408-982-0660).

129. Some devices may generate intermittent programming errors (low yields). If this occurs, repeat the program operation. Data I/O is currently working with the semiconductor manufacturer to improve yields.

130. This device has a non-contiguous memory map. To insure the integrity of the programmer's checksum, the unused and/or unprogrammable memory locations in user RAM must be set to zero.

    Consult the Manufacturer's specifications for further information.

131. This device has a non-contiguous memory map. To insure the integrity of the programmer's checksum, the unused memory locations in user RAM must be set to zero prior to loading a device or downloading data. Use the Fill Ram option under the More-Edit screen.

    Consult the Manufacturer's specifications for further information.

132. The illegal-bit and blank check operations are only executed on the EPROM array.

133. The device memory space is partitioned as follows:

Array	Type	Address	
Instruction	Programmable	0 - 1FFFh	
Reserved	Unprogrammable	2000 - 4FFFh	fill with 0xFF
Data	Programmable	4800 - 4FFFh	

    Instruction and data arrays have unused bit locations which must be set to ones. This should be done by your development tools. Refer to the device specification sheet for more information.

134. The device memory space is partitioned as follows :

Array	Type	Address	
Instruction	Programmable	0 - 3FFFh	
Reserved	Unprogrammable	4000 - 4FFFh	fill with 0xFF
Data	Programmable	4800 - 4FFFh	

135. This device requires socket adapter HS823ESC01H. It is available from the device manufacturer. Set device block size to 5000 hex.

    This device contains two separate EPROM areas, an instruction array address 0-1FFF hex and a data array address 4800-4FFF hex. The instruction array has unused bit locations which must be set to ones (FFC00000 hex, msb-lsb). The data array has unused bit locations which must be set to ones (FFF00000 hex). Addresses 2000-47FF hex are unprogrammable fill these locations in User RAM with FFFFFFFF hex.

    Refer to device specification sheet for more information.

136. This device requires one of the following socket adapters:

Adapter	Manufacturer
AS-84-28-02P-6YAM	Emulation Technology (408-982-0660)
84PL/28D6-ZL-L1032	EDI Corporation (209-892-3270)
84PL/28D6-ZAL-L1032	EDI Corporation (209-892-3270)

137. Set device block size to 4000 hex.

138. In-module programming with this device requires the use of an in-module adapter with part number 615-1548-002 or greater.

139. The selected device has 2 algorithms available. The part number WITHOUT the asterisk '*' should be used for devices with the mask 0D33N or later. The part number WITH the asterisk '*' should be used on devices with the mask 0D54E.

    The devices with mask 0D54E has an error in the bootloader which will not allow the device to perform the following functions properly: load, illegal-bit check and blank check. If the default 2 pass verify is not used as the number of verify passes. Please insure that the number of verify passes is set to a minimum of 1.

140. The programmer's user RAM corresponds directly to the memory map of the device.

141. This device contains an Electronic ID. If an ID error occurs, the wrong device is selected or different version of this device is selected. Two different algorithms are available, 1810T and 1810T-NEW. If both algorithms yield "Device ID error" contact Data I/O Customer Service.

142. This device is a microcontroller with Security Data and User Data features. Enable the security bit in the Program Device Options screen by using the security bit option or by programming a 1 at address 1000 hex. The User Data Bytes are at address 1001 and 1002 hex. The Security Bit and User Data features must be enabled in the Program Device Options screen.

143. If the default 2 pass verify is not used as the number of verify passes. Please insure that the number of verify passes is set to a minimum of 1.

144. Data in the Programmer's User Memory is partitioned as follows:

    Main array, 0 - 3FFF hex
    Unused bytes, 4000h - 400C, 400E hex
    ECON6, 400D hex, (ROM0, RAM0 bits)
    ECON7, 400F hex (security bits)

    The ECON6 or ECON7 have misverified, if a 'Device verification error' occures during Verify, Blank check or Illegal bit check. To determine which fuse has failed, load the device and view locations ECON6 and ECON7 User memory locations.

145. Data in the Programmer's User Memory is partitioned as follows:

     Main Array, 0 - 0FFF hex
     ECON, 1000 hex

146. This device requires an adapter that converts the PLCC pinout to a standard DIP socket. The adapter is available from device manufacture.

     Structured testing is not supported for this device with the adapter.

147. The programmer does not support the "Software Data Protection" feature during programming if the data word width is set to 16-bit or greater.

     To use the "Software Data Protect" feature for word widths greater than or equal to 16-bits, use the following procedure:

     - Program the device/s with 16-bit(or larger) data word width and "Software Data Protection" disabled.
     - Change data word width back to 8-bit.
     - Load the programmed device.
     - Re-program the device with "Software Data Protection" enabled.

148. For test vectors to run successfully on this device, the JEDEC pin swap function "P" needs to be used. The JEDEC file should be modified by inserting 4 lines after the last fuse number and before the first vector:

     Example:

```
L163073 1*
L163082 1*
L163091 1*       <-- last fuse number in JEDEC file
P 15 5 14 4 13 3 12 2 1 11 10 22 21 26 25 30 29 34
33 38 37 42 41 46 45 49 50 60 51 61 52 62 53 63 54
64 55 65 56 66 57 67 68 58 59 47 48 43 44 39 40 35
36 31 32 27 28 23 24 20 19 9 18 8 17 7 16 6*
V0001 01NHXXHHX0HH0XHNHHXNHH11HH10HH11NX1XNX11XX0XXXXX
XNXXXNXXXXXXXXXXXXNX*    <-- first vector in JEDEC file
```

149. This device has an electronically erasable array. When re-programming this device, enable the "Erase EE device" option on the program screen by typing Y or space. Failing to set this option could result in an illegal bit error.

150. Data in the programmer's User Memory is partitioned as follows:

     EEPROM Array Data, 0D80 through 0FFF hex
     EPROM Array Data, 2000 through 7FFF hex

151. The Intel 85C22V10 algorithm is a 22V10 compatible device with superset features. To determine the correct algorithm to use, view the JEDEC file you wish to program and match the QF field to the following menu entries:

    QF=5848 — select the 85C22V10 algorithm under the Intel main menu.

    QF=5828 — select the 22V10 or the IPLD22V10 algorithm under the Intel main menu, or

    QF=5828 — select the 85C22V10 as a 22V10 algorithm under the Intel XPGM menu.

    QF=5838 — select the 85C22V10 as a 22VP10 algorithm under the Intel XPGM menu.

    QF=5892 — select the 85C22V10 as a 22V10UES algorithm under the Intel XPGM menu. The 85C22V10 does not support the UES bits, so these bits will be ignored in the jedec.

152. The load operation is not supported on this device.

153. Currently, only EPROM protect option is supported. All bytes on secured device are read as FF hex. Secured device passes blank check, but fails during programming.

154. This device requires socket adapter YANO2020A. It is available from the device manufacturer.

155. This device requires socket adapter YANO2020A. It is available from the device manufacturer. Cut the pin 1,2,31 and 32 of the socket adapter.

156. This device requires socket adapter MFT2A06-005. It is available from the device manufacturer.

157. This device requires socket adapter PA78P324KC. It is available from the device manufacturer. Set device block size to 8000 hex, if not use ECC function. Set device block size to A005 hex, if use ECC function. The ECC area has unused bits and it should be set to ones. Refer to device spec sheet for more information.

158. This device requires socket adapter PA78P324GJ. It is available from the device manufacturer. Set device block size to 8000 hex, if not use ECC function. Set device block size to A005 hex, if use ECC function. The ECC area has unused bits and it should be set to ones. Refer to device spec sheet for more information.

159. This device requires socket adapter PA78P324LP. It is available from the device manufacturer. Set device block size to 8000 hex, if not use ECC function. Set device block size to A005 hex, if use ECC function. The ECC area has unused bits and it should be set to ones. Refer to device spec sheet for more information.

160. This device requires socket adapter PA78P324KD. It is available from the device manufacturer. Set device block size to 8000 hex, if not use ECC function. Set device block size to A005 hex, if use ECC function. The ECC area has unused bits and it should be set to ones. Refer to device spec sheet for more information.

161. This device requires socket adapter PA78P334KE. It is available from the device manufacturer. Set device block size to 8000 hex, if not use ECC function. Set device block size to A005 hex, if use ECC function. The ECC area has unused bits and it should be set to ones. Refer to device spec sheet for more information.

162. This device requires socket adapter PA78P334GJ. It is available from the device manufacturer. Set device block size to 8000 hex, if not use ECC function. Set device block size to A005 hex, if use ECC function. The ECC area has unused bits and it should be set to ones. Refer to device spec sheet for more information.

163. This device requires socket adapter PA78P334LQ. It is available from the device manufacturer. Set device block size to 8000 hex, if not use ECC function. Set device block size to A005 hex, if use ECC function. The ECC area has unused bits and it should be set to ones. Refer to device spec sheet for more information.

164. This device requires socket adapter PA78P312CW. It is available from the device manufacturer. Set device block size to 2000 hex.

165. This device requires socket adapter PA78P312GF. It is available from the device manufacturer. Set device block size to 2000 hex.

166. This device requires socket adapter PA78P312GQ. It is available from the device manufacturer. Set device block size to 2000 hex.

167. This device requires socket adapter PA78P312L. It is available from the device manufacturer. Set device block size to 2000 hex.

168. This device requires socket adapter PA78P322GF. It is available from the device manufacturer. Set device block size to 4000 hex.

169. This device requires socket adapter PA78P322GJ. It is available from the device manufacturer. Set device block size to 4000 hex.

170. Data in the programmer's User Memory is partitioned as follows:

Not Implemented	0 through 07FF hex
Reserved	0800 through 087F hex
Programmable	0880 through 0F9F hex
Reserved	0FA0 through 0FEF hex
Programmable	0FF0 through 0FF7 hex
Reserved	0FF8 through 0FFB hex
Programmable	0FFC through 0FFF hex

171. Data in the programmer's User Memory is partitioned as follows:

Configuration byte	003F hex
Unused	0000 through 0D7F hex
EEPROM array data	0D80 through 0FFF hex

172. Data in User Memory is partitioned as follows:

Configuration byte	103F hex
EEPROM array data	FE00 through FFFF hex

173. This device has an electronically erasable array. When reprogramming this device, enable the Erase EE Device option on the Program Device screen.

174. Configuration byte is not loaded during the Load operation, but the value of location 103F hex in User Memory is added to the final checksum.

175. Data in User Memory is partitioned as follows:

Configuration byte	003F hex
EEPROM array data	0D80 through 0FFF hex
EPROM array data	2000 through 7FFF hex

176. Data in User Memory is partitioned as follows:

User EPROM	0F00 through 1F00 hex
User Vectors	1FF0 through 1FFF hex

177. This device contains a feature which allow individual sectors to be protected. There are 8 16Kbyte sectors contained in this particular device. Once a sector is protected it's contents cannot be altered or erased.

Note: The programmer does not support sector unprotect, so the sector will effectively become a One Time Programmable array if protected.

To erase unprotected sectors enable the bulk erase feature located on the PROGRAM DEVICE options screen. Please not that bulk erase will ONLY erase unprotected sectors.

Re-programming a device with protected sectors will result in a "Non-Blank" error. This message may be ignored since it is referring to the data in the protected sectors.

Please refer to the AMD 29F010 customer bulletin for additional. information.

Use the following procedure to secure sectors:

1. Set the bytes in User Memory at locations 20000 - 20007 hex with protect or un-protect data values.

Note: Protect data can be 1 or any non-zero value. The protect bytes in user memory 20000-20007 hex are not part of the device array, but are included in the device size to allow the programmer to read and store the sector protection information.

Sector	User RAM Location	Protect Data	Unprotect Data
1	20000 hex	1	0
2	20001 hex	1	0
3	20002 hex	1	0
4	20003 hex	1	0
5	20004 hex	1	0
6	20005 hex	1	0
7	20006 hex	1	0
8	20007 hex	1	0

2. Enable the Program Security Fuse option and set Security Fuse Data to 1 on the Program Device Options screen to enable the protection programming option.
3. Program the device.

Note: Once a sector is protected its content can't be altered or erased. The only way to unprotect the secured sector(s) is to bulk erase all sectors. Be advised that bulk erasing all sectors would set all locations back to their blank state.

178. Consult the Manufacturer's specifications for further information about values of the Configuration byte.

179. This device is a microcontroller with security bit programming capability. To secure the part program bits 0 - 3 in Mask Option Register (MOR) and minor MOR to '1'.

    To use 0A20T mask set algorithm on parts with mask set 1TJ6 (produced before 1987) disable Illegal bit check and Blank check in Program Device Options screen. Then the part can be programmed. MOR and minor MOR have to be programmed to XE in the case the user wants to read data in the device.

180. Any of the four security options can be implemented for this device (Encryption Array data, Security Bits 1, 2 or 3). The security options can be selected from the PROGRAM DEVICE Options screen, or from the Main Array. Once any of the security options have been programmed into the device, no further programming is allowed.

    Data in the Programmer's User Memory is partitioned as follows:

Main Array Data	0 through 7FFF hex
Encryption Array Data	8000 through 803F hex
Security Bit1 Data	8040 hex (bit D7)
Security Bit2 Data	8040 hex (bit D6)
Security Bit3 Data	8040 hex (bit D3)

    Enter Encryption Array data by editing the appropriate address in User Memory. Enter Security Bit data via the edit screen or the PROGRAM DEVICE Options screen.

After the Encryption Array is programmed, device data will no longer match data in User RAM. Encryption Array and Security Bit data cannot be read from the device.

181. This device requires socket adapter PA71P301KA. It is available from the device manufacturer. Set device block size to 4000 hex. If using the AR register (Address register), Set the device block size to 4002 hex. Refer to device spec sheet for more information.

182. This device requires socket adapter PA71P301KB. It is available from the device manufacturer. Set device block size to 4000 hex. If using the AR register (Address register), Set the device block size to 4002 hex. Refer to device spec sheet for more information.

183. This device requires socket adapter PA71P301GQ. It is available from the device manufacturer. Set device block size to 4000 hex. If using the AR register (Address register), Set the device block size to 4002 hex. Refer to device spec sheet for more information.

184. This device requires socket adapter PA71P301GF. It is available from the device manufacturer. Set device block size to 4000 hex. If using the AR register (Address register), Set the device block size to 4002 hex. Refer to device spec sheet for more information.

185. This device requires socket adapter PA71P301L. It is available from the device manufacturer. Set device block size to 4000 hex. If use AR register (Address register), Set device block size to 4002 hex. Refer to device spec sheet for more information.

186. This device requires socket adapter PCA4774. It is available from the device manufacturer. Set device begin address and block size to 4000 hex.

187. This device requires socket adapter PCA4774. It is available from the device manufacturer.

188. When re-programming this device, disable the "Erase EE device" option on the program screen by typing N. The device is erased automatically during programming. Data in the programmer's User Memory is partitioned as follows:

Device	EEPROM	EPROM
370C610	none	7000 - 7FFF hex
370C642	none	6000 - 7FFF hex
370C710	1F00 - 1FFF hex	7000 - 7FFF hex
370C742	1F00 - 1FFF hex	6000 - 7FFF hex
370C756	1E00 - 1FFF hex	4000 - 7FFF hex

189. Data in the programmer's User Memory is partitioned as follows:

Reserved	0 through 007F hex
Programmable	0080 through 0F9F hex
Reserved	0FA0 through 0FEF hex
Programmable	0FF0 through 0FF7 hex
Reserved	0FF8 through 0FFB hex
Programmable	0FFC through 0FFF hex

190. This device requires socket adapter GPA 054 N42. It is available from the device manufacturer.

191. The Clock Detect Enable bit for this device is enabled by programming address 2016 hex of the device with the value DE hex. To program address 2016 hex for this device, edit ram with a word width of 16 and enter a DE hex in the LSB of location 0B hex.

192. Blank Check must be enabled for this device to program properly.

193. This device has address locations in the programmable array that are reserved and are not programmable. These addresses must be set. To manually set these locations, edit the programmer's User memory and fill the following locations. The following table is based on using the editor in the 16-bit data width mode which is the default for this device.

Memory Address (16-bit data)	**Fill Data**	**Addresses corresponding to device's memory map**
0E-0F hex	FFFF hex	201C-201F hex
2F-3F hex	FFFF hex	205E-207F hex
0C hex	20xx hex	2019 hex
0D hex	20xx hex	201B hex

Note: xx - don't care

If these locations do not contain the proper data, verify errors may occur after programming.

The least significant byte of C hex (2018 hex of the part) is the CCB0 byte and is programmable. The two most significant bits of this byte are lock bits, which can only be programmed by selecting the Program Security Fuse option in the PROGRAM options screen.

194. When Loading Ram from a "Master Device" a checksum conflict may occur. Texas Instruments recommends loading Ram from a JEDEC file with a known checksum.

For additional information or assistance, please contact the Texas Instruments PLD Hotline.

195. Device is marked as HW on the bottom portion of this device.

196. Device is marked as HW on the top portion of this device.

209. This device requires socket adapter CE171. It is available from the device manufacturer. Set switch position to C on the socket adapter.

210. This device has a programmable reset polarity. To set polarity active low, set addresses 8DC-8DF hex to zero's. For active high polarity, set the addresses to ff hex.

211. This device requires socket adapter PCA4774. It is available from the device manufacturer. Set device begin address and block size to 8000 hex. Set JP1 on PCA4774 to 1M (101).

212. This device requires socket adapter PCA4774. It is available from the device manufacturer. Set device begin address to 14000 hex and block size to C000 hex. Set JP1 on PCA4774 to 1M (101).

213. This device requires socket adapter PCA4708. It is available from the device manufacturer. Set device begin address to 18000 hex and block size to 8000 hex. Set JP1 on PCA4708 to 1M (101).

214. This device requires socket adapter PCA4708. It is available from the device manufacturer. Set device begin address to 14000 hex and block size to C000 hex. Set JP1 on PCA4708 to 1M (101)

215. This device requires socket adapter PCA4990. It is available from the device manufacturer.

216. The device technology does not permit a post VERIFY. However, a PROGRAM VERIFY occurs during programming. This means that although VERIFY is not a valid operation, each fuse is thoroughly tested (verified) as it is programmed.

    A LOAD operation will display the following information without writing over the data in ram:

    ALS DESIGN CHECKSUM — Actel's design file checksum (not to be confused with the Data I/O ram image checksum displayed after both file download and programming) which is generated by the design software and programmed into the silicon signature field of the device.

    SIGNATURE — User ID that is defined as part of the design and programmed into the silicon signature field of the device.

217. This algorithm requires a 44 SOIC to 40 DIP adapter. The sources and part numbers are:

    Californial Integration Technology (916)626-6168
    #CIC-44PS-40D-B6-YAM
    Emulation Technology (408)982-0660 #AS-44-40-04S-6YAM

218. The device is erased automatically before programming. Set Erase EE Device in the PROGRAM options screen to 'N'.

209. This device requires socket adapter CE171. It is available from the device manufacturer. Set switch position to C on the socket adapter.

210. This device has a programmable reset polarity. To set polarity active low, set addresses 8DC-8DF hex to zero's. For active high polarity, set the addresses to ff hex.

211. This device requires socket adapter PCA4774. It is available from the device manufacturer. Set device begin address and block size to 8000 hex. Set JP1 on PCA4774 to 1M (101).

212. This device requires socket adapter PCA4774. It is available from the device manufacturer. Set device begin address to 14000 hex and block size to C000 hex. Set JP1 on PCA4774 to 1M (101).

213. This device requires socket adapter PCA4708. It is available from the device manufacturer. Set device begin address to 18000 hex and block size to 8000 hex. Set JP1 on PCA4708 to 1M (101).

214. This device requires socket adapter PCA4708. It is available from the device manufacturer. Set device begin address to 14000 hex and block size to C000 hex. Set JP1 on PCA4708 to 1M (101)

215. This device requires socket adapter PCA4990. It is available from the device manufacturer.

216. The device technology does not permit a post VERIFY. However, a PROGRAM VERIFY occurs during programming. This means that although VERIFY is not a valid operation, each fuse is thoroughly tested (verified) as it is programmed.

    A LOAD operation will display the following information without writing over the data in ram:

    ALS DESIGN CHECKSUM — Actel's design file checksum (not to be confused with the Data I/O ram image checksum displayed after both file download and programming) which is generated by the design software and programmed into the silicon signature field of the device.

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218. The device is erased automatically before programming. Set Erase EE Device in the PROGRAM options screen to 'N'.

1 Introduction

HiTerm is a VT-100 terminal emulation program which runs on an IBM PC/XT/AT or compatible computer. HiTerm causes the PC to act like a VT-100 terminal and allows the user to communicate with, and exchange files with, other computers or machines (such as the 2900 or UniSite Programming Systems).

Features

HiTerm is easy to use and provides the following capabilities:

- Support for the programmer's "high speed download" feature (115.2Kbd), which can greatly reduce download times for large files if HiTerm is run on a 286 or 386 PC.
- Control of a programmer on any PC or compatible.
- Use of file transfer operations between the programmer and the host PC without leaving the programmer's menus.
- Support for 8-bit data transfers, which permits users to transfer binary files very quickly and efficiently using any of the binary data formats supported by a Data I/O programmer.
- Software handshaking (Xon/Xoff) for flow control.

HiTerm has two operating modes, General (G) mode and Programmer (P) mode.

- General mode causes HiTerm to perform like a VT-100 terminal. The General mode of HiTerm is useful when the user wishes to transfer files between a host computer and a PC.
- Programmer mode, in addition to its terminal emulation capability, automatically opens and closes files when transferring data files between a PC and a UniSite or 2900 programmer. This frees the user from having to direct the terminal emulator to do so at the appropriate times. Programmer mode is the recommended mode when using HiTerm in conjunction with a UniSite or 2900 programmer.

Note: All references to "programmer" refer to products such as UniSite or the 2900 Programming System. Do not use General mode to control the programmer; instead, use Programmer mode, which is designed for this purpose.

Contents of HiTerm Disk

program.bat	Batch file used to invoke HiTerm in the Programmer mode
prg9600.cfg	Configuration file (Programmer mode, 9600 baud)
prg19200.cfg	Configuration file (Programmer mode, 19200 baud)
general.bat	Batch file used to invoke HiTerm in the General mode
gen9600.cfg	Configuration file (General mode, 9600 baud)
gen19200.cfg	Configuration file (General mode, 19200 baud)
hiterm.exe	Terminal emulator program
read.me	Documentation for HiTerm
sample.dat	Practice file for transferring files between the PC and the programmer and for editing files. Note that this practice file contains intentional typing errors which can be corrected by the user with the editor on the programmer.

2 Installation

HiTerm is provided on a 360K double-sided, double density 5-1/4 inch disk in IBM format. HiTerm can be run from a floppy or hard disk.

On a Floppy Drive

1. Make a working copy of the HiTerm disk by using the DOS Copy *.* command.
2. Save the original disk as a master.
3. Proceed to the Operation section.

On a Hard Disk Drive

Follow the steps below to install HiTerm on your hard disk drive.

1. Copy all the files from the HiTerm disk to the hard disk in any subdirectory you choose.
2. Modify the *autoexec.bat* file in the root directory of the hard disk so the path points to the subdirectory where the HiTerm files reside (if it doesn't already point there). For more information regarding the path command, refer to your DOS manual.
3. Modify the *program.bat* file to reflect the location of the HiTerm files on your system. This batch file must be modified so HiTerm can find the configuration files when it is invoked. Edit the two lines which invoke HiTerm so they indicate the drive which contains the HiTerm files and also the path to the subdirectory where they reside. Refer to the following example.

Note: Bold print indicates the portion that may be modified.

Original *program.bat* File

```
echo off
Rem: HITERM will use the configuration filename from command line if present.
If not (%1) == () HITERM %1

Rem: HITERM will use PRG9600.CFG if no configuration file is specified.
If (%1) == () HITERM PRG9600.CFG
```

Modified *program.bat* File

```
echo off
Rem: HITERM will use the configuration filename from command line if present.
If not (%1) == () HITERM C:\UTIL\%1

Rem: HITERM will use PRG9600.CFG if no configuration file is specified.
If (%1) == () HITERM C:\UTIL\PRG9600.CFG
```

4. Installation is now complete. Reboot your system.

3 Operation

Running HiTerm in General Mode

From A Floppy Disk

To run HiTerm from drive A, place the HiTerm disk in drive A and change to drive A by entering **A:** ↵ . Then enter **general** ↵ .

HiTerm will be invoked using the *gen9600.cfg* configuration file. If you want to use a different configuration file, enter the configuration filename following the word "general." For instance, typing **general gen19200.cfg** ↵

will invoke HiTerm using the *gen19200* configuration file. If you want to execute HiTerm from a drive other than the one you are on, or from a subdirectory, you must set the DOS path variable to point to where HiTerm resides. You must also modify the *general.bat* file so that it points to the location of the configuration files. Refer to the instructions for installing HiTerm on a hard disk for more information.

From a Hard Disk

After installing the HiTerm files, simply enter **general** ↵ to start HiTerm in the General mode. When HiTerm is started, it will read a configuration file to set the operating mode (General or Programmer) and set the various communication port parameters (baud rate, parity, com port, etc.). In order to run HiTerm at a different baud rate, enter the appropriate configuration filename on the command line following the word "general." For example:

- Entering **general gen19200.cfg** will invoke HiTerm using the *gen19200.cfg* configuration file, which will cause HiTerm to run at 19200 baud on Com1.
- If a configuration file is not specified after the word "general," the *general.bat* batch file will use the *gen9600.cfg* file by default which will cause HiTerm to run at 9600 baud on Com1.

Running HiTerm in Programmer Mode

From a Hard Disk

After installing the HiTerm files, simply enter **program** ↵ to start HiTerm in the Programmer mode. When HiTerm is started, it will read a configuration file to set the operating mode (General or Programmer) and set the various communication port parameters (baud rate, parity, com port, etc.). In order to run HiTerm at a different baud rate, enter the appropriate configuration filename on the command line following the Program command. For example:

- Entering **program prg19200.cfg** will invoke HiTerm using the *prg19200.cfg* configuration file, which in turn will cause HiTerm to run at 19200 baud on Com1.
- If a configuration file is not specified after the word "program," the *program.bat* batch file will use the *prg9600.cfg* file by default, which will cause HiTerm to run at 9600 baud on Com1.

From a Floppy Disk

To run HiTerm from drive A, place the HiTerm disk in drive A and change to drive A by entering **A:** ↵. Next enter **program** ↵.

HiTerm will be invoked using the *prg9600.cfg* configuration file. If you want to use a different configuration file, enter the configuration filename after typing the word "program." (Entering **program prg19200.cfg** ↵ will invoke HiTerm using the *prg19200.cfg* file.)

If you want to execute HiTerm from a drive other than the one you are on, or from a subdirectory, you must set the DOS path variable to point to where HiTerm resides. You must also modify the *program.bat* file to point to the location of the configuration files. Refer to the instructions for installing HiTerm on a hard disk for more information.

HiTerm Configuration File

HiTerm uses a configuration file to specify the mode (General or Programmer) and the communication parameters. This file is read when HiTerm is invoked. If HiTerm is not able to use the configuration file, HiTerm will use the default settings and the following message will appear.

```
Unable to Use Config File
```

Several configuration files are included on the HiTerm disk; create any additional configuration files you desire. When creating your own configuration file, be sure each line conforms to the specifications shown below.

- **First line – mode.** Specify either General (G) or Programmer (P). You can use upper or lower case; only the first character of the word is significant.
- **Second line – baud rate.**
  The complete number is required, ie. 9600, not 96.
- **Third line – parity.**
  Specify None, Odd or Even (N/O/E). Use upper or lower case; only the first character of the word is significant.
- **Fourth line – data bits.**
  Specify 7 or 8.
- **Fifth line – stop bits.**
  Specify 1 or 2.
- **Sixth line – Com port.**
  Specify 1 or 2.

An example of a configuration file is shown below.

P
9600
N
8
1
1

Note: Comments can follow the first word (or character) as long as they are separated from the word by a space. The line must end with a line feed. (A ↵ is optional.)

HiTerm supports the following baud rates:

50	600	3600
75	1200	4800
110	1800	7200
150	2000	9600
300	2400	19200

HiTerm Default Settings

The following are the factory default settings and are used if no configuration file is present.

Parameter	Factory Default Setting
Mode	P (Programmer)
Baud Rate	9600
Parity	N (None)
Data bits	8
Stop Bits	1
Com Port	1

Transferring Files With HiTerm (Programmer Mode)

A special host command named "Transfer" is used by the programmer to communicate with HiTerm. Follow the steps below to either upload or download files. The files will be opened automatically and closed on the PC at the appropriate times.

Upload

1. From the More commands/Transfer data/Upload menu, make sure the Destination field reflects the correct programmer serial port (Terminal or Remote).
2. In the Upload host command field at the bottom of the screen, enter **transfer** ***<filename>*** [↵] or alternately, **tr** ***<filename>*** [↵] . Enter another [↵] to transfer the file.

Download

1. From the More commands/Transfer data/Download menu, make sure the Source field reflects the correct Programmer serial port (Terminal or Remote).
2. In the Download host command field at the bottom of the screen, enter **transfer** ***<filename>*** [↵] or, alternately, **tr** ***<filename>*** [↵] . Enter another [↵] to transfer the file.

High Speed Mode

General Information

HiTerm supports high speed downloads at 115.2Kbd. This can greatly reduce download times for large files if HiTerm is run on a 286 or 386 PC. The PC translates the data and then sends it to the Com port.

The speed of the download is affected primarily by two factors: speed of the processor in the PC and format of the data in the file to be downloaded. Since the PC will be translating the data, a faster processor will translate data and supply data to the Com port at a faster rate. The format of the file affects the speed because some formats require less time to translate (such as binary formats).

When a high speed download occurs, data will be transferred at a baud rate of 115.2Kbd regardless of the type of processor involved. However, slower processors may not supply the data to the Com port at the rate required to maintain a continuous flow of data to the programmer. Consequently, the download time will be slower even though the baud rate is 115.2Kbd. To benefit from the high speed download feature, HiTerm should be run on a PC at least as powerful as a 6MHZ 286.

During a high speed download, the PC translates the data in the user's file from its original format into an internal format required by the programmer. The formats which are currently supported by HiTerm for high speed downloads are listed below.

Format Name	Format Number
Binary	10
Intel Intellec 8/MDS	83
Intel MCS-86 Hex Object	88
Intel Hex-32	99
Motorola Exorcisor	82
Motorola Exormax	87
Motorola 32 bit (S3 record)	95

Performing a High Speed Download

To perform a high speed download, perform the following steps.

1. From the More commands/Configure system/Edit/Serial I/O parameters screen, ensure that the baud rate for the Remote port matches that of the Terminal port.
2. Go to the More commands/Configure system/Edit/Communication parameters screen.
3. Set the User Menu Port parameter to "R" (Remote). If it was already set to "R" proceed to Step 5.
4. Enter ↵ in response to the following message:

   ```
   Hit return to switch user menu port ,^Z to abort.
   ```

5. Move the cable currently on the terminal port of the programmer to the remote port.
6. Set the High speed download parameter to "Y".
7. Go to the More Commands/Transfer/Download screen.
8. Set the Source field to "R" (Remote).
9. Select the appropriate I/O translation format. This must be one of the formats currently supported by HiTerm in order to perform a high speed download. Otherwise, the transfer will be done at the normal baud rate.
10. To initiate the transfer, in the Download Host Command field, enter **transfer** ***<filename>*** ↵ or, alternately, **tr** ***<filename>*** ↵.

When the high speed download is started, the following message will be displayed on the programmer screen:

```
Transferring data in high speed mode
```

When this occurs, the programmer and HiTerm will automatically switch baud rates to 115.2Kbd and perform the data transfer. When the transfer is complete, the baud rates will be restored to their original rates and a message will be displayed indicating the operation is complete.

If the format number you have selected is not one of those supported for high speed transfer, the message

```
Transferring data
```

will be displayed and the transfer will occur at the normal baud rate.

CAUTION: ***Do not remove or insert device modules during high speed download operations.***

4 Commands and Functions

The following describes only the functions accessible from the Programmer mode Help menu.

Command	Function
Ctrl – R	Repaint the programmer screen.
Alt – F1	Terminates the HiTerm program, returns to DOS and closes any open files.
Alt – F2	Switches between Text mode and Binary mode for transferring files to the Com port. In the Text mode, certain characters will be stripped from the file during transfer. These characters are Control-Z, Control-C, Line-Feed, and Nulls. When transferring a file from the PC to a host while in text mode, an EOF character will be sent after the data to indicate the end of file. In Binary mode, no characters are stripped and no EOF character is sent following the end of the data. Binary mode is the recommended mode for operation with your programmer and is the default mode.
CAUTION:	***Do not use text mode to transmit files in JEDEC format or any of your programmer's binary formats, since filtering of control characters may result.***
Alt – F3	Displays the HiTerm help screen.

Alt – F4	Displays the current end-of-file character for text mode file transfers. To change this character, enter the hexadecimal value of the desired control character (ASCII 01 through 1F). Press ↵ to select the new character. The default setting is Control-Z (1A Hex). This parameter applies only to text mode. If text mode is used, the EOF character must match that which is selected on the programmer's Communications Parameters screen.

Note: HiTerm operating in the Programmer (P) mode automatically closes the file after Upload and Download operations without the need of an EOF character.

Alt – F5	Allows the user to change directories from within HiTerm. Enter the path for the directory you want to change to. You may change to a different drive also by entering the drive letter followed by a colon (**A:\UTIL**).
Alt – F6	Displays the directory for the drive and path specified.

The status line at the bottom of the screen displays the current settings of various HiTerm parameters and also indicates how to access the HiTerm help screen Alt – F3 . The fields on the status line are described below.

[Caps]	The Caps-Lock key is enabled
[Num]	The Num-Lock key is in the Number mode
[Text]	The file-transfer mode is set to Text mode
[Bin]	The file-transfer mode is set to Binary mode
[EOF=XX]	Indicates the end of file character (only used for file transfers in text mode)

5 Messages

HiTerm error messages appear at the bottom of the screen.

Can't change directory	HiTerm was not able to perform the change directory function to the specified directory. Ensure that the directory entered is correct.
Chars lost	Indicates that HiTerm encountered an error when attempting to close a file.
Data overrun on com port	The UART received another character before the previous one was read by the processor, causing data to be lost. Try using a slower baud rate or eliminate any background programs currently running on the PC.
Default comm param used	HiTerm detected a syntax error in the communication parameters specified in the configuration file. HiTerm will use the mode specified in the file. However, it will use the default values for the communication parameters. Make sure the syntax and values specified in the configuration file are correct.
EOF not used in Bin mode	This message appears if the user attempts to specify an end-of-file (EOF) character while HiTerm is in Binary mode. The EOF character has no significance for Binary mode; it is used only for Text mode.
File I/O error	HiTerm encountered an error during a file access. If this occurred while attempting to send a file from the PC to the Com port, verify that the file actually exists. If this error occurred while transferring data to a file, ensure that enough space exists on the disk to accommodate the data.
File(s) not found	HiTerm was unable to find the file specified by the user. Ensure that you entered the correct filename.
Framing error on com port	The received character did not contain a valid stop bit. Make sure the baud rates of the PC and the programmer match. If that is not the problem, try using a slower baud rate.

Not enough memory for HiTerm

This indicates there is not enough free memory available in the PC. HiTerm requires a minimum of 128K bytes of RAM. Remove other programs from memory or add more RAM.

Parity error on com port

The parity of the data received did not correspond with the parity setting of the UART in the PC. Make sure the parity settings in the PC and the programmer are the same.

Transfer Error

This indicates HiTerm did not close the file on the PC automatically. Make sure the HiTerm mode is set to Programmer (P). If the mode is correct, try using the pacing delay feature on the programmer, or a slower baud rate.

Unable to use config file

HiTerm either couldn't find the configuration file or there was an error detected in the configuration file. Make sure the *program.bat* file has been modified correctly to point to the location of the configuration files.

If you specified a configuration file on the command line when you typed **program**, make sure the configuration filename was correct. Check the contents of the configuration file used (*prg9600.cfg*, if not specified on the command line) to ensure there are no syntax errors. If this error occurs, HiTerm will use the default parameters.

SetSite Module

User Manual

DATA I/O
Corporation

981-0230-002

April 1990 981-0230-002

Data I/O has made every attempt to ensure that the information in this document is accurate and complete. However, Data I/O assumes no liability for errors, or for any damages that result from use of this document or the equipment which it accompanies.

Data I/O reserves the right to make changes to this document without notice at any time.

Acknowledgments:

6 *Troubleshooting*

If you cannot invoke HiTerm or are having difficulty with the transfer command, check the following:

1. Invoke the HiTerm Help screen [ALT] – [F3] and make sure the mode of HiTerm is set to "Programmer" (P). The mode is specified in the configuration file.
2. When you are using the Transfer command, make sure you are using the correct syntax on the host command line of the programmer transfer menu.
3. If the programmer menu is not present or complete on the PC screen, press [CTRL] – [R] to repaint the Programmer menu.
4. Be sure to type **program** to invoke HiTerm. Do not type the word "HiTerm," since this will bypass the *program.bat* batch file, which is necessary for invoking the default configuration file if one is not specified on the command line.
5. Make sure the programmer's baud rate matches the HiTerm baud rate. The programmer's factory default setting is 9600 baud.
6. Make sure the programmer is connected to the correct Com Port on the PC (default is Com1).
7. If the programmer indicates framing, parity or overrun errors during high speed downloads, the communication board in your PC may not be able to support data transfers at 115.2Kbd. Disable the high speed download feature or use a different Com board in your PC.
8. Make sure that the terminal type on the programmer is set to VT-100 (ANSI 3.64). You can check this on the programmer's power up screen.

The data fields left blank by the **040]** command — the Electronic ID field and the Module Support field — should not be needed in most CRC driver applications since that information is not required for device operations. However, if you need the data in these fields, you can obtain it in one of two ways. You can use the **240]** command to upload the full set of device support information. Or, you can use the **040]** command to upload the terse set of device support information and then use the **140]** command to get information for a particular device after selecting the device.

040]

Upload Terse Device List — The **040]** command uploads a terse list of all the devices supported by the programmer. The only difference between the **040]** and the **240]** commands is that some fields in the data stream returned by the **040]** command are zeroed out. The zeroed out fields are represented below as "Zeroes". The data is transferred as a string of characters in the following format:

Definition	Number of Bytes
Number of manufacturers	2
<CR><LF>	2 hex

Next is data for EACH device manufacturer, organized as follows:

Device manufacturer's name	1 to 32
Colon	1
Number of devices for this manufacturer	3

Next, the following is repeated for each device this manufacturer supports:

<CR><LF>	2 (hex)
Device's part number	1 to 32
Colon	1
Family code	4
Pinout code	4
Zeroes	8
Zeroes	2

<CR><LF> next device for *this* manufacturer . . . etc.
<CR><LF> next manufacturer . . . etc.

140]

Upload Current Part Information — The **140]** command uploads information about the currently selected device. If the device has been selected by family/pinout code, the silicon signature is set to 0. The current part information is transferred as a string of characters in the format described below.

Definition	Number of Bytes
Device manufacturer's name	1 to 32
Colon	1
Device's part number	1 to 32
Colon	1
Family code	4
Pinout code	4
Electronic ID	8
unused	2

240]

Upload Verbose Device List — The **240]** command uploads a verbose list of all the devices supported by the programmer. The only difference between the **040]** and the **240]** commands is that some fields in the data stream returned by the **040]** command are zeroed out. The data is transferred as a string of characters, in the following format:

Definition	Number of Bytes
Number of manufacturers	2
<CR><LF>	2 hex

Next is data for EACH device manufacturer, organized as follows:

Device manufacturer's name	1 to 32
Colon	1
Number of devices for this manufacturer	3

Next, the following is repeated for each device this manufacturer supports:

<CR><LF>	2 (hex)
Device's part number	1 to 32
Colon	1
Family code	4
Pinout code	4
Electronic ID	8
unused, reserved field	2

<CR><LF> next device for *this* manufacturer . . . etc.
<CR><LF> next manufacturer . . . etc.

49]

Suspend CRC Mode — Suspends CRC mode temporarily and returns to Terminal mode. While in Terminal mode, menu data will be sent to the port specified by the User Menu Port parameter. The values for all system parameters will still contain the values they had while in CRC mode prior to the **49]** command. Any changes to the parameters will apply to CRC mode when CRC mode is resumed.

The **49]** command allows you to temporarily leave CRC mode, perform some operations and then re-enter CRC mode with the system parameters unchanged. For example, the following scenario would be possible with the **49]** command:

- Enter CRC mode
- Select a device manufacturer (*xxx...xxxx***33]** command)
- Select a device part number (*xxx...xxxx***34]** command)
- Change the setting of some programming parameters, such as illegal bit check, blank check, etc. (*hhh***2A]** command)
- Suspend CRC mode and return to Terminal mode (**49]** command)
- Perform terminal functions, such as viewing a fuse pattern or editing memory
- Re-enter CRC mode (At this point, the changes to the programming parameters mentioned above would still be in place.)
- Program the device

Note: The **49]** *command differs from the* **Z** *command (Exit CRC Mode). The* **Z** *command exits CRC and sets the system parameters to the values they had prior to entering CRC mode. Entering CRC mode after previously exiting CRC mode with the* **Z** *command will cause the system parameters to be set to CRC default values.*

***n*4A]**

Get Filename From Disk — Displays the current filename or scrolls backwards or forwards through the filenames of the files found in the disk drive(s). Valid arguments are listed and described below:

0 uploads the filename of the next file in the directory list

1 uploads the filename of the previous file in the directory list

2 rebuilds the directory list and uploads the filename of the first file

The ***n*4A]** command is designed to be used as a front end to the *xxx...xxx***38]** command. Use the ***n*4A]** command to get a filename which can be sent with the *xxx...xxx***38]** command to load the file from disk.

***n*4D]**

Select Algorithm Source — Selects which set of algorithms to use with the *xxx...xxxx***33]**, *xxx...xxxx***34]**, ***n*40]**, and @ commands. Valid arguments are listed and described below:

0 Use the set of algorithms included on the Algorithm disk.

1 Use the extended set of algorithms (if any are available). Devices are selected from the ALG.EXT file.

2 Use the Keep Current set of algorithms (if any are available). The Keep Current algorithms are downloaded from the Keep Current BBS. See the documentation behind the Keep Current tab for more information.

The *n*4D] command allows you to switch between the algorithms that are included on the Algorithm disk and, for example, a collection of Keep Current algorithms. Consider the following scenario:

- Enter CRC mode
- Select the standard device file (*0*4D] command)
- Select a device manufacturer (*xxx...xxxx*33] command)
- Select a device part number (*xxx...xxxx*34] command)
- Program the device (P command)
- From your PC, download an updated version of the algorithm from the Keep Current BBS. See the Keep Current documentation for more information. Transfer the Keep Current algorithm to a 3.5" disk.
- Select the Keep Current device files (24D] command)
- Select a device manufacturer (*xxx...xxxx*33] command)
- Select a device part number (*xxx...xxxx*34] command)
- Program the device with the Keep Current algorithm (P command)

The above example is a typical example of how to use the *n*4D] command to select a different algorithm source.

A7] **Swap Bytes** — Swaps the high bytes and the low bytes in a given memory range. Use the *hhhhhh*< and *hhhhhh*; commands to specify the memory begin address and the size of the memory range to swap. The memory begin address (specified by the *hhhhhhhh*< command) added to the block size (specified by the *hhhhhh*; command) cannot exceed the size of user memory. Also, the block size must be an even number.

Entering a block size of 0 will swap all memory beginning with the address specified by the *hhhhhhh*< command.

Note: This command will not work if you have a logic device selected.

If you want to swap high- and low-order nibbles, see the Q command for more information.

DC] **Device Check** — Checks for the presence of a device in the socket. If the socket is empty, the DC] command returns an F. Error code 3B will be returned after the X command is sent. If a device is in the socket, further device checks are done if the device supports insertion and socketing tests. For example, the DC] command returns a device insertion error if the device is mis-socketed. If a device is in the socket and no continuity errors occur, the DC] command returns the normal > prompt.

*hh*2D]

Vector Test Options — Enables or disables the compensated vector test, serial vector test, and high speed logic driver options. Valid arguments are listed and described below:

Bit 0 = 0 to disable compensated vector test
Bit 0 = 1 to enable compensated vector test
Bit 1 = 0 to disable high speed logic driver
Bit 1 = 1 to enable high speed logic driver
Bit 2 = 0 to disable serial vector test
Bit 2 = 1 to enable serial vector test

2F] or *nn*2F]

View 8-Character Sumcheck — Returns the 8-character hexadecimal sumcheck of the data in User RAM. Refer to the S command for more information.

*xxx...xxxx*30]

Set Data File Name — Sets the filename for any subsequent file operations.

*n*31]

Set Data Source/Destination — Sets the source/destination for a data file. Valid arguments are listed and described below:

0 = RAM

1 = Disk

2 = RAM file

*xxx...xxxx*33]

Select Device Manufacturer — Selects the device manufacturer for device operations. Valid arguments can range from 1 to 13 alphanumeric characters. Valid arguments must also match the manufacturer name exactly as it appears on the Manufacturer List screen or as it is uploaded via the 40] command. The manufacturer selected does not take effect until the 34] command is sent to select the device part number.

*xxx...xxxx*34]

Select Device Part Number — Selects the device part number for device operations. Valid arguments can range from 1 to 29 alphanumeric characters. Valid arguments must also match the part number as it appears on the Parts Number screen for the selected Manufacturer or as it is uploaded via the 40] command. This command selects an algorithm based on the part number sent in this command and the Manufacturer sent in the 33] command.

xxx...xxxx38]

Load File From Disk — Loads a disk file into RAM. Valid arguments range from 1 to 14 alphanumeric characters. The entire file is always loaded, and the User Data Size is updated to reflect the size of the file loaded into RAM. Drive A is the default drive. To load a file from the B drive, precede the filename with a B:. For example, B:27128.DAT38].

39]

Delete All RAM Files — Clears RAM files from memory. Use this command to keep UniSite from running out of RAM space for files. RAM files stay in memory until this command is sent to clear them.

*xxx...xxxx*3B]

Delete Disk File — Deletes a disk file. Valid arguments range from 1 to 14 characters and may include the * wildcard character. Drive A is the default drive. To delete a file from the B drive, precede the filename with a B:, for example, B:27128.DAT3B].

*n*3C]

Set Data Transfer Port — Specifies which port (Terminal or Remote) UniSite will use for CRC data transfer operations (such as the input, output and JEDEC input/output commands). Unless specified otherwise, UniSite defaults to the Remote port for data transfer operations. This command makes it possible to transfer data to UniSite from a system other than the one currently running your CRC driver program. The driver program would be communicating with the Remote port of UniSite and could initiate a download or upload with a different computer connected to the Terminal port of UniSite. This is useful if the data files which you want to use exist on a system other than the one running your CRC driver program. CRC commands are still recognized only on the Remote port. Valid arguments are listed and described below:

0 Remote Port
1 Terminal Port

*xxx...xxxx*3E]

Select Keep Current algorithm — The Keep Current algorithm is loaded from the specified .KC*x* filename. With this CRC command, Keep Current algorithms with different revision numbers may be selected for the same device.

*n*40]

Upload Device Information — Depending on the argument supplied, the *n*40] command uploads either a terse list of all the supported devices, information about the currently selected device, or a verbose list of all the supported devices. Valid arguments are listed and described below:

0 upload terse list of all devices supported

1 upload current device information

2 upload verbose list of all devices supported

Note: The 040] *and* 240] *commands — the terse and verbose lists of devices supported — share the same format. Certain fields in the terse list are zeroed out, making the upload quicker.*

While the 040] and 240] commands yield results that appear to be insignificantly different, the two commands operate in ways that can affect the performance of a CRC driver.

The 240] command needs to access data stored on the Algorithm and System disks to build the data stream it returns. This means that the upload of device information could take longer than desired.

On the other hand, the 040] command does not need to access data on the Algorithm and System disks. As a result, the 040] command provides a quicker method of uploading device support information.

*n*41]

Upload Self Test Results — 041] returns the results of the previous self-test as a 30-character string in which each character represents the results of a different test. The tests and their positions in the string are described below.

Character Position	Item Tested	Character Position	Item Tested
1	Spare	16	Pin Driver board 7
2	EPROM	17	Pin Driver board 8
3	System RAM	18	Pin Driver board 9
4	User RAM	19	Pin Driver board 10
5	Serial port A	20	Pin Driver board 11
6	Serial port B	21	Pin Driver board 12
7	Disk drive A	22	Pin Driver board 13
8	Disk drive B	23	Pin Driver board 14
9	Option board	24	Pin Driver board 15
10	Pin Driver board 1	25	Pin Driver board 16
11	Pin Driver board 2	26	Pin Driver board 17
12	Pin Driver board 3	27	Waveform generator board
13	Pin Driver board 4		
14	Pin Driver board 5	28	Pin Control Unit
15	Pin Driver board 6	29	PSM board
		30	FSM board

Each test can produce one of four result codes, which are described below:

– Hardware not installed

? Untested

F Failed self-test

P Passed self-test

43]

Upload Yield Tally — Uploads the yield tally for up to sixteen different devices. The yield tally is uploaded in the following format:

Manufacturer's name or family/pinout	25 characters
Total parts attempted	5 characters
Space	1 character
Total parts passed	5 characters
Space	1 character
Total illegal bit/blank errors	5 characters
Space	1 character
Total verify errors	5 characters
Space	1 character
Total structured test errors	5 characters
Space	1 character
Total program failures	5 characters
Carriage return, line feed	2 characters

There is one line returned in the format above for every device entry in the yield tally statistics file.

46]

Clear Yield Tally — Clears the yield tally statistics.

Table of Contents

1 Introduction

Data I/O's SetSite module allows you to perform set or gang programming operations with the UniSite (set and gang programming are defined on the following pages). SetSite programs MOS/CMOS EPROMs and EEPROMs in the DIP style package. See the device list shipped with each UniSite software update for a complete list of supported devices. Devices programmable with SetSite are listed in the Product Module column on the device list.

Included here are applications for using SetSite and explanations of memory allocation for set/gang programming. If you have never used UniSite before, read through the "Sample Sessions" section of the UniSite Operator's Manual. The procedures and explanations in the SetSite manual assume at least a basic working knowledge of how UniSite operates.

The following information is contained in this manual:

Compatibility	Describes compatibility requirements between UniSite and SetSite.
Specifications	Describes SetSite's physical and operating specifications.
SetSite Features	Describes how to select gang/set programming.
Operating SetSite	Provides description of SetSite specific screens and functions.
Set and Gang Programming	Provides examples of set and gang programming.
Applications	Provides examples of how UniSite and SetSite may be used in a programming environment.
SetSite Messages	Provides details on SetSite specific messages.

Compatibility

Whether or not SetSite is compatible with your UniSite depends on (1) the version of UniSite software diskette you are using and (2) your memory requirements. The SetSite module is fully compatible with any UniSite that has a V2.0 (or later) system disk. If you are using SetSite, ChipSite, or PinSite and the part number of your UniSite is 901-0058-007 or less, it is recommended that you have the UniSite updated. This will be done as part of the standard warranty and is required to assure that SetSite will operate properly with all devices.

Memory requirements depend on the type of device, the set size and word-width you want to use for set programming. UniSite has a standard user RAM size of 128K x 8. Using this architecture, you could gang program up to eight 1Mbit devices (programming the SAME data into all eight parts). Set programming the same eight 1Mbit devices (programming so each device has a DIFFERENT block of data) would require 1Mbyte of user RAM. Should your programming needs require it, Data I/O offers upgrades for additional RAM. Contact your local Data I/O Service Center for more information about the RAM upgrades.

Note: If the disk is being used as user memory (instead of RAM), the user memory you have available is limited by the free space currently available on the disk. The disks have a capacity of 720 Kbytes when newly formatted.

If you need to check what your UniSite's current configuration is, remember that both the RAM size and software configurations appear on the upper-right portion of most of the UniSite screens.

Specifications

Physical	11.75 X 8.5 X2.5 in.
Temperature	Operating range: +5 to +40 C
Humidity	Up to 90%, non-condensing
Altitude	Operational to 10,000 ft.

Features

Selecting the SetSite Module

You may select the SetSite module in one of two ways: (1) in the Load, Program or Verify menus, pressing the [PF4] key until the SetSite screen is displayed or (2) using the "mode" parameter field in the MANUFACTURER LIST screen.

To select SetSite using the mode field, first enter the Select device menu (press [S] at the MAIN MENU). The MANUFACTURER LIST screen will then appear--the mode field is the reverse video block on the right. Move the cursor to the mode field. The space bar toggles the display between "Single device" and "Gang/set" mode. By choosing "Gang/set" mode, only the manufacturers and devices supported by the SetSite module will appear in the MANUFACTURER LIST and PART MENU FOR MANUFACTURER screens.

If you press [PF4] after selecting a Load, Program or Verify screen, the appropriate gang/set screen will appear. Screens which are specific to the SetSite module operation are different than for other UniSite modules and display information on-screen for each of the eight device sockets.

Pressing the [PF4] key allows you to select between the "non-default" or "all parameters" screens for either the PSM (smaller) module or the FSM (larger) module. These represent the four selections possible with the [PF4] key. UniSite will sequence through these four selections with the [PF4] key. The "ready" LED will light for the module currently selected. Devices should be removed from any module which is not selected.

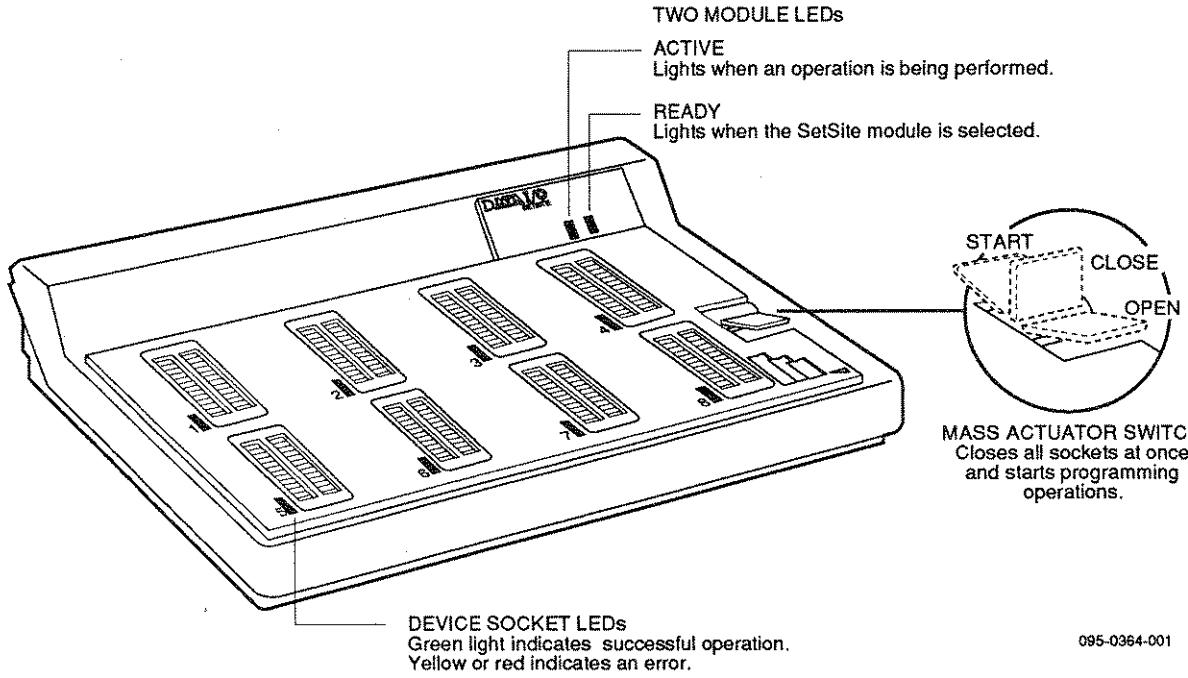
Start Switch

The SetSite module is shown below in Figure 1. The eight 40-pin DIP sockets have a "mass-actuation" feature: there is only one socket lever on the module. Moving this lever moves ALL the socket contacts.

The socket lever has three positions: open, close and start. Because the lever is spring-loaded, it will automatically return to the closed (straight-up) position after being pushed to the start position. The start position – lever pushed forward toward the ACTIVE/READY indicator panel – initiates (starts) Load, Program or Verify operations, just like pressing [↵] on the terminal keyboard.

The socket lever also functions as an interrupt or [Break] key. If you pull the switch back (thereby opening the socket contacts) while an operation is in progress, that operation will be halted.

Figure 1-1
The SetSite Module



LED Indicators

SetSite has two module LEDs and eight individual socket LEDs. The two module LEDs indicate the current status for the entire unit. The "READY" LED lights yellow when SetSite is ready for use. The "ACTIVE" LED lights yellow whenever an operation (such as programming parts) is taking place.

CAUTION: When the "ACTIVE" LED is lit, programming voltages are being applied to the device sockets. You should not remove socketed devices or remove the SetSite module from UniSite when the "ACTIVE" LED is illuminated.

LEDs next to each socket indicate status of that socketed part. The LEDs light green to indicate a successful operation; yellow or red indicates an error. A red LED signals a "fatal" error, meaning that the device cannot be programmed. A yellow LED signals a "non-fatal" error--the device can still be programmed. (For example, a "non-blank device" error is non-fatal because even though the device is found to contain programmed bits, those locations can still be programmed over). The table below shows conditions and LED colors corresponding to each.

Condition	LED Color
Module	
SetSite READY for use	"READY" yellow
Operation executing	"ACTIVE" yellow
Socket	
Device programmed successfully	green
Device errors	
Non-blank	yellow
Backwards device	red
Wrong silicon signature	red
Illegal bit	red
Programming error	red
Verify error	red
Empty socket	LED off

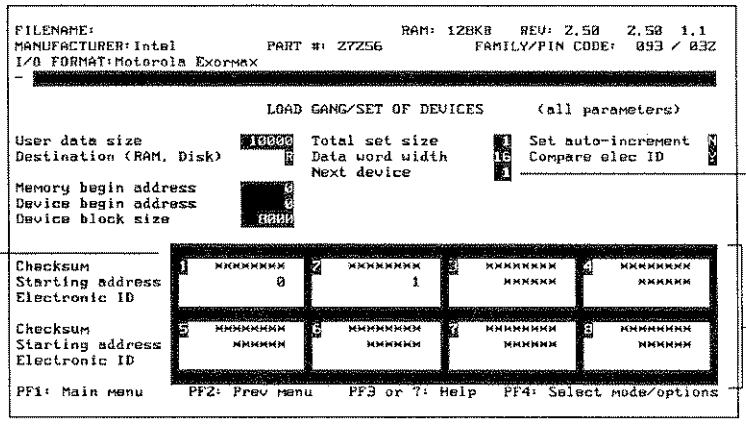
2 Operation

SetSite Screens

When the SetSite module has been selected (using one of the two methods described in the previous subsection), the SetSite screens will appear. These screens are different than the screens (see the figure below) for the other modules. This subsection describes the unique features of the SetSite screens.

Reverse video blocks at the bottom of the SetSite screen represent the eight SetSite sockets. Each block displays information for the socket it represents: error status, checksum, starting RAM address and electronic ID information is displayed here.

Figure 2-1
The SetSite Screen



MESSAGE AREA - tells status of device. Displays "PASS" if operation was successful; displays an error if there is a problem.

NEXT DEVICE - indicates next device in the set.

SOCKET DISPLAY - shows the Begin Device Address for each device, indicating the first address of user data to program or load from the device.

Information shown in each of the blocks will differ depending on what kind of operation you are performing. If you are doing a Load operation, the eight blocks show how UniSite's user memory will be allocated. If you are programming devices, the reverse video blocks show how the user data will be organized into the parts.

After any device operation (such as loading or verifying data) has completed, messages will appear in the area above each block. The messages indicate what the device's status is. PASS will appear above all successfully programmed parts. Any programming errors that might occur will display above the block where the error occurred. A list of SetSite's status and error messages can be found at the back of this manual.

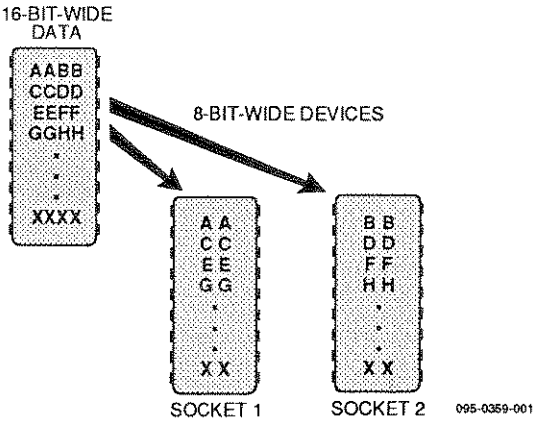
The "Next device" parameter on the screen can be used to visually scroll through the data organization. This feature is useful if you are programming partial sets of devices or if you are programming a set of more than eight devices. For example, say you are programming a set of 20 devices, and want to check status of organization in the ninth device of the set. If you move the cursor to the Next device parameter and type in 9, UniSite will redisplay the status data showing device number 9s status data in socket number one.

Set and Gang Programming

Set Programming

A "set" is defined as being one or more devices containing a unique block of data--regardless of how many devices that data is programmed into.

Figure 2-2
Set Programming - each device ends up with unique data.



SetSite can program any set size from one to 99. If you choose a set size such that the number of devices is less than or equal to 4, then multiple sets can be programmed on the SeiSite module simultaneously. The way that data will be arranged in the devices programmed is determined by three factors: (1) the device word-width, (2) the data word-width and (3) the number of devices you want to have in each set. The general equation to use is

$$\text{Set Size} = \frac{\text{Device word-width}}{\text{Data word-width}} \text{ X Number of devices}$$

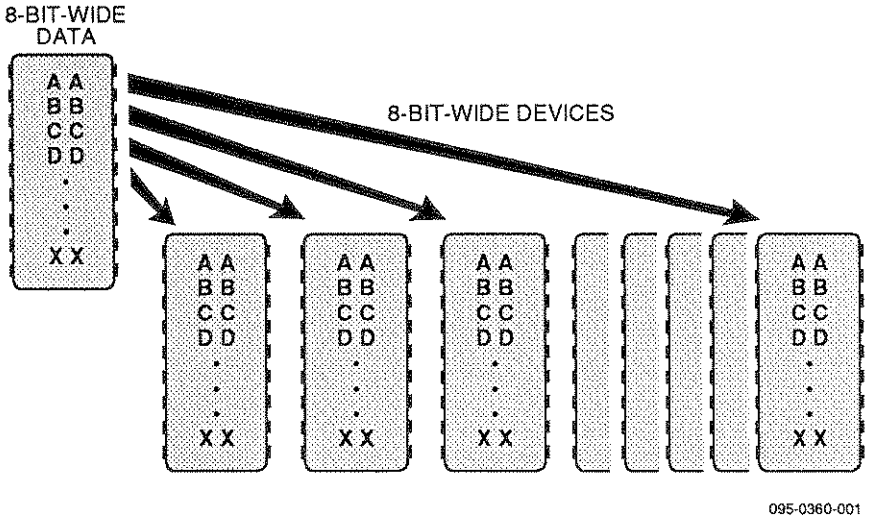
For example, if you are programming two 27128 devices, which are 8-bit-wide (device word-width) parts: If your programming data is constructed 16-bit-wide (data word-width) in the target system, the set size [8/16 x 2] equals one. The byte swap flag is enabled for this example.

Gang Programming

"Gang" programming simply means that the same data will be programmed into each device: the set size is therefore equal to one (and the device word-width should equal the data word-width).

If you want to perform gang programming operations with SetSite, you will need to specify a set size of ONE in the Programming data entry screen.

Figure 2-3
Gang Programming - the programmed devices all have the same data.



3 Applications

This part of the SetSite manual includes examples of how UniSite and SetSite might be used in a programming environment. Three examples are given here:

- Gang programming eight 27128 devices — programming the same data into all eight parts.
- Set programming devices — programming devices so that each ends up with unique data.
- Programming a partial set of devices — using only part of the original block of data to program the devices.

Gang Programming

This example shows how to load data from a master (already programmed) 27128 device into RAM and then gang-program that data into a set of eight blank devices.

1. Power up UniSite with the SetSite module installed (if necessary, refer to the procedure in the Operator's manual).
2. Using the Select device menu, select any 27128 EPROM from the manufacturers' and device type lists. When you have chosen a part, UniSite will return to the MAIN MENU.
3. Type [L] to go to the Load device menu. The Load Gang/Set of Device screen should then appear. If not, press the [PF4] key until the Load Gang/Set screen appears: the "READY" indicator will light yellow on SetSite's panel when SetSite has been selected.
4. The 27128 is a 16K X 8 part: there are 16K (or 4000 hex) addressable locations. Therefore, the "device block size" should be set at 4000. Check the device block size window and make sure that UniSite has set the "device block size" to 4000 and "data word width" to 8.
5. Check the "User data size" window. Make sure that the user data size is set at 4000.
6. Insert the master 27128 device into SetSite's socket number one; the socket at the upper-left of the module. The device should be inserted bottom-justified: no open socket pins below the device. Push the socket lever up to the closed position.
7. When you are certain the displayed screen parameters are correct, push the socket lever forward again to the START position (or press [↵] on the terminal keyboard) to start loading the data. The action symbol on the UniSite screen will rotate and when the operation is finished, a message will appear. Because the socket lever is "spring-loaded", it will automatically return to the closed position.
8. The screen will now show the data just loaded. The "total set size" will be 1, meaning that the entire set of data can be programmed into one device. A "0" appears in socket number one next to the starting Address parameter, meaning that data was loaded from socket one beginning at user memory address 0. Notice that asterisks appear inside the other device socket boxes on the screen: it is not possible to "gang-load" data into RAM with the set size equal to 1 (gang mode).
9. Press [PF2] to go back to the MAIN MENU. Open the sockets and remove the master device. Data is now loaded into RAM; the next part of the procedure explains how to program that data into the eight blank devices.
10. Type [P] to go to the Program Gang/Set of devices menu.

11. Insert the eight devices into the SetSite sockets. Push the socket lever up to the closed position. Notice that starting address 0 appears in the boxes for all eight devices on-screen. This means that UniSite will take data from user memory address 0 to program EACH device, so they will all end up with the same data.
12. Push the socket lever forward to the START position (or press [↵] on the terminal's keyboard) to begin programming the devices.
13. The action symbol on the UniSite screen will rotate and when the operation is finished, a message will appear. "PASS" will appear on the SetSite screen, above all sockets whose devices are successfully programmed.
14. The devices are now programmed. Pull the socket lever to the open position and remove the eight devices.
15. If you want to program eight more devices with the same data, simply repeat steps 11 through 14.

Set Programming

This example shows how to load data from a master (already programmed) 27512 device (containing a whole 64K set of data) into RAM and then set program that data into eight blank 27256 devices (4 sets): Because the 27256 has half the memory of the 27512, it will require two 256's to store an entire SET of data from a 512. The "set size", therefore, equals two. If eight devices are programmed, four sets (of two 27256's) will be produced.

The 27512 is a 64K X 8 part: it has 64K (or 10000 hex) addressable locations; the 27256 devices have 32K (or 8000 hex) addressable locations. So that you do not have to worry about calculating and entering memory block parameters for two different types of devices, UniSite will AUTOMATICALLY alter device parameters when the devices are READY to be programmed.

1. Power up UniSite with the SetSite module installed. (If necessary, refer to the procedure in the UniSite Operator's manual.)
2. Using the Select device menu, select any 27512 EPROM from the manufacturers' lists. When you have chosen a part, UniSite will return to the MAIN MENU.
3. Type [L] to go to the Load device menu. The Load Gang/Set of Device screen should then appear. If not, press the [PF4] key to display the different Load screens until the correct one appears. The "READY" indicator on SetSite's panel will illuminate when UniSite is ready.
4. Make sure the "device block size" window displays 10000, so that the device block size equals the selected device's size.

5. Make sure the "User data size" window displays 10000, and the "Data word width" shows 8. The "set size" will be 1, meaning that the entire set can be programmed into one device. A "0" appears in socket number one next to the starting Address parameter, meaning that data will be loaded from socket one beginning at user memory address 0. Notice that asterisks appear inside the other device sockets: it is not possible to "gang-load" data into RAM, only one device's data may be loaded at a time with a set size of 1.
6. Insert the master 27512 device into SetSite's socket number one. The device should be inserted bottom-justified: no socket pins below the device. Push the socket lever up to the CLOSED position.
7. When you are certain the displayed screen parameters are correct, push the socket lever forward to the START position (or press [↵]). The action symbol on the UniSite screen will rotate and when the operation is finished, a message will appear.
8. Pull the socket lever back to the open position and remove the device.
9. Press [PF2] to go back to the MAIN MENU. Data is now loaded into RAM; the next part of the procedure explains how to program that data into the eight blank devices.
10. Type [S] to enter the Select device screen. Select the 27256 device from the Select device menu. UniSite will then load the correct programming algorithm for the devices.
11. Type [P] to go to the Program Gang/Set of devices menu.
12. Even though you will be programming data into devices that are only half as big as the master, you will NOT need to change the Device block size parameters: UniSite does it automatically when you select the device.

Note: UniSite now displays "Set Size 2." This means the entire set of data from the 27512 can be programmed into two devices. Notice also the memory allocation shown at the bottom of the screen: starting address 0 is shown for the odd-numbered sockets; address 8000 is displayed for the even-numbered sockets. This display means that data from UniSite's RAM addresses 0000 to 7FFF will be programmed into half of the devices (those in odd-numbered sockets); data at addresses 8000 to FFFF will be programmed into the other four devices (those in even-numbered sockets).

13. Insert the eight devices into the SetSite sockets. Push the socket lever up to the CLOSED position.
14. When you are certain the displayed screen parameters are correct, push the socket lever forward to the START position (or press [↵]) to begin programming the devices.
15. The action symbol on the UniSite screen will rotate and when the operation is finished, a message will appear.
16. The devices are now programmed. Pull the socket lever back to the open position and remove the eight devices.

Programming Partial Sets of Devices

There are some applications which call for programming only part of a device set. UniSite and SetSite are designed to allow partial device operation with a minimum of effort on your part.

Reprogramming Devices

Say you are programming a set of eight devices and two of the eight in the set do not program successfully. To reprogram the two devices, this is what you would need to do:

1. Move the socket lever back to the OPEN position and remove the six programmed parts and the two bad devices.
2. With NEW devices installed in the socket positions of the two that failed, push the socket lever up to the START position (or press ↵), initiating the programming operation.

It does not matter what two sockets the devices are in; the six LEDs adjacent to the empty sockets will remain off. You also do not need to change any of the data block limits: UniSite will automatically assume you want to attempt programming the SAME data into the socketed parts.

Programming Sets of More Than Eight Devices

Programming using a set size of more than eight devices may also be considered "partial" set programming, since the set size is greater than the number of devices that SetSite can program simultaneously.

Devices in sets larger than eight can be programmed in two or more "partial" sets. UniSite can be viewed as being able to program a "window" of eight devices at a time, out of the total number in the set. You can position which eight devices to program using the "Next device" parameter mentioned in the Introduction section. By setting the "Next device" parameter to 1, 9 and 17, you could program successive windows of user data (eight devices at a time)

Note: You can accomplish the same thing using the "Auto Increment" feature. If Auto Increment is set to Y, UniSite will increment the "Next device" parameter for you.

For example, say you want to program 20 devices. With "Next device" set to 1, devices 1 through 8 would be programmed. After these first eight were programmed, you could set the "Next device" to 9 and then program devices 9 through 16. The last four devices could be programmed after "Next device" was set to 17.

The four empty sockets remaining when devices 17 through 20 were programmed would NOT cause an error to be generated; the socket LEDs would just remain off. If you use the "Set Auto Increment" feature, UniSite will reset the "Next device" window to 1 after these last four devices are programmed.

4 Messages

Below is a list of the messages that will appear on UniSite's screens when SetSite is being used. These messages will appear above the socket they pertain to; the introduction section of this manual shows a sample SetSite screen and illustrates where the message area is.

Data Load Err — An error occurred during a Gang/Set Load operation, and data was not correctly loaded from this part.

Device Alg Err — A device algorithm error has occurred.

Elec Erase Err — A device error occurred when UniSite attempted to electronically erase this part.

Empty Socket — UniSite has detected that this SetSite socket is empty. This display may appear if you are doing partial set programming and do not need to use all eight SetSite sockets. The operation will still be completed: this is a status message.

Elec ID Err — The electronic ID of the socketed device does not match the one UniSite has stored in its memory. Make sure the correct device type is installed or selected.

Illegal bit — UniSite has detected already-programmed locations of incorrect polarity in this socketed device. An illegal bit is a programmed device bit whose corresponding memory bit is unprogrammed.

Insertion Err — A device insertion error has occurred.

Non-blank Err — UniSite has detected programmed locations in this device. You may still program OVER the existing data if you wish (by pressing ↵ or moving the lever to START); this is merely a status message.

Overcurrent	An overcurrent condition was detected during the previous operation. One or more of the socketed devices may be faulty.
PASS	The operation just performed was successful for this device.
Program Err	This display indicates that a programming error has occurred during the last operation. Try another device. The socketed device may be faulty.
Secur Prog Err	An error occurred when UniSite attempted to program the security fuse of this device.
Security Violation	This device cannot be programmed because its security fuse bit is already set to the programmed state.
Verify (1st pass)	The socketed device failed the verify test at the manufacturer's low Vcc level or nominal Vcc level.
Verify (2nd pass)	The socketed device failed the verify test at the manufacturer's high Vcc level.
Verify (2 passes)	The socketed device failed the verify test at manufacturer's low and high Vcc levels.

Device Insertion Error

```
Device insertion error
```

Probable Cause	Solution
Device inserted improperly.	Ensure that the device is properly justified in the socket or properly oriented in the MatchBook.
Faulty device(s).	Check the device for bent or damaged pins/leads. Repeat the operation with similar devices from the same as well as other manufacturers. If the operation proves successful with similar devices, then the suspect part is probably defective.
Socket/pad is dirty or worn.	Examine the socket or pad for debris and wear. Clean or replace the socket or pad as necessary. Refer to documentation for cleaning and replacement instructions.
Possible bug in programmer software associated with continuity check.	If this error occurs during an attempt to load the device (via Load Device from the Main Menu), disable the Continuity Check parameter (change from "Y" to "N") in the Programming Parameters screen (via More/Configure system/Edit/ Programming options from the Main Menu). If the device is loaded successfully without insertion errors, try to program the device. If the device programs successfully, you've found a reasonable workaround. *Note: Report your findings to Data I/O Technical Support.*

Continuity problem with device/programmer interface.	If following the steps described in the previous section causes the device to fail programming, a subtle continuity problem may exist. **Workaround:** On your programmer's Device List find the earliest version of programmer software that supports the device, boot your programmer with this version, and attempt the operation again. If the operation is successful, you've found a temporary workaround. *Note: Report your findings to Data I/O Technical Support.*

Additional Information

The "Device insertion error" message is caused by a failure of the continuity check. During the continuity check, which is activated prior to device programming, the programmer applies low level current to each pin on the device to determine whether it is making good contact with the programming fixture.

After disabling the continuity test, we suggest loading a device rather than programming one. A load operation is less apt to harm the device because no programming voltages are applied.

Device Over-current Fault

Device over-current fault

Probable Cause	Solution
Improper device selected.	Make sure the device selection matches the manufacturer and part number of your device as precisely as possible. If it doesn't, select the proper characteristics and perform the operation again. *Note: Choosing a wrong manufacturer and/or part number (via Select device option from Main Menu) causes the programmer to expect an electronic ID different than your device's ID.*
Faulty device(s).	Load the suspect device (via Load device option from Main Menu). If an overcurrent error occurs, load new devices. If other devices load with no errors, a single device may be faulty. If no errors occur during load operation, try to program another device (via Program device option from Main Menu). If other devices program without error, a single device may be faulty. If other devices also produce overcurrent errors during load or program operations, check the date code. If failures occur only on devices with a particular date code while other parts are programmed or loaded successfully, the problem is probably device related. *Note: If the problem appears to be device related, you may wish to notify the device manufacturer.*

Possible bug in software associated with device tests.	If other devices produce overcurrent errors during load and program operations, disable the Continuity check parameter displayed on the Programming Parameters screen (via More/ Configure system/ Edit/Programming options from Main Menu). If this error occurs during a program but not a load operation, a device test may be causing the problem. Disable all device checks listed on the Program Device screen (such as Device check and Illegal bit check) by changing the appropriate fields from "Y" to "N." Press the F4 key to display all parameters.
Improper algorithm applied by programmer due to possible bug in software.	If this error occurs on devices with old and recent date codes, there may be a software bug in the device's programming algorithm. **Workaround**: On the programmer's Device List, find an earlier version of programmer software that supports your device, boot your programmer with this version, and repeat the operation. If the operation is successful, you've found a temporary workaround. *Note: Report your findings to Data I/O Technical Support.*
Programmer hardware problem.	An overcurrent error occurring with different devices may indicate a hardware problem. Perform a self-test (via More/Self-test options from main menu) with no devices in the socket to determine whether a hardware malfunction exists. If so, make the necessary service arrangements.

Additional Information

This error is reported by the hardware overcurrent detection circuitry on the programmer. The trip level for the overcurrent error is set by the programming algorithm. From the error alone, it is not possible to determine which operation the programmer was performing (device tests, program, verify/read) when the overcurrent condition was detected. To determine the nature of the problem, you need to isolate the operation being performed.

Device Programming Error

```
Device programming error
```

Probable Cause	Solution
Improper device selected.	Make sure the device selection matches the manufacturer and part number of your device as precisely as possible. If it doesn't, select the proper characteristics and perform the operation again. *Note: Choosing the wrong manufacturer and/or part number (via Select device option from the Main Menu) causes the programmer to expect an electronic ID that differs from the ID in your device.*
Faulty device(s).	Program at least one more device labeled with the same date code. If the operation is successful, the original device is probably faulty. If other devices with the same date code fail, try to program devices labeled with different date codes. If devices with different date codes are programmmed successfully, the devices from the original date code are probably faulty. *Note: You may wish to contact the device manufacturer and report your findings.*
Improper algorithm applied by programmer due to recent change in manufacturer specifications.	If this error occurs only on devices with recent date codes, the devices may require a modified programming algorithm. *Note: You may wish to contact the device manufacturer to determine whether the programming specifications for the device have changed. If they have, please notify Data I/O Technical Support.*

Improper algorithm applied by programmer due to possible flaw in programmer software.	If this error occurs on devices spanning old and recent date codes, this error may indicate an algorithm-related problem in your programmer software. **Workaround:** On the programmer's Device List, find the earliest version of programmer software that supports your device, boot your programmer with this version, and repeat the operation. If the operation is successful, you've found a temporary workaround. *Note: Call Data I/O Technical Support and report your findings.*

Additional Information

A device programming error is reported when a repeated attempt to program a particular cell or fuse has failed. This error may be caused by a faulty device or an improper programming algorithm.

Electronic ID Verify Error With Memory Device

`Electronic ID verify error. Device = hex value`

Probable Cause	Solution
Improper device selected.	Make sure the device selection matches the manufacturer and part number of your device as precisely as possible. If it doesn't, select the proper characteristics and perform the operation again. *Note: Choosing the wrong manufacturer and/or part number (via Select device option from Main Menu) causes the programmer to expect an electronic ID that differs from the ID in your device.*
Device manufacturer has changed the Electronic ID of the part and programmer does not recognize it.	If the device is labeled with a recent date code, the manufacturer may have placed a new electronic ID on the device that is not recognized by your programmer. To minimize ID errors, use the latest version of your programmer software. **Workaround:** If your programmer is at the current version, disable the Compare elec ID parameter (change from "Y" to "N") under the Load Device, Program Device, Verify Device, or Programming Parameters screens. *Note: You may wish to contact the device manufacturer to find out if they changed the ID on the device. If they did, please notify Data I/O Technical Support.*
Faulty device(s).	If disabling the Compare elec ID parameter causes an operation (such as load, program, or verify) to fail, try the operation on other devices with the same date code. If the operation is successful on these devices, the original device may be defective. *Note: If a high percentage of parts fail the operation, you may wish to contact the device manufacturer and report your findings.*

Possible bug in programmer software.	If disabling the Compare elec ID parameter causes the operation to fail on a high percentage of parts across several date codes, there may be a software bug in the programming algorithm associated with the part. **Workaround:** On the programmer's Device List, find the earliest version of programmer software that supports the device, boot your programmer with this version, and repeat the operation. If the operation is successful, you've found a temporary workaround. *Note: Report your findings to Data I/O Technical Support.*

Additional Information

Most memory devices are uniquely identified by their silicon signatures (electronic IDs). At times, device manufacturers change the electronic IDs of devices that undergo changes in the manufacturing process. Typically, the electronic ID is altered to promote automatic device selection and usually does not reflect a change in the device programming specifications. Consequently, disabling the electronic ID check is a viable workaround for most memory devices.

When this error occurs, the electronic ID of the device is displayed. You can also determine the electronic ID of your part by selecting the Compare Elec ID the Device checks option (via More/ Device checks from Main Menu).

The Compare elec ID parameter is located in the Load Device, Program Device, Verify Device and Programming Parameters screens. To display the full parameter list under the Load Device, Program Device, and Verify Device screens, press the F4 function key.

Illegal Bit Error

```
Illegal bit error
```

Probable Cause	Solution
Windowed device contains data.	Perform a blank check on the device (via More/Device checks options from the Main Menu) to determine whether it is truly blank. If blank check reports "non-blank device," place the device under a UV lamp and allow sufficient time to fully erase. After erasure, reprogram the device.
Electrically erasable (EE) device contains data and device's electronic erase feature is not enabled.	Make sure that the device's electronic erase feature (Erase EE Device parameter under the Program Device screen) is enabled (set to "Y"). Reprogram the device after the electronic erase feature has been enabled. *Note: To display all parameters on the Program Device screen, press the F4 function key.*
One Time Programmable (OTP) device contains data.	Perform a blank check on the device to determine whether the device contains data. If so, your OTP device had been previously programmed and most likely cannot be over-programmed with different data or fuse pattern. Program another device.
Faulty device(s).	Program at least one more device labeled with the same date code. If it programs successfully, your original device was probably faulty. If other devices with the same date code also fail, attempt to program devices labeled with different date codes. If these devices program successfully, the devices from the original date code are probably faulty. *Note: You may wish to contact the device manufacturer and report your findings.*

Improper algorithm applied by programmer due to recent change in manufacturer specifications.	If this error occurs only on devices with recent date codes, the devices may require a modified programming algorithm. *Note: You may wish to contact the device manufacturer to determine whether the programming specifications for the device have changed.*
Improper algorithm applied by programmer due to possible bug in programmer software.	This error, if it occurs on devices with old to recent date codes, may indicate an algorithm-related problem in your programmer software. **Workaround:** On your programmer's Device List, find the earliest version of programmer software that supports the device, boot your programmer with this version, and attempt the operation again. If the operation is successful, you've found a temporary workaround. *Note: Report your findings to Data I/O Technical Support.*

Additional Information

An "illegal bit error" indicates that at least one location in the device contains data (programmed state) while its corresponding location in RAM has no data (unprogrammed state). For example, the unprogrammed state of a PROM is 0, while its programmed state is 1. If a particular 8-bit PROM's memory location contains 09 hex (00001001 binary) and the corresponding memory location in RAM contains F0 hex (11110000 binary), then an "illegal bit error" will occur because the programmer is not able to unprogram the first and fourth least significant bits.

Invalid Device ID On Logic Device

```
Invalid device ID
```

Probable Cause	Solution
Improper device selected.	Make sure the device selection matches the manufacturer and part number of your device as precisely as possible. If it doesn't, select the proper characteristics and perform the operation again. *Note: Choosing the wrong manufacturer and/or part number (via Select device option from the Main Menu) causes the programmer to expect an electronic ID that differs from the ID in your device.*
Device manufacturer has changed the device ID of the part and programmer doesn't recognize it.	If the device is labeled with a recent date code, the semiconductor manufacturer may have assigned a new device ID to the part that is not recognized by your programmer. To minimize ID errors, use the latest version of your programmer software. *Note: If your programmer is at the current version, you may wish to contact the device manufacturer to determine if they changed the device's ID. If they did, contact Data I/O Technical Support.*
Faulty device(s).	Attempt the operation with at least one more device labeled with the same date code. If the operation is successful, the original device is likely faulty. *Note: If a high percentage of parts produce ID errors, you may wish to contact the device manufacturer and report your findings.*

Possible bug in programmer software.	A high percentage of parts failing with ID errors may also indicate that a bug exists in the programming algorithm software associated with the part. **Workaround:** On your programmer's Device List, note the earliest version of programmer software that supports the device, boot your programmer with this version, and repeat the operation. If the operation is successful, you've found a temporary workaround. *Note: Report your findings to Data I/O Technical Support.*

Additional Information

Most logic devices are uniquely identified by their device IDs. Semiconductor manufacturers issue new IDs to reflect changes in manufacturing processes that may produce modifications to device programming algorithms.

Data I/O engages in ongoing communication with semiconductor manufacturers and is usually informed when device IDs change.

I/O Timeout Error

`I/O timeout error.  Data sum = Hex Value`

Probable Cause	Solution
Wrong download command sent to host.	Your host machine (PC-DOS, Sun, VAX, etc.) will transfer a file upon receipt of the proper command. Under HiTerm, for example, the Download Host Command must begin with "tr" or "transfer" followed by the appropriate drive letter, path and filename. Refer to your programmer's User Manual, *HiTerm User Manual*, or host documentation for more information.
Wrong I/O translation format code selected.	The format of the file being transferred must match the description in the programmer's User Manual. If it doesn't, enter the proper I/O translation format number and transfer the file again.
Unrecognized characters in beginning of file.	The data file must begin with characters that match the appropriate format described in the programmer's User Manual. Remove any characters in the data file that the programmer will not recognize. In general, ensure that the format of the data file conforms to the description in the "Translation Formats" section of your User Manual.
No recognizable end-of-file character or record in file.	The data file must end with the proper end-of-file character or record, as described in the programmer's User Manual under the I/O translation format type selected. Add the end-of-file character or record, if it is missing. Of course, this does not apply to binary files, which have no end-of-file character or record.

Additional Information

This error occurs when a file is being transferred from systems such as a PC, Sun or VAX over RS-232 or when transferring via programmer disk drive (via More/Transfer/Input from disk). If the programmer displays `data sum = 00000000`, no data was transferred. Other hex values indicate the file transferred partially or completely.

The I/O translation format parameter is selected in the download screen. All I/O translation formats and their corresponding codes are listed in the "Translation Formats" section of your programmer's User Manual. To tell which format your data file corresponds to, view the file with an ASCII editor (or hex editor if the file is binary).

Partial or No Transfer Performed

```
Partial or no transfer performed.
Data sum = hex value
```

Probable Cause	Solution
I/O Address Offset = FFFFFFFF and first file address is not the lowest.	Absolute translation: To transfer data from file to corresponding RAM locations, enter an I/O Address Offset value of 00000000. Offset translation: If file data must begin at the programmer RAM location 0000H, find the lowest file address and use that value as the I/O Address Offset.
Improper use of Begin RAM Address and/or User Data Size.	Your file must be transferred to proper locations in programmer RAM. Edit programmer RAM to determine whether data has been transferred properly. If it hasn't, make sure your Begin RAM Address and User Data Size parameters are appropriate. Refer to the Download Data section of your User Manual for definitions and usage.
File addressing places data outside RAM address range.	View your file with an ASCII editor and look for addresses that exceed your programmer's RAM address range. To convert the decimal value of your programmer RAM size to its hex equivalent, refer to the "Data I/O Memory Chart" Application Note.

Additional Information

This warning message appears in the download screen (reached via More/Transfer/Download from the Main Menu) and indicates that a portion of your file's data has not been transferred into programmer RAM.

Transfer problems of this nature occur more often with files that have been generated with addresses in non-sequential order, where the lowest address is embedded somewhere in the middle of the file.

More About I/O Address Offset: In general, the following formula represents where in programmer RAM data will be transferred.

Physical RAM Address = [(File Address) - (I/O Offset Address)] + (Begin RAM Address)

The default I/O Address Offset, FFFFFFFF, does not represent a numerical hex value. It is simply a flag to indicate that the first address in your file will be used as the I/O Address Offset. By default, the programmer interprets the first file address as the I/O Address Offset and subtracts that value from all of the remaining addresses in the file. Consequently, the data contained in address locations lower than the first address will be lost.

Application Note

Programming 8-bit Devices for 16-bit and 32-bit Target Applications

To program 8-bit devices for 16-bit or 32-bit target applications using UniSite, the 2900, or the 3900, follow the appropriate procedure below.

Procedure for 16-bit Applications

To program two 8-bit devices in a 16-bit format, follow the procedure below:

1. Select the manufacturer and part number of the 8-bit device to be programmed.
2. Transfer the 16-bit wide file via the RS232C port or programmer disk drive. Refer to your programmer User Manual for information about these functions.
3. Set the parameters in the Program Device screen (via Program device option from the Main Menu) as follows:

   Data word width: 16
   Set auto-increment: Y
   Total set size: 1

   Note: To display all parameters, press the F4 key .
4. Program the devices.

The programmer then programs alternate devices with even addressed data and odd addressed data, causing the **Next device** parameter to alternate between "1" (first device) and "2" (second device). Furthermore, the read-only **Next operation begins at** parameter alternates between "0" (devices with even addressed data) and "1" (devices with odd addressed data).

Procedure for 32-bit Applications

To program four 8-bit devices in a 32-bit format, follow the procedure below:

1. Select the manufacturer and part number of the 8-bit device to be programmed.
2. Transfer the 32-bit wide file via the RS232C port or programmer disk drive. Refer to your programmer User Manual for information about these functions.
3. Set, the parameters in the Program Device screen (via Program Device option from Main Menu) as follows:

   Data word width 32
   Set auto-increment Y
   Total set size 1

   Note: To display all parameters, press the F4 key .
4. Program the devices.

The programmer alternately programs devices with data in every fourth RAM location, as shown in the following table:

Device Number	Programmed RAM Address
1	0,4,8,C,...
2	1,5,9,D,...
3	2,6,A,E,...
4	3,7,B,F,...

Consequently, the **Next device** parameter alternates between 1, 2, 3, and 4 (indicating the device being programmed). Furthermore, the read-only **Next operation begins at** parameter alternates between 0 (address 0000H), 1 (address 0001H), and so forth.

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Application Note

Memory Chart

Device	Decimal Size	Decimal No. Bits	Hex Addr Range	Hex No. Bytes	Hex Checksum*
2708	1K x 8	8K	0 to 3FF	400	3FC00
2716	2K x 8	16K	0 to 7FF	800	7FC00
2732	4K x 8	32K	0 to FFF	1000	FFC00
2764	8K x 8	64K	0 to 1FFF	2000	1FE000
27128	16K x 8	128K	0 to 3FFF	4000	3FC000
27256	32K x 8	256K	0 to 7FFF	8000	7F8000
27512	64K x 8	512K	0 to FFFF	10000	FF0000
27010	128K x 8	1M	0 to 1FFFF	20000	1FE0000
27020	256K x 8	2M	0 to 3FFFF	40000	3FC0000
27040	512K x 8	4M	0 to 7FFFF	80000	7F80000
27080	1024K x 8	8M	0 to FFFFF	100000	FF00000
	2048K x 8	16M	0 to 1FFFFF	200000	1FE00000
	4096K x 8	32M	0 to 3FFFFF	400000	3FC00000
	8192K x 8	64M	0 to 7FFFFF	800000	3F800000

* *Checksum of a blank EPROM where memory locations contain FF hex.*